ELEC 569A - Selected Topics in Computer Engineering
(Reconfigurable Computing)

Term - FALL 2014 (201409)

Instructor
Dr. Mihai Sima
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E-mail: msima@ece.uvic.ca

Office Hours
Days: Wednesday
Time: 1:30pm - 3:30pm
Location: EOW 313

Lectures
A-Section(s): A01 / CRN 11252
Days: Wednesday
Time: 3:30pm - 6:30pm
Location: ECS-130

Required Text
Title: Course Notes available online
Author: Mihai Sima
Publisher: UVic
Year: 2014

Optional Text
Title: Application Notes
Author: Xilinx, Altera
Publisher: Xilinx, Altera
Year:

References:

Title: Architecture and CAD for deep-submicron FPGA's
Author: V. Betz, J. Rose, A. Marquardt
Publisher: Springer
Year: 1999

Title: Design of Interconnection Networks for Programmable Logic
Author: G. Lemieux, D. Lewis
Publisher: Springer
Year: 2003

Title: Low-energy FPGA's: architecture and design
Author: V. George, J. Rabaey
Publisher: Springer
Year: 2001

Title: Research Papers on IEEE Digital Library
Assessment:

Mid-term report 10% Date: November 05, 2014
Project report 40%
Presentation 20%
Final (questions and answers) 30%

The final grade obtained from the above marking scheme will be based on the following percentage-to-grade point conversion:

<table>
<thead>
<tr>
<th>Passing Grades</th>
<th>Grade Point Value</th>
<th>Percentage for Instructor Use Only</th>
</tr>
</thead>
<tbody>
<tr>
<td>A+</td>
<td>9</td>
<td>90 - 100</td>
</tr>
<tr>
<td>A</td>
<td>8</td>
<td>85 - 89</td>
</tr>
<tr>
<td>A-</td>
<td>7</td>
<td>80 - 84</td>
</tr>
<tr>
<td>B+</td>
<td>6</td>
<td>77 - 79</td>
</tr>
<tr>
<td>B</td>
<td>5</td>
<td>73 - 76</td>
</tr>
<tr>
<td>B-</td>
<td>4</td>
<td>70 - 72</td>
</tr>
<tr>
<td>C+</td>
<td>3</td>
<td>65 - 69</td>
</tr>
<tr>
<td>C</td>
<td>2</td>
<td>60 - 64</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>50 - 59</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Failing Grades</th>
<th>Grade Point Value</th>
<th>Percentage for Instructor Use Only</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>0</td>
<td>0 - 49</td>
<td>Fail, *Conditional supplemental exam. (For undergraduate courses only)</td>
</tr>
<tr>
<td>F</td>
<td>0</td>
<td>0 - 49</td>
<td>Fail, no supplemental.</td>
</tr>
<tr>
<td>N</td>
<td>0</td>
<td>0 - 49</td>
<td>Did not write examination, Lab or otherwise complete course requirements by the end of term or session; no supplemental exam.</td>
</tr>
</tbody>
</table>

*Assignment of E grade will be at the discretion of the Course Instructor.*

The rules for supplemental examinations are found on page 80 of the current 2014/15 Undergraduate Calendar.

<table>
<thead>
<tr>
<th>Term in which E Grade Was Obtained</th>
<th>Application Deadline for Supplemental Exam</th>
<th>Supplemental Exam Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>First term of Winter Session (Sept – Dec)</td>
<td>February 28 in the following term</td>
<td>First week of following May</td>
</tr>
<tr>
<td>Second term of Winter Session (Jan – Apr)</td>
<td>June 30 in the following term</td>
<td>First week of following September</td>
</tr>
<tr>
<td>Summer Session (May – Aug)</td>
<td>October 31 in the following term</td>
<td>First week of following January</td>
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</tbody>
</table>

Deferred exams will normally be written at the start of the student's next academic term; i.e., approximately 4 months following the deferral of the exam.
Course Description

1. Course Objectives
   • Expose students to state-of-the-art FPGA architectures
   • Make students understand what the FPGA design challenge is
   • Show students where to look for information and how to read it
   • Present a literature digest for the FPGA domain

2. Learning Outcomes
   • Ability to write efficient VHDL code for FPGAs
   • Ability to choose the appropriate FPGA architecture given a specific application
   • Ability to use FPGA design tools

3. Syllabus
   • Field-Programmable Gate Arrays (FPGA) and Reconfigurable Computing paradigm
   • FPGA: major architectural classes
   • FPGA as a performance accelerator
   • Optimizing circuits for a specific FPGA architecture
   • Programmable interconnection networks
   • Low-energy FPGA's
   • CAD tools for mapping onto FPGA's

Note to Students:
Students who have issues with the conduct of the course should discuss them with the instructor first. If these discussions do not resolve the issue, then students should feel free to contact the ECE Chair by email or the ECE Chair's Secretary eceasst@uvic.ca to set up an appointment.

Accommodation of Religious Observance
See http://web.uvic.ca/calendar2014/GI/GUPo.html

Policy on Inclusivity and Diversity
See http://web.uvic.ca/calendar2014/GI/GUPo.html

Standards of Professional Behaviour
You are advised to read the Faculty of Engineering document Standards for Professional Behaviour at http://www.uvic.ca/engineering/current/undergrad/index.php#section0-25 which contains important information regarding conduct in courses, labs, and in the general use of facilities.

Cheating, plagiarism and other forms of academic fraud are taken very seriously by both the University and the Department. You should consult http://web.uvic.ca/calendar2014/FACS/UnIn/UARe/PoAcI.html for the UVic policy on academic integrity.