1. Consider a circuit shown in Fig. A1-1(a). Diode has characteristic as shown in Fig. A1-1(b). Find graphically current through resistor $R$ and calculate voltage $v_0$ across it.

![Figure A1-1](image)

2. For circuit shown in Fig. A1-2a, plot in Fig. 1-2b dependence $V_o$ vs. $V_i$.

![Figure A1-2](image)
ELEC 330: Assignment 2

ELEC 330
Assignment 2 (due in one week after posted)

1.

![Diagram A2-1]

In circuit of Fig. A2-1,

(a) find the minimum value of \( R_2 \) for Zener diode to conduct.
(b) find the maximum value of \( R_2 \) for Zener current \( I_Z \) not to exceed 10 mA.

2.

![Diagram A2-2]

For the rectifier shown in Fig. A2-2, find value for \( C \) to assure that \( (V_{rip}/V_{dc}) \times 100 \% \) is less than 1 %.

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ELEC 330 Assignment #3 (due in one week after posted)

1. For power supply shown in Fig. A3-1, assume peak voltage at node A, \( V_p = 20V \). Find ripple at nodes A and B.

![Figure A3-1](image)

2. a) Check if transistor of Fig. A3-2 operates in linear region or it is saturated.
   b) Find power dissipated in the transistor.

![Figure A3-2](image)
For the biasing circuits shown in Fig. A4-1 and Fig. A4-2,

1. Assume firm biasing for circuit of Fig. A4-2 and $\beta_{dc} = 200$ for both circuits.

   Find values for $R_B$, $R_1$ and maximum permissible value for $R_2$ to establish operating point $V_{CE} = V_{CEQ} = V_{CC}/2 = 10V$.

2. Assume that $\beta_{dc}$ has changed its value from $\beta_{dc} = 100$ to $\beta_{dc} = 200$. Find percentage of variation in $V_{CEQ}$ for both circuits.

Which circuit is better?
ELEC 330 Assignment #5 (due in one week after posted)

1. For the inverter shown in Fig. A5-1, find the maximum load current I for which \( v_o > 4 \) volts.

2. For circuit shown in Figure A5-2, find
   a) load current
   b) voltage \( V_{EC} \).
For the circuit shown in Figure A6-1,

a) find voltage $v_i$
b) find voltage $v_{o1}$ when the switch is open
c) find voltage $v_{o2}$ when the switch is closed.
Assume that JFET in Figure A7-1 can assume the following parameters:

(a) $I_{DSS} = 8$ mA and $V_P = -2$ V
(b) $I_{DSS} = 20$ mA and $V_P = -6$ V

For each case, check if JFET operates in its active region.
Figure A8-1

JFET in Figure A8-1 operates as a voltage controlled resistor. Voltage \( V_G \) can assume two values: \( V_{G1} = V_p \) and \( V_{G2} = 0 \) volts.

Find \( R_1 \) and \( R_2 \) such that the output voltage corresponding to different \( V_G \) voltages varies as 1:10.

For JFET, assume \( V_p = -2 \) V and \( I_{DSS} = 10 \) mA
ELEC 330 Assignment #9 (due in one week after posted)

1) Design an amplifier with the following specifications:

- input impedance: $R_i \geq 1 \text{M}\Omega$
- output impedance: $R_o \leq 50\Omega$
- gain: 10
- lower frequency of operation: $f_L = 100\text{ Hz}$

In the design, you can use bipolar transistors and/or enhancement type MOSFET.

2) Confirm your design by simulation. That is, demonstrate $R_i$, $R_o$, gain and lower frequency response.

$R_i \geq 1 \text{M}\Omega$
$R_o \leq 50\Omega$