Design of a Low-Noise Preamplifier for Nerve Cuff Electrode Recording

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***Abstract*—This paper discusses certain important issues involved in the design of a nerve signal preamplifier for implantable neuroprostheses. Since the electroneurogram signal measured from cuff electrodes is typically on the order of 1 μV, a very low-noise interface is essential. We present the argument for the use of BiCMOS technology in this application and then describe the design and evaluation of a complete preamplifier fabricated in a 0.8-μm double-metal double-poly process. The preamplifier has a nominal voltage gain of 100, a bandwidth of 15 kHz, and a measured equivalent input-referred noise voltage spectral density of 3.3 nV/$\sqrt{\text{Hz}}$ at 1 kHz. The total input-referred rms noise voltage in a bandwidth 1 Hz–10 kHz is 290 nV, the power consumption is 1.3 mW from $\pm$2.5-V power supplies, and the active area is 0.3 mm^2.**

***Index Terms*—Cuff, low-noise amplifier (LNA), nerve signal amplifier, neuroprostheses.**

I. Introduction

ALTHOUGH most neuroprostheses are stimulators of the nervous system, one of the challenges currently facing researchers is to enable neural signals (*electroneurogram*, ENG) to be used as *inputs*, either as command sources or to provide feedback in neuroprosthetic systems. ENG signals recorded from insulating cuffs fitted with electrodes and placed around nerves may be used instead of artificial sensors in implants for *functional electrical stimulation* (FES). Applications that have been investigated include the correction of foot-drop after stroke, hand grasp in tetraplegic patients, and bladder voiding [1]–[4].

The amplitude of the ENG signal recorded using this method depends to some extent on the dimensions of the nerve cuff but is typically on the order of 1-μV rms with a broad flat power spectral density (PSD) centered at about 1–2 kHz. The signal is embedded in noise generated by various mechanisms, notably white noise from the interstitial fluid and from the electrode–tissue interface. Amplifiers also contribute white noise and additionally, especially in the case of MOS-based circuits, flicker noise ($1/f$), which, because of its spectrum, can be harmful in a low-frequency application such as this [5]. The smallness of the signal and the prevalence of noise sources emphasize the need for a very low-noise interface, which is the subject of this paper.

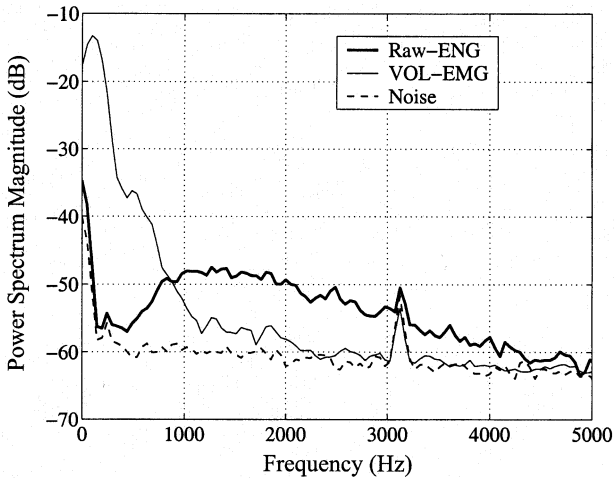

Fig. 1. Power spectral densities of ENG, EMG, and background noise recorded from a cuff implanted around the digital nerve in a human hand [source: Dr M. Haughland, SMI, Aalborg, Denmark].

In addition to noise, interfering signals can have amplitudes of many millivolts. The main sources of such interference are the electromyographic (EMG) potentials generated by active muscles near the cuff. The EMG spectrum peaks at about 100 Hz. A plot of the PSDs of typical human EMG and ENG signals is shown in Fig. 1, together with the background noise level. In order to reduce the effects of the EMG potentials, it is usual to employ a tripolar electrode structure, of which several are available, as discussed in more detail in Section II. However, these arrangements suffer from the effects of manufacturing tolerance and time-varying changes in the tissue properties, both of which can lead to failure of the cancellation process and, hence, significant EMG breakthrough. This problem can be overcome by tuning the recording system adaptively using a simple feedback control system of the type described in [6] and [7].

In order to simplify the design of the adaptive control system it is preceded by two preamplifiers, cascaded with variable gain differential amplifiers which form the first stages of the control system [7]. Each preamplifier is designed to provide optimum performance in terms of noise and power consumption and to have sufficient voltage gain so that noise is not an issue in the design of the subsequent adaptive stages. A nominal value of 100 was chosen as being adequate in this respect, but this is not

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TABLE I
PREAMPLIFIER SPECIFICATION

Parameter	Specification
Power supply	± 2.5 V
Power consumption	< 2 mW
Circuit area	as small as possible
Gain	100
–3 dB frequency	15 kHz
CMRR @ 1 kHz	100 dB
PSRR @ 1 kHz	
V_{DD}	> 40 dB
V_{SS}	> 40 dB
Total input-referred noise voltage PSD	
@ 1 Hz	$< 20\,\text{nV}/\sqrt{\text{Hz}}$
@ 1 kHz	$< 4\,\text{nV}/\sqrt{\text{Hz}}$
Total input-referred noise current PSD	
@ 1Hz	$< 35\,\text{pA}/\sqrt{\text{Hz}}$
@ 1kHz	$< 5\,\text{pA}/\sqrt{\text{Hz}}$
Total input-referred r.m.s. noise voltage (1 Hz – 10 kHz)	300 nV
Residual input DC base current	100 nA

by any means a critical parameter. Any residual differential gain errors between the two channels will be cancelled by the action of the control system [7]. In addition, since future work involves the development of multielectrode nerve cuff systems requiring arrays of ten or more preamplifiers, circuit area is a significant design issue.

Although many integrated circuit amplifiers have been proposed for use with bioelectric signals [8]–[13], existing circuits tend to have excessive power consumption and, in particular, cannot meet the noise specification required for nerve cuff recordings. Given the very small signal levels, a value of 300 nV for the input-referred rms noise voltage in a bandwidth 1 Hz–10 kHz has been chosen (see Table I).

This paper describes the design and evaluation of the preamplifiers to the outline specification given in Table I. A comparison between three candidate designs is presented. Two designs use MOS input stages and one has bipolar inputs. We seek to establish that in this application an optimum arrangement in terms of noise performance, size, and power consumption employs n-p-n bipolar input transistors in a BiCMOS design. Although it has been suggested that MOS input stages operating in weak inversion can be used to advantage in this type of application [8], the comparison example presented shows that this can only be achieved at the cost of increased power consumption and an unacceptably large increase in die area. Note that although the preamplifier described in this paper was designed for use in conjunction with an adaptive true-tripolar cuff, it can be seen as a generic very low-noise interface to any configuration of nerve cuff electrodes.

The outline of this paper is as follows. In Section II, the principles of ENG recording from nerve cuff electrodes are reviewed briefly. Design issues for the preamplifier are discussed in Section III and simulation results for the three candidate designs are presented in Section IV. Measurement results for the fabricated BiCMOS preamplifier are reported in Section V and, finally, conclusions are drawn in Section VI.

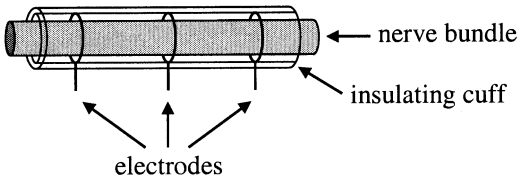

Fig. 2. Insulating cuff and tripolar electrode assembly fitted to a nerve bundle.

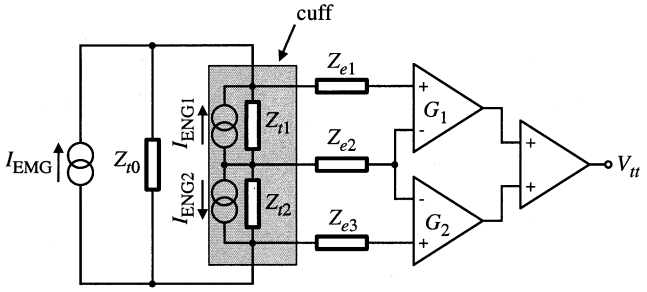

Fig. 3. True-tripole arrangement.

II. PRINCIPLES OF ENG RECORDING FROM NERVE CUFFS

Nerve cuff electrodes are currently one of the most promising recording devices for chronic implantation in humans, with safe implantation being reported for as long as 15 years [14]. One of the simplest types of nerve cuffs is a split cylinder containing three equally spaced ring electrodes embedded in the wall, as shown in Fig. 2. This structure is called a *tripole* and with such a symmetrical structure, the interfering signals appearing between each of the outer electrodes and the center electrode are equal and opposite and can be cancelled by a suitably designed differential amplifier arrangement. In practice, as already noted, exact cancellation is unlikely due to the effects of manufacturing tolerances in the design of the cuff and tissue inhomogeneity. In the example shown in Fig. 2, an insulating cuff of length L and internal diameter D is shown fitted with three equally spaced circular electrodes. L is typically 2–3 cm while D is typically about 1 mm depending on the diameter of the enclosed nerve. To a first approximation, the nerve is an insulator, while the space between the nerve bundle and the cuff is filled with connective tissue and/or conducting fluid.

In one possible configuration, the two outer electrodes are connected to one input of a differential amplifier and the remaining central electrode is connected to the second input. This arrangement is termed the *quasi-tripole* [14], [15], which has been used in a number of experimental studies and FES applications. However, EMG rejection by the quasi-tripole relies on perfect symmetry in cuff geometry and tissue resistivity, which will only be an approximation, at least due to manufacturing tolerances. Its performance is also affected by slowly time-varying parameter changes due to the effects of tissue regrowth.

An alternative configuration shown in Fig. 3, termed the *true-tripole* [16], employs the same split cylinder and three electrode rings as the quasi-tripole. In this arrangement, the two outer electrodes are not shunted together but are connected to two separate differential amplifiers with gains G_1 and G_2. The center electrode is then connected to the remaining input on both amplifiers. The outputs from the differential amplifiers are then summed in a third amplifier whose output V_{tt} is the recorded

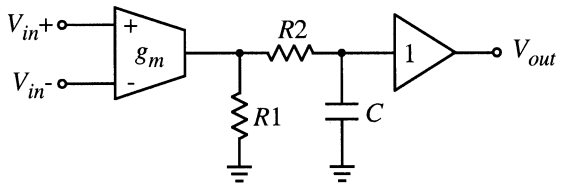

Fig. 4. Basic preamplifier architecture.

signal. In the cuff model of Fig. 3, Z_{t1} and Z_{t2} (typically 1 kΩ) represent the tissue impedances inside the cuff, Z_{t0} (typically 100 Ω) is the tissue impedance outside the cuff, Z_{e1}, Z_{e2}, and Z_{e3} (typically 1 kΩ) are the electrode–tissue contact impedances, I_{EMG} is the interfering EMG current that flows in the cuff, and I_{ENG1} I_{ENG2} are the ENG currents.

The main benefits of the true-tripole system are: 1) the amplitude of the ENG signal recorded is about twice that of the quasi-tripole and 2) the gains of the input amplifiers can be adjusted independently to compensate for any imbalance, including time-varying parameter variations. It is this feature that permits the form of adaptive adjustment employed by the control system [7]. Note that the true-tripole is much more sensitive to differences in impedance than the quasi-tripole and that without some form of adaptive compensation, its practical application is questionable [6].

III. Design Considerations

In this application, both very low-noise and low-power consumption are critical. In addition, since we intend ultimately to use an array of these preamplifiers in a multielectrode cuff system, die area is also significant, although no exact specification is given in Table I. Bearing these factors in mind, a single-stage feedforward architecture was chosen. This was possible since the preamplifiers are ac coupled to the subsequent (adaptive) stages so dc offsets occurring at the preamplifier output are not significant. In addition, although the absolute gain of each preamplifier will be less repeatable than for, say, a two-stage amplifier with feedback, this is less important than the differential gain errors introduced into the two channels of the control system. These differential gains are likely to be small (e.g., the ratio of two polysilicon resistors on the same die is specified to $\pm$1% in the chosen process [17]) and can be corrected by the control system, which is designed for a pull-in range of $\pm$10%.

The basic arrangement is shown in Fig. 4 and consists of an operational transconductance amplifier (OTA) terminated in a load resistor ($R1$), a low-pass filter ($R2$ and C), and an output buffer (for testing purposes). The combination of $R2$ and C is chosen to restrict the bandwidth to about 15 kHz, which is suitable for this application. The candidate OTA circuits shown in Fig. 5 are conventional, consisting of a differential pair transconductance stage terminated in a current mirror. Three possible OTA architectures were considered: MOS transistors throughout, consisting of a *p*MOS differential stage and an *n*MOS mirror using: 1) weak inversion; 2) strong inversion; and 3) a BiCMOS approach using n-p-n bipolar transistors in the differential pair with *p*MOS transistors in strong inversion for the current mirror. The input-referred noise voltage was

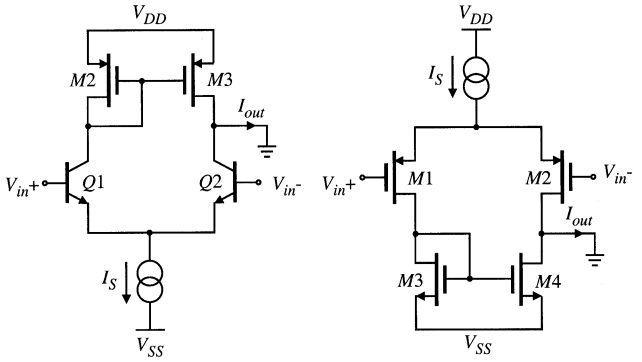

Fig. 5. Candidate OTA circuits.

evaluated and simulated in each of these types of OTA. For the bipolar case, the input-referred noise current was taken into account by passing it through a noiseless 1-kΩ resistance (representing the approximate ohmic resistance of the cuff electrodes in the relevant frequency band but noiseless to avoid including any source noise).

In addition to the OTA stages, the final BiCMOS preamplifier contains circuitry to cancel the base currents of the input transistors. Although primarily intended for ac coupling to the nerve tissue, a future application requires dc coupling. In either case, we want to find out what the safe direct current can be, whether capacitor leakage current or residual base bias current. *In vitro* experiments are in progress to determine this.

A. Basis of Comparison

Since the maximum permitted dc power dissipation is 2 mW with $\pm$2.5-V power supplies, the maximum tail current I_S for the OTA is limited to 400 μA. This immediately sets upper bounds on the transconductance gain (g_m) for the BiCMOS and CMOS weak inversion OTAs of 15 and 10 mA/V, respectively (the transconductance gain for CMOS in strong inversion is a function of the device aspect ratio W/L, in addition to the tail current). Also, since the nominal voltage gain is required to be 100, knowledge of g_m fixes the value of the load resistor $R1$. Because the amplifier noise depends on I_S (all cases) and W/L (CMOS versions), knowledge of the maximum power dissipation, supply voltages, nominal voltage gain and target input-referred rms noise voltage sets the framework for the comparison discussed below.

B. Input-Referred Noise Voltage

The input-referred noise voltage of CMOS OTAs, first discussed in [18], is dominated by flicker $(1/f)$ noise at low frequencies and thermal/shot noise at higher frequencies. The frequency at which the $1/f$ noise tail intersects the noise floor is called the flicker-noise corner frequency [5]. By representing the noise sources of each transistor by a voltage source at its input, the total input-referred noise contribution can be calculated by considering the voltage gains from the device to the amplifier output. For both strong and weak inversion MOS transistors the input-referred flicker-noise voltage model is [5]

$$\overline{v_f^2} = \frac{KF}{C_{\mathrm{ox}}WLf}\Delta f \tag{1}$$

TABLE II
PROCEDURE FOR MINIMIZING THE NOISE FLOOR AND THE $1/f$ NOISE

OTA Circuit	Minimize Noise Floor	Minimize $1/f$ Noise
CMOS weak inversion	strong function of $1/g_m$	maximize all transistor areas
CMOS strong inversion	strong function of $1/g_m$	maximize input transistor W maximize mirror transistor L
BiCMOS	reduce r_b, also depends on g_m	maximize mirror transistor L

where KF is the flicker-noise coefficient, $C_{\rm ox}$ is the gate capacitance, and f is frequency in hertz. Hence, the total input-referred flicker-noise voltage PSD for the weak inversion CMOS OTA is

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{2}{C_{\rm ox} f}\left(\frac{KF_{\rm in}}{W_{\rm in}L_{\rm in}} + \frac{KF_m}{W_m L_m}\right)\left(\frac{\rm V^2}{\rm Hz}\right) \tag{2}$$

where the subscripts $\rm in$ and m denote the input and mirror transistors, respectively, and for the strong inversion CMOS OTA is

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{2}{C_{\rm ox} f}\left(\frac{KF_{\rm in}}{W_{\rm in}L_{\rm in}} + \frac{KP_m KF_m L_{\rm in}}{KP_{\rm in}W_{\rm in}L_m^2}\right)\left(\frac{\rm V^2}{\rm Hz}\right) \tag{3}$$

where KP is the intrinsic transconductance parameter. In the case where the input MOS transistors are in strong inversion, but the mirror transistors are in weak inversion, the input-referred flicker-noise voltage PSD is

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{2}{C_{\rm ox} f}\left(\frac{KF_{\rm in}}{W_{\rm in}L_{\rm in}} + \frac{KF_m}{W_m L_m}\cdot\frac{I_D L_{\rm in}}{2U_{\rm th}^2 KP_{\rm in}W_{\rm in}}\right)\left(\frac{\rm V^2}{\rm Hz}\right) \tag{4}$$

where I_D is the drain current and $U_{\rm th}$ is the thermal voltage. Equation (4) is similar to (2) but contains another term, which modifies the mirror noise contribution. It can be shown that this term is never smaller than unity, making the all weak inversion case better in terms of flicker-noise performance. Similarly, in the case where the input transistors are in weak inversion, but the mirror transistors are in strong inversion, the input-referred flicker-noise voltage PSD is

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{2}{C_{\rm ox} f}\left(\frac{KF_{\rm in}}{W_{\rm in}L_{\rm in}} + \frac{2KF_m KP_m U_{\rm th}^2}{I_D L_m^2}\right)\left(\frac{\rm V^2}{\rm Hz}\right). \tag{5}$$

Again, the factor needed to transform (3) into (5) is never smaller than unity, resulting in an equal or higher flicker-noise performance compared with the all-strong inversion case.

For bipolar transistors, the input-referred flicker-noise voltage model is [19]

$$\overline{v_f^2} = \left((r_b + R_s)^2 \frac{I_C KF}{\beta f}\right)\Delta f \tag{6}$$

where I_C is the collector current, β is the forward current gain, r_b is the base spreading resistance, and R_s is the source (cuff) resistance. Using this model, the input-referred flicker-noise voltage PSD for the BiCMOS OTA is

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{2}{f}\left(KF_{\rm in}\frac{I_C}{\beta}(r_b + R_s)^2 + \frac{2KP_m KF_m U_{\rm th}^2}{I_C L_m^2 C_{\rm ox}}\right)\left(\frac{\rm V^2}{\rm Hz}\right). \tag{7}$$

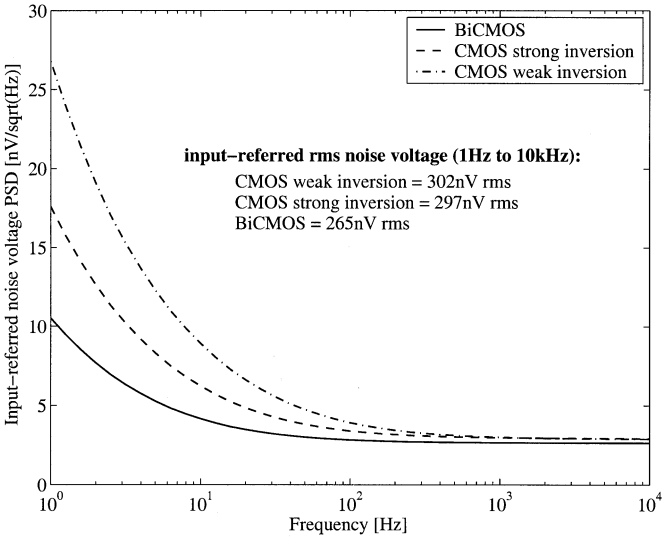

Fig. 6. Simulated input-referred noise voltage PSDs of the candidate OTAs.

At higher frequencies, the noise floor is dominated by white (thermal/shot) noise. Using the input-referred MOS thermal-noise voltage model for weak and strong inversion [5]

$$\overline{v_{\rm th}^2} = 4kT\frac{2}{3}\frac{1}{g_m}\Delta f \tag{8}$$

where k is the Boltzmann constant and T is the temperature, the input-referred thermal-noise voltage PSD for the weak inversion CMOS OTA is

$$\frac{\overline{v_{\rm th}^2}}{\Delta f} = \frac{16}{3}\cdot\frac{2kT}{g_m(in)}\left(\frac{\rm V^2}{\rm Hz}\right) \tag{9}$$

and for the strong inversion CMOS OTA is

$$\frac{\overline{v_{\rm th}^2}}{\Delta f} = \frac{16}{3}kT\left(\frac{1}{g_m(in)} + \frac{g_m(m)}{g_m^2(in)}\right)\left(\frac{\rm V^2}{\rm Hz}\right). \tag{10}$$

For the bipolar transistor, the input-referred shot/thermal-noise voltage model is [19]

$$\overline{v_{s,\rm th}^2} = \left(4kTr_b + \frac{2qI_C}{\beta}(r_b + R_s)^2\right)\Delta f \tag{11}$$

and the input-referred shot/thermal-noise voltage PSD for the BiCMOS OTA is

$$\frac{\overline{v_{s,\rm th}^2}}{\Delta f} = 4kT\left(2r_b + \frac{g_{m(in)}}{\beta}(r_b + R_s)^2 + \frac{4}{3}\frac{g_m(m)}{g_m^2(in)}\right)\left(\frac{\rm V^2}{\rm Hz}\right). \tag{12}$$

From these equations, straightforward procedures to minimize both the noise floor and the $1/f$ noise can be deduced and are summarized in Table II. Notice that for the CMOS OTAs,

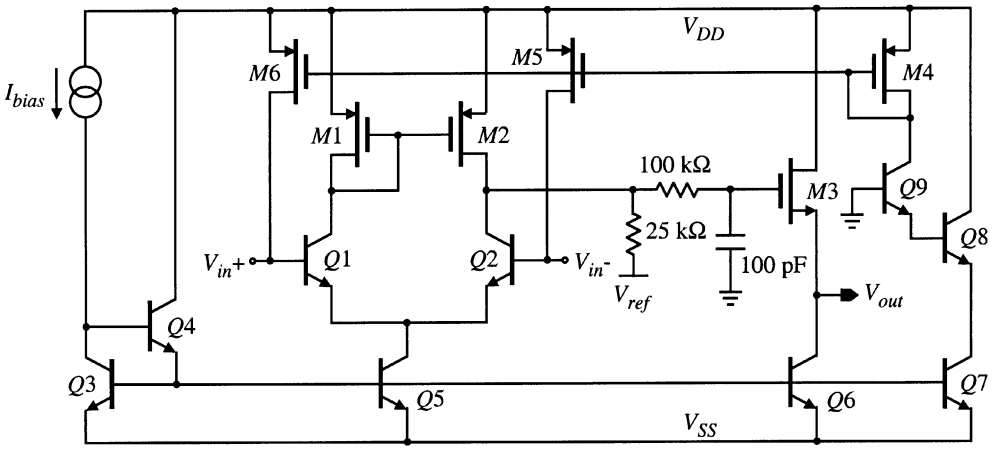

Fig. 7. Final BiCMOS preamplifier schematic diagram.

TABLE III
MAIN PARAMETERS OF THE THREE CANDIDATE OTAS

Parameter	CMOS weak inversion	CMOS strong inversion	BiCMOS
Dimensions (μm), *W/L*			
Input transistors	200,000/6	20,000/50	
Mirror transistors	150,000/12	2,400/1,200	36/12
Active area (mm^2)	6.0	7.76	0.0024
Tail current	400 μA	400 μA	200 μA
Power consumption (±2.5 V)	2 mW	2 mW	1 mW
Input-referred r.m.s. noise voltage (1 Hz – 10 kHz)	302 nV	297 nV	265 nV

the noise floor is approximately inversely proportional to g_m, whereas in the BiCMOS case, the link with g_m is less direct and contributions due to r_b and R_s can be significant. On the other hand, the $1/f$ components are dominated by the device geometries in all cases. Considering all these factors, the transistor dimensions shown in Table III were chosen.

Finally, note that for weak inversion CMOS operation, the following inequality should be satisfied [5]:

$$8I_D \leq \frac{W}{L} KP \cdot 2U_{\text{th}}^2$$

which places a further constraint on the permissible values of W and L.

IV. SIMULATED RESULTS

In order to examine the noise performance of each configuration, a model of each OTA was simulated using the Cadence analog design tools and the AMS 0.8-μm BiCMOS (double-metal double-poly) process parameters [17]. Using the principles outlined in Table II, the tail currents, MOS aspect ratios, and load resistors $R1$ were adjusted to meet the specified values of gain, power consumption, and input-referred rms noise voltage specified in Table I. The input-referred noise voltage PSDs are plotted in Fig. 6 and the total input-referred rms noise voltage of each OTA (integrated across the bandwidth 1 Hz–10 kHz) are also stated. All three designs meet the power/noise specifications, although the BiCMOS design achieves this with a dc dissipation of 1 mW compared with 2 mW for the CMOS designs.

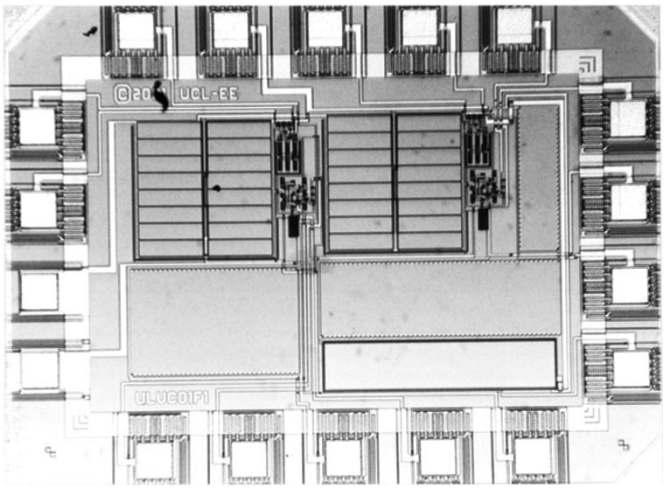

Fig. 8. Chip microphotograph.

The noise floors are quite similar for all designs, the BiCMOS having the lowest value at about 2.6 nV/$\sqrt{\text{Hz}}$. The BiCMOS case also has the best $1/f$ noise performance, followed by the strong inversion CMOS OTA. However, as Table III shows, in order to obtain this performance from the CMOS OTAs, the transistor dimensions must be made impractically large. This should be set against the extra cost of using a BiCMOS process. However, it was felt that the choice presented showed a reasonable compromise solution to the requirements of a preamplifier for an implantable neuroprosthesis where nerve cuffs are used. The specified values of common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR), measured at a spot frequency of 1 kHz, were achieved in all cases.

V. PREAMPLIFIER IMPLEMENTATION AND MEASURED RESULTS

The complete circuit schematic of the fabricated BiCMOS preamplifier is depicted in Fig. 7, while Fig. 8 shows a microphotograph of the chip (which includes two amplifiers). In addition to the components already discussed, circuitry was included to cancel the base currents of $Q1$ and $Q2$. This is very important, as significant current flowing into the tissue cannot be permitted. Transistor $Q8$ generates a replica of the base currents of $Q1$ and $Q2$, which is fed into the *p*MOS current mirror

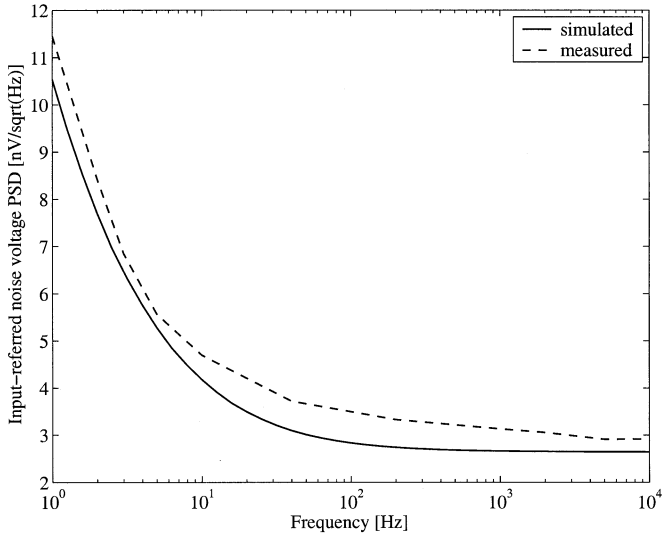

Fig. 9. Comparison between simulated and measured input-referred noise voltage PSD of the BiCMOS preamplifier.

TABLE IV
SUMMARY OF PERFORMANCE

Parameter	Specification	Measured
Power supply	± 2.5 V	± 2.5 V
Power consumption	< 2 mW	1.3 mW
Circuit area	as small as possible	0.3 mm^2
Gain	100	110
–3 dB frequency	15 kHz	14 kHz
CMRR @ 1 kHz	100 dB	82 dB
PSRR @ 1 kHz		
V_{DD}	> 40 dB	42 dB
V_{SS}	> 40 dB	54 dB
Total input-referred noise voltage PSD		
@ 1 Hz	$< 20\,nV/\sqrt{Hz}$	$11.5\,nV/\sqrt{Hz}$
@ 1 kHz	$< 4\,nV/\sqrt{Hz}$	$3.3\,nV/\sqrt{Hz}$
Total input-referred noise current PSD		
@ 1Hz	$< 35\,pA/\sqrt{Hz}$	$34\,pA/\sqrt{Hz}$
@ 1kHz	$< 5\,pA/\sqrt{Hz}$	$1.8\,pA/\sqrt{Hz}$
Total input-referred r.m.s. noise voltage (1 Hz – 10 kHz)	300 nV	290 nV
Residual input DC base current	100 nA	120 nA

$M4$, $M5$, $M6$. The common base transistor $Q9$ level shifts the current from $Q8$ and ensures that its dc conditions match those of $Q1$ and $Q2$ as far as possible. The pMOS mirror transistors $M6$ and $M5$ feed the bases of $Q1$ and $Q2$, respectively. The nMOS source follower $M3$ was included to enable the output to be measured off chip. In a complete ENG amplifier where the output is ac coupled to the next (MOS) stage, this buffer would not be necessary. I_{bias} is an external bias current source and V_{ref} is a reference bias voltage of 1 V. Note that the base of $Q9$ is connected to ground potential (i.e., halfway between the supplies) and that the inputs ($V_{in}{}^{+}$ and $V_{in}{}^{-}$) and V_{ref} are also referenced to this level. In an implanted system, this ground potential would be defined by connection to an indifferent electrode.

A comparison between the simulated and measured input-referred noise voltage PSD of the preamplifier is shown in Fig. 9. The measured results are summarized in Table IV and generally show good agreement with the simulation and the specification. The residual input dc base current could be further reduced by the use of longer transistors and/or cascoding of the dc sources (*M*4–*M*6, etc.).

VI. CONCLUSION

The design, evaluation, and fabrication of a preamplifier for an implantable ENG recording system using nerve cuffs has been presented. The preamplifier employs a simple OTA arrangement whose optimum realization for this application in terms of noise performance, size, and power consumption requires the use of BiCMOS technology. Although it is possible to meet the power/noise specification using a CMOS approach (in weak or strong inversion), this solution requires impractically large transistors. It is felt that the advantages of bipolar input transistors compared with MOS are very striking and fully justify the use of the more expensive BiCMOS process in this application.

REFERENCES

[1] M. K. Haugland and T. Sinkjaer, "Cutaneous whole nerve recordings used for correction of footdrop in hemiplegic man," *IEEE Trans. Rehab. Eng.*, vol. 3, pp. 307–317, Dec. 1995.

[2] M. Haugland, A. Lickel, J. Haase, and T. Sinkjaer, "Control of FES thumb force using slip information obtained from the cutaneous electroneurogram in quadriplegic man," *IEEE Trans. Rehab. Eng.*, vol. 7, pp. 215–227, June 1999.

[3] M. K. Haugland, J. A. Hoffer, and T. Sinkjaer, "Skin contact force information in sensory nerve signals recorded by implanted cuff electrodes," *IEEE Trans. Biomed. Eng.*, vol. 2, pp. 18–28, Mar. 1994.

[4] S. Jezernik and T. Sinkjaer, "Detecting sudden bladder pressure increases from the pelvic nerve afferent activity," in *Proc. 20th Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, vol. 5, Hong Kong, 1998, pp. 2532–2535.

[5] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.

[6] M. Rahal, J. Winter, J. Taylor, and N. Donaldson, "Adaptive interference reduction (AIR) in cuff electrode recordings," in *Proc. 1st Joint IEEE EMBS/BMES Conf.*, vol. 1, Atlanta, GA, 1999, p. 419.

[7] I. Triantis, R. Rieger, J. Taylor, A. Demosthenous, and N. Donaldson, "A CMOS interference reduction system for nerve cuff recordings," in *Proc. 28th Eur. Solid-State Circuits Conf. (ESSCIRC)*, Florence, Italy, 2002, pp. 113–116.

[8] K. Papathanasiou and T. L. Ehmann, "An implantable CMOS signal conditioning system for recording nerve signals with cuff electrodes," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, vol. 5, Geneva, Switzerland, 2000, pp. 281–284.

[9] F. Callias, F. H. Salchli, and D. Girard, "A set of four ICs in CMOS technology for a programmable hearing aid," *IEEE J. Solid-State Circuits*, vol. 24, pp. 301–321, Apr. 1989.

[10] M. S. J. Steyaert and W. M. C. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1163–1168, Dec. 1987.

[11] R. R. Harrison and C. Charles, "A low-power low-noise amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, pp. 958–965, June 2003.

[12] M. Sahin and D. Durand, "An interface for nerve recording and stimulation with cuff electrodes," in *Proc. 19th Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, vol. 5, Chicago, IL, 1997, pp. 2004–2005.

[13] P. Mohseni and K. Najafi, "A low power fully integrated bandpass operational amplifier for biomedical neural recording applications," in *Proc. 2nd Joint EMBS/BMES Conf.*, vol. 3, Houston, TX, pp. 2111–2112.

[14] J. J. Struijk, M. Thomsen, J. O. Larsen, and T. Sinkjaer, "Cuff electrodes for long-term recording of natural sensory information," *IEEE Eng. Med. Biol. Mag.*, vol. 18, pp. 91–98, May–June 1999.

[15] M. Sahin, D. M. Durand, and M. A. Haxhiu, "Whole nerve recordings with the spiral nerve cuff electrode," in *Proc. 16th Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, vol. 1, Baltimore, MD, 1994, pp. 372–373.

[16] C. Pflaum, R. R. Riso, and G. Wiesspeiner, "Performance of alternative amplifier configurations for tripolar nerve cuff recorded ENG," in *Proc. 18th Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, vol. 1, Amsterdam, The Netherlands, 1996, pp. 375–376.
[17] "0.8-μm BiCMOS process parameters," Austria Micro Systems AG, Doc. 9933008, Rev. 2.0, May 2001.
[18] J.-C. Bertails, "Low-frequency noise considerations for MOS amplifier design," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 773–776, Aug. 1979.
[19] R. Motchenbacher, *Low-Noise Electronic Design*. New York: Wiley, 1973.

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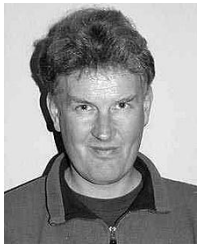

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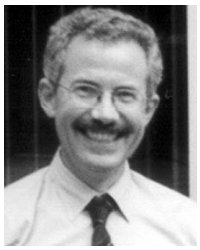

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