A LOW NOISE CMOS AMPLIFIER FOR ENG SIGNALS

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ABSTRACT

The development of an integrated amplifier intended to record electrical signals from extracellular peripheral nerves, using cuff electrodes, is presented. In order to minimize the flicker noise generated by the CMOS circuitry, a chopper full differential amplifier is implemented. The amplifier has a gain of 74 dB, a bandwidth of 3 kHz and a power dissipation of 1.3 mWatts, with 5 V power supply. Equivalent input-referred noise level of 6.6 nV/(Hz)$^{0.5}$ has been achieved, obtaining a noise efficiency factor of 5.3, which is clearly competitive, compared with other developed recording amplifiers reported in the literature. The amplifier has been fabricated with a fully CMOS 0.7 μm technology (one poly, two metals, self aligned twin-well CMOS process) and the active area is 2.7 mm^2. In vivo nerve recordings are provided to demonstrate the feasibility of the amplifier.

1. INTRODUCTION

The recording of neural signals or ENG signals, allows the use of sensory signals as feedback information to control implantable stimulators, which can be a part of a neuroprosthesis. In order to develop a recording system for ENG signals, the electrodes and the amplifier system have to be carefully chosen and designed.

Cuff electrodes [1] (composed of Pt-Ir contacts attached to the inner wall of a silicone tube) are preferred since the isolation tube provides not only an enlargement of the neural recorded signal in comparison with other kinds of invasive electrodes but also a reduction of interference produced by the electrical signals coming directly from the muscle, or EMG signals, when a balance contact impedance is achieved.

Neural signals are characterized by a low amplitude signal (several microvolts); low bandwidth (around 1.2 khz); an electrode offset voltage (around several hundreds of mvolts) and an inherent electrode impedance.

In general, in a recording system, there is an input stage prior to the amplifier for eliminating the electrode dc offset, which can cause the saturation of the amplifier and also neglects any direct current passing from the amplifier towards the electrode, which can damage the tissue surrounding the electrode, and even the nerve functionality. Different input stage structures to provide this dc baseline stabilization can be found in the literature: for non implantable versions transformer or simply a capacitor in series with the electrode [1]; and also for integrated and implantable implementations [2]. In this work, and for the in vivo testing of the implemented amplifier, an external capacitor and resistor have been used. For a totally integrated version, the inclusion of an integrated capacitor and a resistor, implemented with sub-threshold biased MOS transistors is a feasible option to achieve the low cutoff frequency.

The amplifier constitutes the second and more important stage. In order to be effective, a differential, low noise, high common mode rejection ratio (CMRR) and high gain amplifier needs to be used. One of the main features in the design of very low signal amplifiers is the intrinsic electric noise of the devices. Many examples of neural recording amplifiers can be found in the literature. Most of them use CMOS technology, for low cost systems or BiCMOS technology in order to decrease noise [3]. The use of MOS transistors to implement amplifiers working at low frequencies implies restrictions due to the intrinsic flicker noise (1/f) which can represent a serious drawback. Since flicker noise is inversely proportional to the transistor gate area, the gate enlargement reduces the noise with an area, speed and power cost. Autozero and chopper stabilization techniques [4] represent two specific techniques focused on the flicker noise reduction. The chopper technique is based on the translation of the signal (due to an amplitude modulation) to frequencies where the flicker noise effect can be neglected. In the literature several examples of chopper amplifiers are found, showing all of them a very low noise behavior [5]. In particular, Dagtekin et al. recently reported simulated results of a chopper amplifier applied to neural recording, although no experimental data was shown [6].

In this paper we are focused on the development of an ENG integrated CMOS amplifier using the chopper stabilization technique.

2. SYSTEM DESIGN

The design proposed on this paper is focused on the amplification of neural signals (unit action potentials or small amplitude compound action potentials) with amplitudes as low as several microvolts. As we said in the introduction, the present work describes an ENG CMOS amplifier based on the chopper stabilization technique.

In this technique, the input signal is modulated, amplified, band pass filtered and demodulated back to its original frequency (demodulation is carried out by the similar first modulator structure followed by a low pass filter that allows to recover the original band base spectrum). By choosing the adequate parameters, the input noise spectrum (corresponding to the dominant flicker noise for small frequencies) is translated to higher frequencies, obtaining at low frequencies a white spectrum. After the chopper process, the corresponding base band output power spectral density has an approximated base band value of:

$$S_{out}(f) \cong S_0(1 + 0.8525 f_k T) \qquad (1)$$

being T the sampling period of the modulation, S_0 the thermal noise power spectral density, and f_k the noise corner frequency (corresponding to the intersection between flicker and thermal noise frequency).

A reduction can be obtained just increasing the chopper frequency. However, the sampling frequency needs to be smaller than the amplifier cutoff frequency in order to avoid signal frequency distortion [4].

On the other hand, due to the non-idealities of the switches forming the modulator, the chopper process generates undesirable spikes which appear as high frequency components in the spectrum (always higher than the chopper frequency). In order to eliminate these components, in our system a band pass filter with a center frequency equal to the chopper frequency and a bandwidth large enough to allow to pass all the signal has been chosen. In this section we detail the design of each circuit forming the chopper amplifier: modulator, preamplifier, band pass filter and low pass filter.

2.1 Modulator

The modulator is composed of four NMOS transistors that act as switches, driven by two complementary clock signals [4]. Since no phase change takes place during the amplification and filter process, both modulators can be driven by the same clock. Transistor dimensions have been selected taking into account the spikes time constant (τ) caused by the charge injection:

$$\tau = R_{on} C_{in} \qquad (2)$$

R_{on} being the switch resistance and Cin being the amplifier input capacitance. This time constant must be smaller than the chopper period. In our case, the NMOS transistors have been designed to achieve a time constant three orders of magnitude smaller than the chopper period.

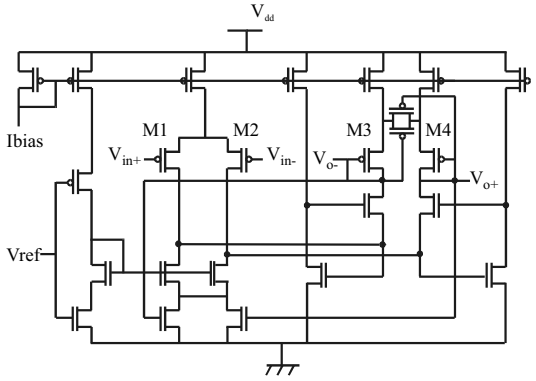

Figure 1. *Preamplifier electrical scheme*

2.2 Preamplifier

The preamplifier, as the first stage of the chopper amplifier, is responsible of the circuit noise performance. If a good frequency selection is done, the thermal noise will be responsible of the overall noise and thus, an ultra low noise amplifier can be achieved .

	Band Pass Filter		Low Pass Filter	
	(W/L)	I_D	(W/L)	I_D
M_1, M_2	20/5	5 μA	20/5	16.6 μA
M_3, M_4	10/20	2 μA	10/90	0.8 μA
M_5, M_6	4/60	1 μA	4/60	0.6 μA
M_7, M_8	10/20	2 μA	10/90	0.8 μA
C	22 pF		22 pF	
	Preamplifier			
	(W/L)		I_D	
M_1, M_2	900/6		60 μA	
M_3, M_4	40/8		10 μA	

Table I*. Main transistor dimensions and biasing currents*

The preamplifier (shown in Figure 1) is composed of a differential PMOS transconductance input stage (M1 and M2 devices) with a common mode feedback, followed by a transimpedance stage in a folded cascode configuration (M3 and M4 devices) [5]. This architecture, provides a differential voltage gain which

results from the ratio of the channel transconductance (gm_1) of the input stage and the channel transconductance (gm_2) of the transimpedance output stage. Table 1 summarizes the main bias currents and transistor dimensions for this preamplifier.

Since the thermal noise is inversely proportional to the transconductance input stage (g_m), the current biasing and transistor dimensions have been adapted to obtain a high input transconductance value (1.082 μA/V corresponding to gm_1). A linearized transimpedance stage has been used to implement the transimpedance output stage [7], obtaining a channel conductance value of 20.8 μA/V for M3 and M4 MOS transistors.

The designed amplifier has a 32 dB DC gain with a 380 kHz cutoff frequency, and a corner noise frequency of 2.5 kHz with a 3.7 $nV/(Hz)^{0.5}$ thermal noise (simulated results). Its active area is 650μm x 210μm.

2.3 Band pass and low pass filters

The band pass filter is used as a selective stage, with its center frequency locked to the chopper frequency, so that a minimization in the residual offset produced by the spikes can be achieved.

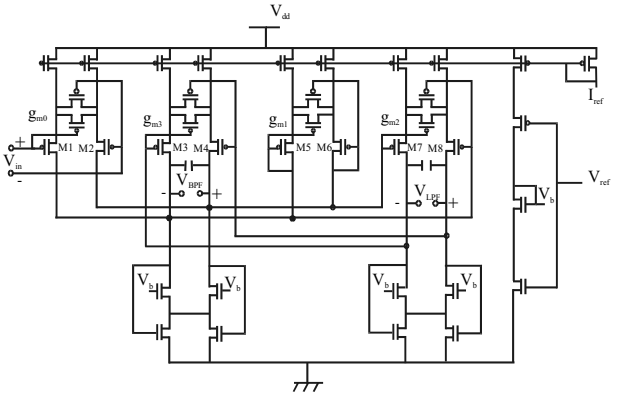

***Figure 2**. Band-pass filter and Low-pass filter scheme*

Both, band pass and low pass continuous time filters have been designed using the Gm-C technique [7]. They are composed basically of a resonator loop (Fig. 2), implemented with two integrators, built with a linearized transconductance amplifier and floating capacitors. Table 1 summarizes the main bias currents and transistor dimensions.

In the case of the band pass filter, a center frequency of 25 kHz, corresponding to the chopper frequency and a bandwidth of 10 kHz has been implemented, obtaining a quality factor Q of 2.5. This bandwidth value assures the neural signal will pass since it implies an amplifier effective bandwidth of 5 kHz. Taking into account the correction due to the voltage controlled degenerated resistors, an effective value of 7.7 μA/V for g_{m2} and g_{m3} and 22 pF for the floating capacitors have been used to obtain the center frequency. By choosing an appropriate value for $g_{m1,}$ the bandwidth is fixed and finally, g_{m0} establish the 23 dB gain at the resonance frequency. The low pass filter has been designed to have a low cutoff frequency of 4 kHz, in order to reduce noise, and a 20 dB DC gain.

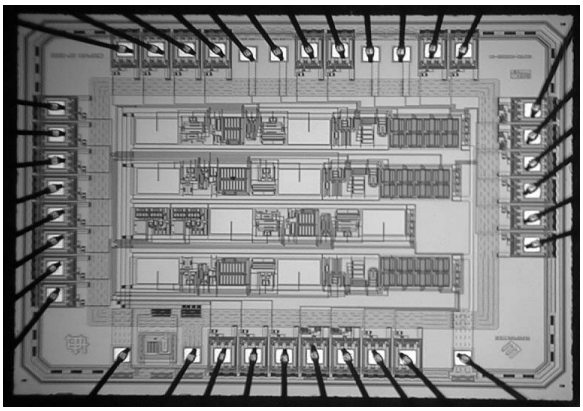

***Figure 3.** Photograph of the implemented amplifier*

3. EXPERIMENTAL RESULTS

All the circuitry has been designed using standard Mietec 0.7 μm CMOS technology. Figure 3 shows a picture of the implemented chip. It is composed of a full chopper amplifier along with an unrouted replica of every module that assures an easy individual test. The full amplifier area is 2.7 mm^2 although the chip core area is (2648 x 2031)μm^2.

Preamplifier, band pass and low pass filters frequency responses have been tested. Table 2 summarizes the main measured results of the implemented chopper amplifier.

A noise analysis has been performed using a 16 bits data acquisition card (NI_PCI6052E). The obtained noise spectrum corresponds to an average equivalent input white noise of 6.6 $nV/(Hz)^{0.5}$. By considering a bandwidth of 3 kHz, the corresponding input noise has an RMS value of 453 nV_{RMS}, which is low enough to amplify the small ENG signals that are in the range of μV. Moreover, taking into account that electrode impedances are in the range of few kΩ, the amplifier noise value is comparable with the noise generated by the electrode itself. As it has been previously commented, if a correct frequency selection is done, final noise will depend only on thermal noise contribution. Since thermal noise is inversely related with the transconductance (g_m), low noise can be achieved at the expense of power consumption and increment of chip area.

Supply voltage	5 V	
	Current	Gain
Preamplifier BPF LPF	193 μA 26 μA 42 μA	30.5 dB 25 dB 19.8 dB
Total DC gain	74 dB	
CMRR (25 kHz)	80 dB	
Power consump.	1.3 mW	
Bandwidth	3 kHz	
Input Noise PSD	6.6 nV/(Hz)$^{0.5}$	
Total integrated noise	453 nV	

***Table II**. Experimental characteristics of the amplifier*

To quantify and compare the performance of different low noise amplifiers, Steyaert et al [8] introduced the noise efficiency factor (NEF). Our implemented amplifier presents a NEF of 5.3. Comparing our work with the amplifiers reported in the literature until now, the designed an tested amplifier is clearly competitive [9].

Nerve signals were obtained in acute animal experiments using needle electrodes in anesthetized (pentobarbital, 50 mg/kg i.p.) Sprague-Dawley rats. In order to test in vivo the amplifier, a passive high pass filter has been used for AC-coupling. In particular, since the neural signal is center at 1 kHz, a rejection of signals under 100 Hz has been chosen to improve the SNR and also to reduce the 50 Hz interference. Compound nerve action potential (CNAP) and Motor unit action potentials (MUAP) have been recorded. Figure 4 shows three recorded compound action potentials of the fourth toe digital nerve, while the sciatic nerve is being stimulated proximally. Amplitudes around 15 μV have been measured.

4. CONCLUSIONS

As a conclusion we can state that a full system intended for the amplification of neural signals has been designed, and electrically and in vivo tested. An ac coupling has been used to eliminate the offset generated by the electrode and to fix the lower cutoff frequency for acute in vivo experiments. The integrated amplifier, implemented in a standard 0.7 μm CMOS technology, uses the chopper stabilization method and, an equivalent input-referred noise as low as 6.6 nV/(Hz)$^{0.5}$ has been achieved.

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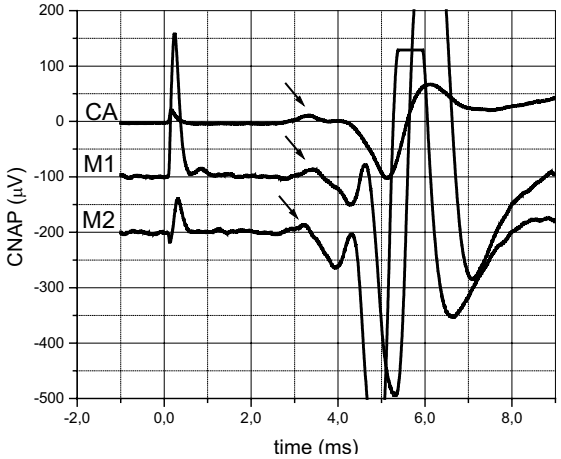

***Figure 4**. In-vivo CNAP recordings (arrows) during three stimulations using commercial amplifier (CA) and the chopper CMOS amplifier (M1 and M2). Curves are arbitrarily shifted for clarity*