Adaptive Sigma–Delta Modulation With One-Bit Quantization

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***Abstract*—A method for improving the signal-to-noise ratio (SNR) of sigma–delta modulators with one-bit quantization is presented. The two-level feedback signal of a standard sigma–delta modulator is replaced by a multilevel signal, which is a superposition of two parts. One part $s(n)$ represents a rough estimate of the instantaneous amplitude of the input signal (prediction signal), and the other $y_b(n)$ is the sign of the quantizer output, multiplied with constant b. Compared to a nonadaptive modulator, the amplitude of $y_b(n)$ is reduced. Therefore, less noise power is introduced in the quantizer, and the SNR is considerably enhanced. Signal $s(n)$ is derived numerically from the quantizer output $y_0(n)$ according to a particular adaptation algorithm. Except for the dc-level of $s(n)$, sequence $y_0(n)$ contains the full digital information of the modulator input signal. From $y_0(n)$, a digital multilevel sequence $w_0(n)$ can be calculated, which represents the digital modulator output. The price paid for the improved SNR is a moderate slew rate limitation of the input signal. The approach is basically suited for a wide class of sigma–delta modulators. Here, simulation results and an example for a practical implementation of an adaptive sigma–delta modulator of first order are presented.**

***Index Terms*—Adaptive sigma–delta modulation, analog-to-digital conversion, information compression, multilevel feedback, quantization.**

I. Introduction

SIGMA–DELTA modulation is a widely used and thoroughly investigated technique for converting an analog signal into a high-frequency digital sequence [1], [2]. The basic features of sigma–delta modulation can be summarized as follows.

1) The sampling frequency is much higher than the Nyquist frequency of the input signal (i.e., much higher than twice the maximum input frequency).
2) A low-resolution quantizer is incorporated within a feedback loop configuration.
3) The noise energy generated in the quantizer is shaped toward higher frequencies according to a so-called "noise transfer function" $\mathrm{NTF}(z)$.
4) The signal passes the modulator more or less unchanged according to a so-called "signal transfer function" $\mathrm{STF}(z)$.

The simplest modulator, a sigma–delta modulator of first order with one-bit quantization, is depicted in Fig. 1(a) as a discrete time system. It is composed of a subtraction stage, an accumulator, and a one-bit quantizer. In normal operation, the input signal $x(n)$ within the range $[-a, +a]$ is converted to the binary output sequence $y_a(n) \in \pm a$.

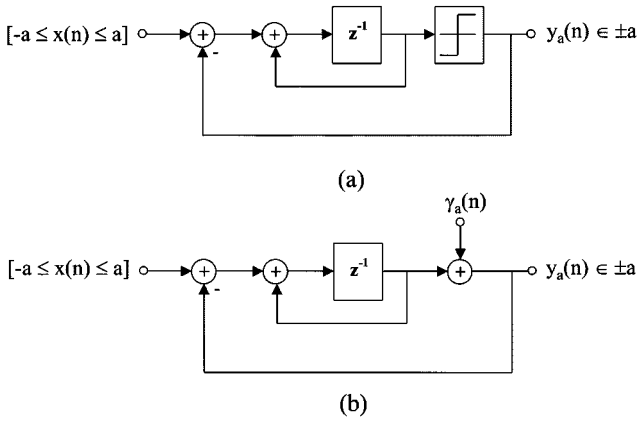

Fig. 1. Sigma–delta modulator of first order. (a) Discrete time system. (b) Linear model with additive noise source.

If the quantizer is replaced by an adder and a noise source [cf. Fig. 1(b)], the basic relationship between the z-transforms of system input $x(n)$, quantizer noise $\gamma_a(n)$, and the two-level output sequence $y(n)$ is

$$Y_a(z) = z^{-1}X(z) + (1 - z^{-1})\Gamma_a(z). \tag{1}$$

Index "a" denotes the amplitude of sequence $y_a(n)$, i.e., $y_a(n) \in \pm a$. Signal- and noise-transfer functions can be identified as $\mathrm{STF}(z) = z^{-1}$ and $\mathrm{NTF}(z) = (1 - z^{-1})$, respectively. For higher order modulators, the signal transfer function remains unchanged, and the noise transfer function becomes $\mathrm{NTF}(z) = (1 - z^{-1})^k$, where k denotes the order of the modulator.

Signal transfer function $\mathrm{STF}(z) = z^{-1}$ means that the input signal is represented in the output sequence $y_a(n)$, delayed by one sampling clock period. This transfer function does not contain any bandwidth limitations of the input signal. *Any* input signal $x(n)$ within the range $[-a, +a]$ can be processed by the sigma–delta modulator, including, e.g., discontinuous signals with step-like transitions. For the modulator depicted in Fig. 1, this can easily be demonstrated, if it is regarded as a linear (nonadaptive) delta modulator, whose input is the accumulated input $x(n)$. If the input is within the range $[-a, +a]$, the magnitude of the maximum slope of the accumulated sequence $x(n)$ is a/T (with T as sampling period). Thus, the delta modulator can always track its input, and the so-called "slope-overload conditions" cannot occur.

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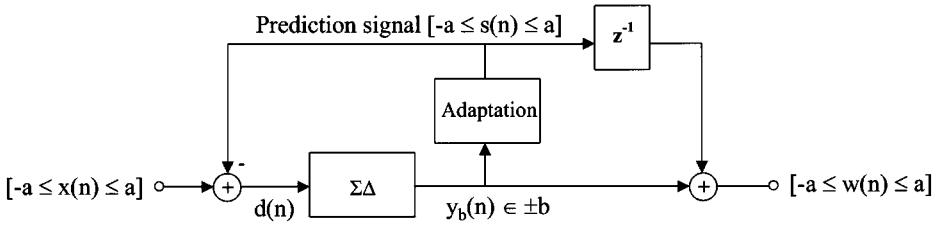

Fig. 2. Adaptive sigma–delta ($\Sigma\Delta$) modulator: principle of operation.

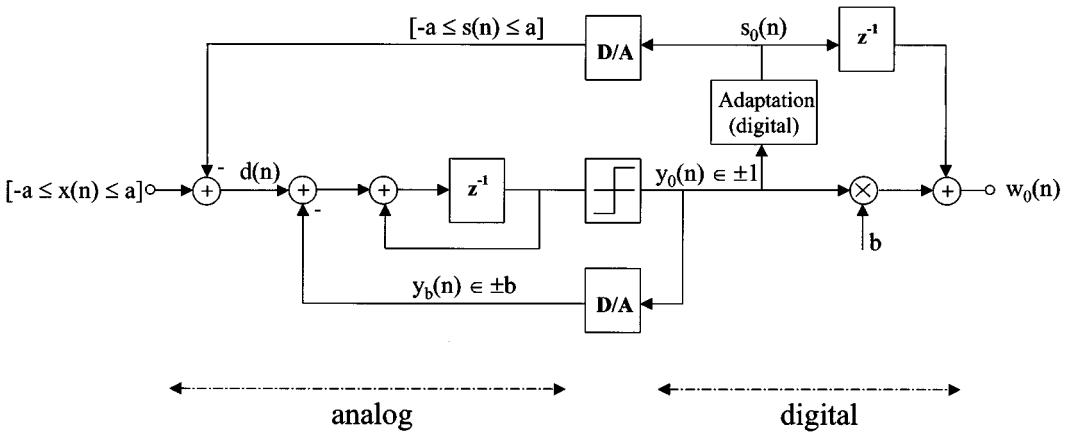

Fig. 3. Adaptive sigma–delta modulator of first order.

However, in standard applications, this basic sigma–delta feature is not exploited, since in the spectrum of the sequence $y_a(n)$, the high-frequency spectral components of the (discontinuous) input cannot be easily separated from the high-frequency spectral components due to the shaped quantization noise, and at least linear filter techniques are impractical. The decoding of discontinuous input signals requires more sophisticated nonlinear techniques, such as, e.g., the "thread algorithm," as described in [3].

II. Adaptive Sigma-Delta Modulation: Basic Concept

The idea of the present approach is explained with the help of Fig. 2. It shows a sigma–delta modulator within a closed-loop configuration. The input to this modulator is signal $d(n)$, which is the difference between the system input $x(n)$ (within range $[-a, +a]$) and signal $s(n)$. Signal $s(n)$ is a rough estimate of the input $x(n)$ and ensures that signal $d(n)$ is kept within a reduced range $[-b, +b]$ (with $b < a$). In the following, $s(n)$ is designated as "prediction signal". Signal $d(n)$ can now be digitized with a sigma–delta modulator operating within the *reduced range* $[-b, +b]$, and thus only a fraction b/a of quantization noise is generated in the quantizer as compared to the standard modulator Fig. 1.

The z-transform of sequence $y_b(n) \in \pm b$ is given by

$$Y_b(z) = z^{-1}(X(z) - S(z)) + (1 - z^{-1})^k \Gamma_b(z) \qquad (2)$$

where $\Gamma_b(z)$ is the z-transform of the noise $\gamma_b(n)$ generated in the 1-bit quantizer. The output of the adaptive sigma–delta modulator is a multilevel sequence $w(n)$. Its z-transform is obtained by

$$W(z) = Y_b(z) + z^{-1}S(z) = z^{-1}X(z) + (1 - z^{-1})^k \Gamma_b(z). \quad (3)$$

$W(z)$ exactly corresponds to $Y(z)$ in (1) for a system of first order $(k = 1)$. Signal- and noise-transfer functions remain unchanged, i.e., $\mathrm{STF}(z) = z^{-1}$ and $\mathrm{NTF}(z) = (1 - z^{-1})$. The only difference concerns the noise factor. Here the noise factor is $\Gamma_b(z)$ instead of $\Gamma_a(z)$, which means a considerable reduction of added quantization noise.

A rough expression for the gain in signal-to-noise ratio (SNR) of the adaptive technique as compared to the standard scheme is given by

$$G = 20 \log_{10}(a/b). \qquad (4)$$

III. Adaptive Sigma–Delta Modulator of First Order

Incorporating the modulator presented in Fig. 1(a) in the loop system depicted in Fig. 2 results in an adaptive sigma–delta modulator of first order, as shown in Fig. 3. In this plot, analog (physical) and digital representations of signals are distinguished from each other. Digital one- or multi-bit signals are labeled with index "0". The system can be separated into an analog and a digital section. The quantizer output $y_0(n) \in \pm 1$ and the prediction signal $s_0(n)$ are converted to the actual feedback signals $y_b(n) \in \pm b$ and $s(n)$ within $[-a, +a]$ by means of digital-to-analog (D/A) converters (note that two D/A converters are shown here for better understanding; in a practical implementation only one converter is necessary). The system output $w_0(n)$ is obtained by numerically adding signals $s_0(n)$ delayed by one clock period, and sequence $y_0(n)$, which is numerically multiplied by factor b (trivial multiplication, since $y_0(n) \in \pm 1$).

The system can also be considered a sigma–delta modulator of first order, where the overall feedback signal $s(n) + y_b(n)$ is

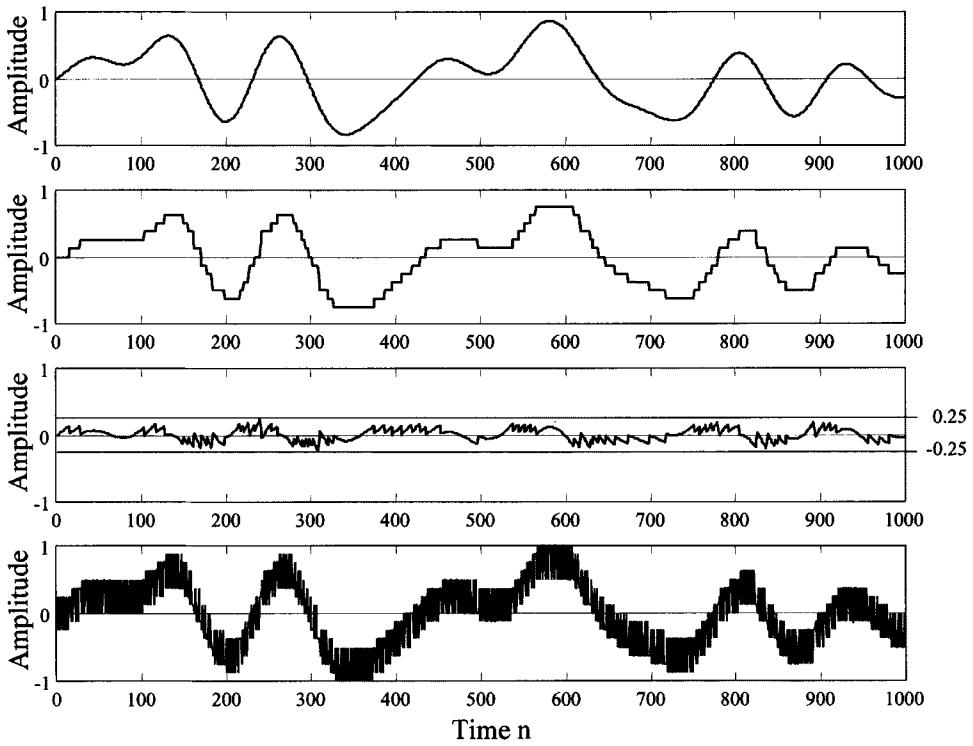

Fig. 4. Typical wave forms of an adaptive sigma–delta modulator of first order with $a = 1, b = 0.25$, and $q = 0.5$ Trace 1: input signal $x(n)$ (band-limited) Trace 2: prediction signal $s(n)$ (after D/A conversion) Trace 3: sigma–delta input signal $d(n) = x(n) - s(n)$ Trace 4: digital multi-bit output signal $w_0(n)$.

regarded as an adaptive feedback signal (hence the name "adaptive" sigma–delta modulator).

Note an interesting difference: as a general feature of standard sigma–delta modulators (first and higher orders), the feedback signal is always an analog version of the digital modulator output. For example, in a nonadaptive sigma–delta modulator of first order, the digital output $y_0(n) \in \pm 1$ is converted to the physical feedback signal $y_a(n) \in \pm a$. This is not the case in an adaptive sigma–delta modulator approach; here, the digital modulator output is $w_0(n) = s_0(n-1)+by_0(n)$, and the overall feedback signal $s(n) + y_b(n)$ is derived from the digital signal $w_0(n) = s_0(n) + by_0(n)$. The delay in $s_0(n)$ by one clock period for the digital modulator output is essential for the system performance [cf. (2) and (3)].

The way the adaptation stage has to work is intuitively clear. Code $y_0(n)$ indicates whether or not signal $d(n)$ tends to leave the range $[-b, +b]$, and signals $s_0(n)$ and thus $s(n)$ are adapted to prevent this case. If the local density of "+1" ("−1") exceeds a particular limit, $s_0(n)$ has to be increased (decreased), but otherwise it has to remain unchanged.

An example for an adaptation algorithm for an easy-to-implement system of first order is shown in Table I.

Signal $s(n)$ is a stair-like signal, where the difference between neighboring samples is $+bq, -bq$, or zero. Thus, parameter q (within the range $0 \le q \le 1$) defines the step-size of $s(n)$. Some typical signal wave forms occurring in an adaptive sigma–delta modulator with the adaptation algorithm in Table I are depicted in Fig. 4 for $a = 1, b = 0.25$, and $q = 0.5$. Trace 1 depicts a bandwidth-limited input signal $x(n)$, trace 2 the prediction signal $s(n)$. With the chosen parameters, the step-size of $s(n)$ is $bq = 0.125$. The difference signal $d(n)$

TABLE I
PREDICTION ALGORITHM FOR A SYSTEM OF FIRST ORDER (WITH $0 \le q \le 1$)

Code $y_0(n)$ $y_0(n-1)$ $y_0(n-2)$	Prediction Signal
+1 +1 +1	$s_0(n) = s_0(n-1) + bq$, upper limit: $s_0(n) \le +a-b$
-1 -1 -1	$s_0(n) = s_0(n-1) - bq$, lower limit: $s_0(n) \ge -a+b$
Other combinations	$s_0(n) = s_0(n-1)$

(trace 3) is the input of the sigma–delta modulator operated in the range $[-0.25, +0.25]$ (the limits -0.25 and $+0.25$ are shown as straight lines). The digitally computed system output $w_0(n)$ is shown in trace 4. This multilevel sequence is a considerably better digital representation of the input $x(n)$ than a two-level sequence $y_a(n) \in \pm 1$ obtained with a standard sigma–delta modulator of first order.

It should be emphasized at this point that the exact shape of $s(n)$ (here assuming that $s(n)$ is derived from $s_0(n)$ by means of an ideal A/D converter) is not crucial for the functioning of the system. It is only important that $d(n)$ be kept within the limited range $[-0.25, +0.25]$, so that it can be processed by the sigma–delta modulator operated in this range. Furthermore, signal $d(n)$ is clearly not a band-limited signal, but, as mentioned above, the sigma–delta modulator is capable of processing such a discontinuous signal.

IV. SLEW-RATE LIMITATION OF THE INPUT SIGNAL

If $d(n)$ exceeds the range $[-b, +b]$, additional quantization noise is generated. This condition can be identified as a typ-

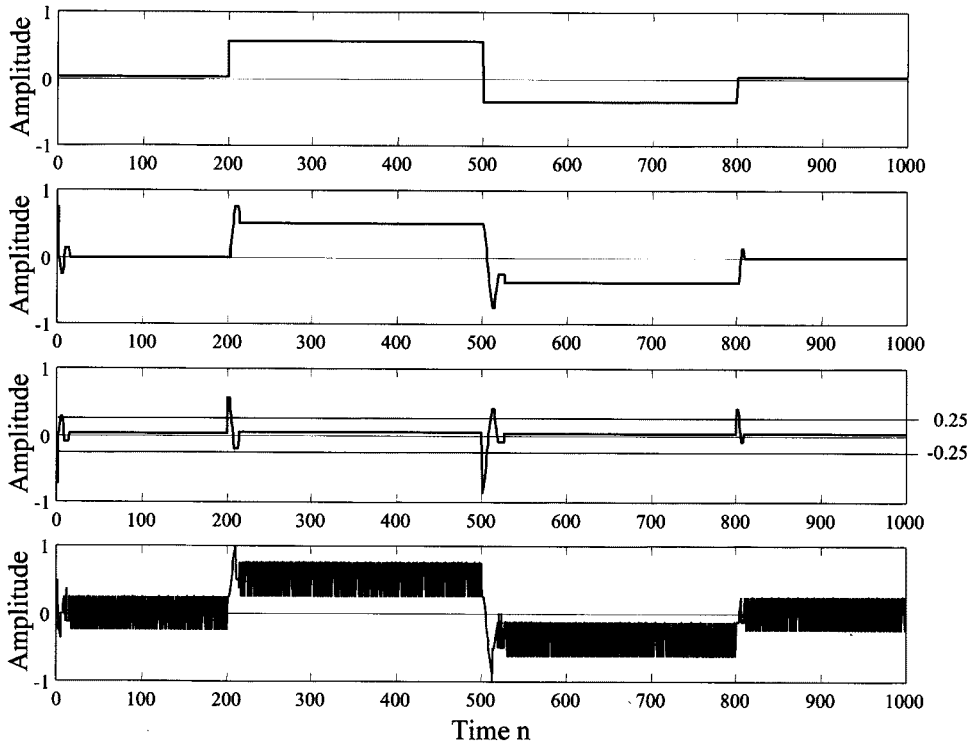

Fig. 5. Typical wave forms of an adaptive sigma–delta modulator of first order for an input with step-like transitions with $a = 1, b = 0.25$, and $q = 0.5$ Trace 1: input signal $x(n)$ (band-limited) Trace 2: prediction signal $s(n)$ (after D/A conversion) Trace 3: sigma–delta input signal $d(n) = x(n) - s(n)$ Trace 4: digital multi-bit output signal $w_0(n)$.

ical "slope-overload" condition, if the sigma–delta modulator of first order is regarded as linear delta modulator of first order, whose input is the accumulated sequence $d(n)$. Slope overload conditions occur when the prediction signal $s(n)$ cannot track the input signal $x(n)$ fast enough. With the adaptation algorithm of Table I for a system of first order, the maximum slope of $s(n)$ is bq/T. Assuming $f_x \ll 1/T$, for a sinusoidal input $x(n) = A\sin(2\pi T f_x n)$, the maximum slope is $A2\pi f_x$. This results in the absolute maximum input frequency

$$f_{x,\max} = \frac{bq}{2\pi AT}. \tag{5}$$

For example, with $b = 0.25, q = 0.5, A = 1$, and $T = 1\mu$s, the maximum input frequency is $f_{x,\max} = 19.89$ kHz.

If the input signal contains slopes steeper than $\pm bq/T$, slope overload noise is generated. Nevertheless, the system does not show any tendency to fall into unstable operation modes. An example is depicted in Fig. 5, where the input signal $x(n)$ (trace 1) contains step-like transitions. At these positions, signal $s(n)$ (trace 2) tracks $x(n)$ with limited slew-rate.

However, stable conditions are reached after a few sampling periods. As expected, signal $d(n)$ exceeds the range $[-b + b]$ (trace 3).

Fig. 5 also illustrates a typical initialization behavior. An arbitrary initial state of $s(n)$ qualitatively corresponds to the case of a step-like transition of $x(n)$. In Fig. 5, the initial condition has been set to $s(1) = 1-b = 0.75$, and signal $s(n)$ has adapted within some clock periods.

V. Signal Reconstruction from Sequence $y_0(n)$

As shown in the example in Fig. 5, signals $s_0(n)$, and thus $s(n)$, adapt from an arbitrary initial state within a short time, when the adaptation stage is within a closed loop configuration. If the adaptive sigma–delta modulator is, e.g., used as the front-end of an A/D converter, $s_0(n)$ and $y_0(n)$ are directly used to compute $w_0(n)$ and digital filters for further signal processing (for decimation etc.) can be applied.

However, when $s_0(n)$ has to be reconstructed from sequence $y_0(n)$, and the initial state of $s_0(n)$ is unknown, a principal uncertainty regarding the dc-offset of $s_0(n)$ remains. If $s_0'(n)$ designates the sequence with unknown initial state, the difference to the correct sequence $s_0(n)$ is reduced each time $s_0'(n)$ reaches the limits set by the adaptation algorithm. An example is shown in Fig. 6, where the same input signal and the same adaptation algorithm as in Fig. 4 are used (resulting in traces 1 and 2, as in Fig. 4). Trace 3 depicts signal $s_0'(n)$, if it is reconstructed from the binary sequence $y_0(n)$ only, and the initial condition is assumed to be $s_0'(1) = -(1 - b)$. As can be seen in trace 4, the difference $s_0(n) - s_0'(n)$ is successively reduced to zero, and the error reduction takes place each time $s_0'(n)$ reaches the limits $\pm(1 - b)$. Once the error has reached zero, it remains zero.

VI. Calculated SNR's for Adaptive Sigma–Delta Modulation of First Order

In Fig. 7, the SNR's of different types of sigma–delta modulators of first order are shown as a function of the power of the input signal. The input signal $x(n)$ is a periodic zero-mean noise sequence composed of $N = 10\,000$ samples, and the

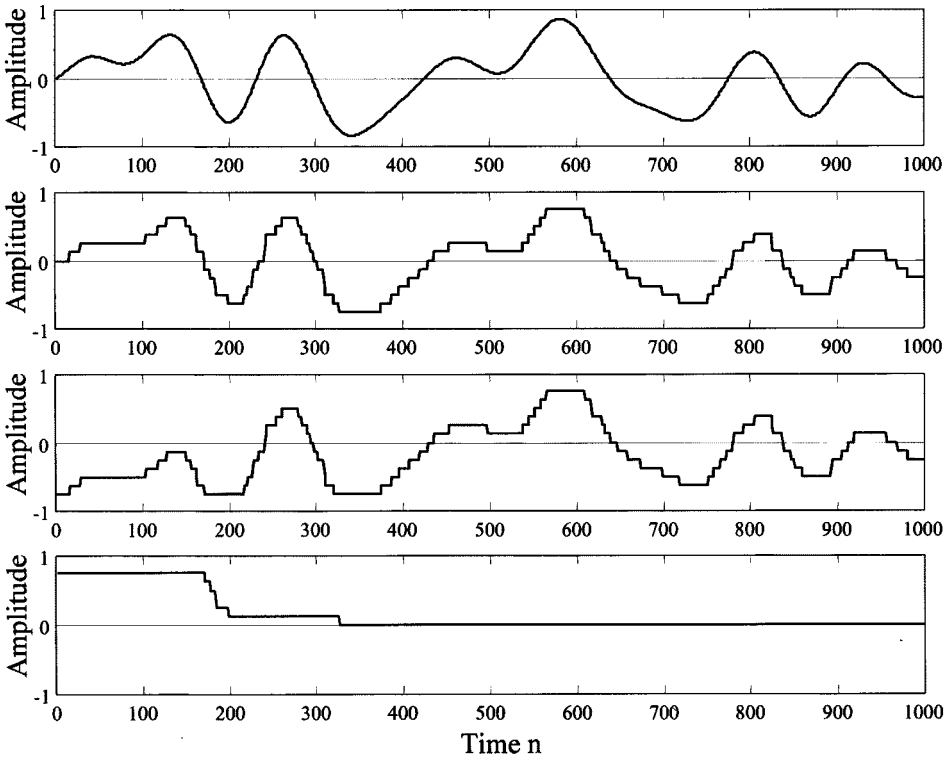

Fig. 6. Typical wave forms of an adaptive sigma–delta modulator of first order with $a = 1, b = 0.25$, and $q = 0.5$ Trace 1: input signal $x(n)$ (bandwidth-limited) Trace 2: digital prediction signal $s_0(n)$ (before D/A conversion) Trace 3: digital prediction signal $s_0'(n)$ reconstructed from $y_0(n)$ only with initial condition $s_0(1) = -(1-b)$ Trace 4: error signal $s_0(n) - s_0'(n)$.

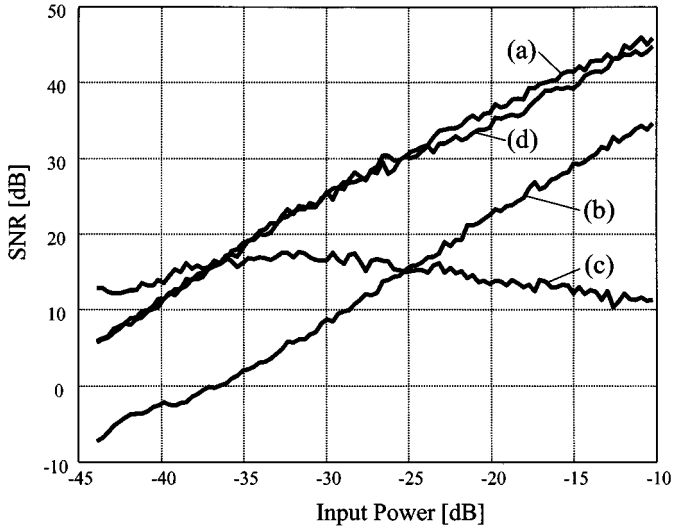

Fig. 7. Calculated SNR's with noise input signals as a function of input signal power. (a) Ideal adaptive sigma–delta modulator of first order with $a = 1, b = 0.25$, and $q = 0.5$ (b) Ideal standard sigma–delta modulator of first order with $a = 1$. (c) Gain [difference between curves (a) and (b)]. (d) Adaptive sigma–delta modulator of first order with $a = 1, b = 0.25$, and $q = 0.5$, but with nonideal D/A converter (linearity as 8-bit D/A converter with maximum error $\pm(1/2)\mathrm{LSB}$).

bandwidth is $B = 20$ kHz. Within this bandwidth, amplitudes and phases of the spectral lines are randomized. Different values of signal power are obtained by proportional amplification of this signal. The input power is referred to a reference power level of 1, which corresponds to the power of the standard sigma–delta output sequence with $y_a(n) \in \pm 1$. At the maximum input power level shown in Fig. 7 (i.e., at -9.45 dB), the maximum signal amplitude reaches 0.99. For the adaptive sigma–delta modulators, the adaptation algorithm of Table I is used, and the system parameters are set to $a = 1, b = 0.25$, and $q = 0.5$, and $a = 1$ is assumed for the standard modulator. The sampling rate for all systems is $1/T = 1$ MHz and the SNR's are computed within $B = 20$ kHz.

The maximum SNR is obtained with an ideal adaptive sigma–delta modulator. This system is clearly superior to the (ideal) standard system: the gain (i.e., the difference SNR) at an input power of about -30 dB peaks at about $G = 18$ dB, which is even higher than the gain of 12 dB, as estimated with (4) for $a/b = 1/0.25 = 4$. An adaptive sigma–delta modulator requires a multi-bit D/A-converter in the feedback loop, since the feedback signal $s(n) + by_0(n)$ is a multilevel signal. The requirements with respect to the linearity of this D/A converter must meet the requirements of an enhanced SNR. This is due to the fact that a nonideal D/A converter can be regarded as an ideal converter plus a noise source, and in the present application, the transfer function of this additional noise source is $-\mathrm{NTF}(z) = -z^{-1}$. Thus, this noise (multiplied by -1) is directly added to the input signal and enhances the noise energy in the base band. Fig. 7 shows the SNR of an adaptive sigma–delta modulator with a nonideal D/A converter, where the contribution of the dc-offset error is omitted. The nonideal D/A converter has a linearity equal to an 8-bit D/A converter with a maximum deviation of $\pm 1/2\mathrm{LSB}$ from the ideal levels, i.e., for $a = 1$, the maximum deviation of the 17 levels from the ideal values is $\pm 1/255$. The error is assumed to be uniformly distributed. As demonstrated, the reduction of SNR increases

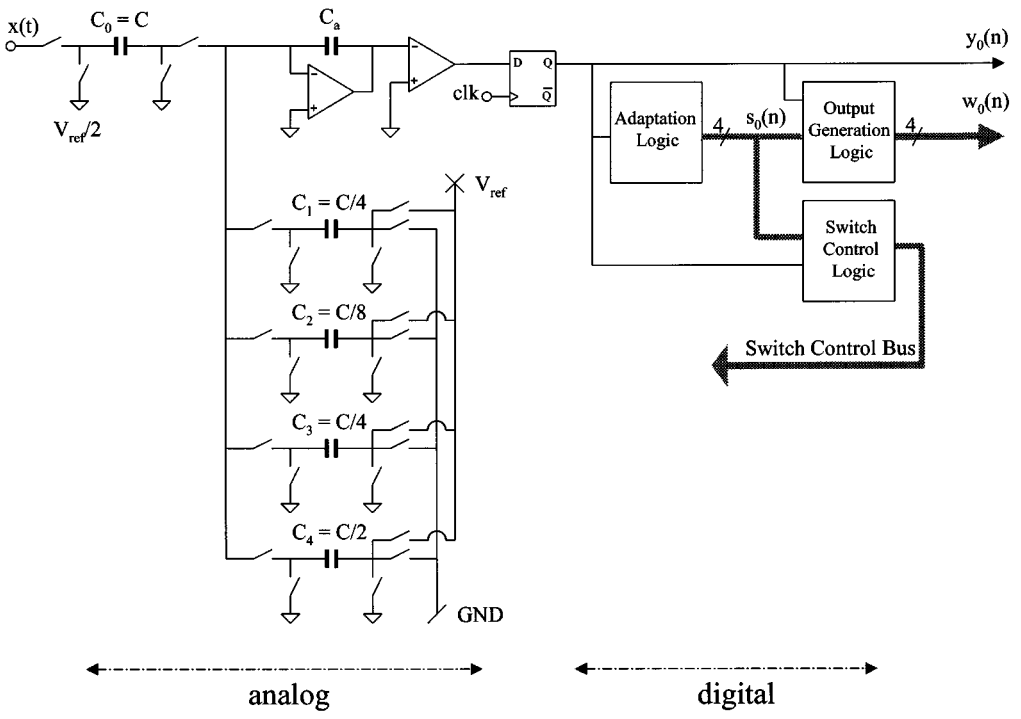

Fig. 8. Switched-capacitor implementation of an adaptive sigma–delta modulator of first order with $a = 1, b = 0.25$, and $q = 0.5$.

with increasing input power level, and the mean SNR reduction for input levels between -25 and -9.45 dB is smaller than 2 dB.

Input signals as in Fig. 7 have been applied to a multi-bit sigma–delta modulator of first order, involving a multi-bit quantizer and a multi-bit D/A converter with a quantization step size Δ =0.5, and a sampling rate $1/T = 1$ MHz. The quantizer shows a "mid-riser" type of transfer function, i.e., possible quantization levels are $\pm 1/2\Delta, \pm 3/2\Delta, \ldots$. The amount of quantization noise power generated by this type of multi-bit sigma–delta modulator should be comparable to that of an adaptive sigma–delta modulator of first order with b =0.25. An ideal multi-bit sigma–delta modulator of first order, and one with a nonideal D/A converter have been examined. As above, the nonideal D/A converter has a linearity equal to an 8-bit D/A converter within the range $[-1, +1]$, where the maximum deviation from the ideal levels is $\pm$(1/2) LSB. The results obtained are very close to curves (a) and (d) for the ideal and the nonideal modulators, respectively (consequently, these results are not shown again). The representation of an input power range as in Fig. 7 requires a 3-bit digital output sequence at 1 MHz.

VII. Circuit Example

A practical example for an adaptive sigma–delta modulator of first order is shown in Fig. 8. An adaptation algorithm as in Table I is assumed, and the system parameters are set to $a = 1, b = 0.25$, and $q = 0.5$. Here, the focus is on the analog part which is realized as a standard switched-capacitor design. The generation of the overall feedback signal $s(n) + by_0(n)$ requires a D/A converter with 17 equidistant levels $\pm 1, \pm 0.875, \pm 0.75, \pm 0.625, \pm 0.5, \pm 0.375, \pm 0.25, \pm 0.125$, and 0. Assuming a reference voltage $V_{\rm ref}$, level 0 is associated with voltage $V_{\rm ref}/2$, levels $\pm$0.125 with voltages $V_{\rm ref}/2(1\pm$0.125, etc. Here, four capacitors $C_1 = C/4, C_2 = C/8, C_3 = C/4$, and $C_4 = C/2$ are used which are fractions of the input capacitor $C_0 = C$. The 4-bit signal $s_0(n)$ is derived numerically from signal $y_0(n)$ in block "Adaptation Logic". The 4-bit digital output sequence $w_0(n)$ is calculated in block "Output Generation Logic" by adding sequences $s_0(n-1)$ and $y_0(n)$*0.25. The switching control signals for charging/discharging the capacitors are derived from $s_0(n)$ and $y_0(n)$ in block "Switch Control Logic." As in Fig. 3, there is a clear distinction between analog and digital signal processing stages.

In a standard sigma–delta modulator of first order with the same input range $a = 1$, the feedback signal would be $y_a(n)$, and the generation from $y_0(n)$ would require only one capacitor $C_1 = C$. Thus, the additional hardware costs for the adaptive modulator as compared to the standard modulator are three capacitors (plus the associated analog switches), and the logic stages. There are no additional demands on the specifications of the operational amplifier and the comparator, e.g., with respect to slew rate or open loop gain. However, as mentioned above, the precision of the prediction signal has to fulfil special requirements. The realization of 17 quantization levels with a maximum level error of $\pm$(1/255) (corresponding to an 8-bit DAC with maximum error of $\pm$(1/2 LSB) should be feasible with standard switched-capacitor technology, and thus only a slight reduction of the SNR has to be expected (cf. Fig. 7). The power consumption due to the feedback capacitors is even lower in the adaptive than in the nonadaptive modulator, since the power of the overall feedback signal $s(n) + y_b(n)$ is smaller than the power of signal $y_a(n)$.

VIII. Similarities Between Adaptive Sigma–Delta and Adaptive Delta Modulation

An adaptive sigma–delta modulator as presented here can be regarded as a combination of a sigma–delta modulator and an adaptive delta modulator, and thus, it has some features typical for adaptive delta modulation. Compared to linear delta modulation, adaptive delta modulation is characterized by its employment of variable (adaptive) step sizes instead of a fixed step size. The instantaneous step size in an adaptive delta modulator is determined by multiplying a particular step size by an adaptive multiplier, which is derived from previous codewords. In practice, this approach results in a significant reduction of the slope overload probability, and thus in an improved SNR. Typical examples of adaptive delta modulators can be found, e.g., in [4] and [5].

There is a general problem involved in adaptive delta modulation applications concerning error accumulation due to mismatch of step size multipliers in the coder unit (feedback loop) and in the decoder. Ideally, signal reconstruction can unambiguously be achieved by means of the digital code only (except for its dc component). Thus, the prediction signal (coder) and a signal constructed from the code only (decoder) should differ only in their dc-level. However, in practical implementations, since the step size multipliers in the coder differ slightly from the multipliers in the decoder due to hardware imperfections, the error between the prediction signal and a reconstructed signal keeps increasing (error accumulation). To reduce this effect, "leaky" integrators (removing the pole at frequency zero) are employed in the decoder in practical applications. However, as shown in [5] in more detail, error accumulation can be completely avoided if the number of possible values of the prediction signal is reduced to a finite set. This allows a numerical computation of the prediction signal, and the conversion to a physical signal can be achieved by means of a D/A converter.

Looking at the adaptive sigma–delta modulator Fig. 2, the adaptation stage corresponds to the integrator (accumulator) of an adaptive delta modulator. With an adaptation algorithm as in Table I, the step size then is bq, and the (adaptive) step size multipliers are $+1$, 0, and -1. Following the considerations in [5], here the possible values of the prediction signal $s(n)$ are limited to a finite set, and the generation from its digital representation $s_0(n)$ is achieved by means a D/A converter. Therefore, this implementation avoids any problems encountered with error accumulation.

IX. Conclusion

The properties of adaptive sigma–delta modulation be summarized as follows.

1) The performance of sigma–delta modulators with respect to SNR can be significantly improved at the cost of a moderate slew-rate limitation of the input signal. This improvement is made possible by the ability of standard sigma–delta modulators to process discontinuous input signals, i.e., the digital high-rate output signal contains the information of discontinuous input signals. This capability is usually not exploited, since in standard applications, signal reconstruction from the high-rate output requires nonlinear decoding techniques. However, the two-level output $y_0(n)$ of the sigma–delta modulator within an adaptive sigma–delta modulator loop is further processed to a multilevel system output $w_0(n)$, which allows for standard linear decoding algorithms.
2) The additional hardware of an adaptive modulator as compared to a standard (nonadaptive) modulator comprises logical gates, capacitors and switches. In particular, the quantization stage does not have to be changed, i.e., the resolution of the quantizer remains the same. However, the feedback signal is a multilevel sequence, and thus a multi-bit D/A converter in the feedback loop with particular demands on the linearity is required. The properties of analog components such as operational amplifiers and comparators can be left unchanged.
3) The power consumption of an adaptive modulator compared to a nonadaptive modulator remains almost the same. A slight increase due to additional logical gates is offset by a slight decrease of power consumption in the analog part.
4) Except for the dc value of $s_0(n)$, the entire digital information characterizing the input signal $x(n)$ is contained in the two-level sequence $y_0(n)$. However, the actual signal $x(n)$ (delayed by one sampling period) as a temporal waveform is contained in the multilevel sequence $w_0(n)$, which has to be reconstructed from $y_0(n)$. If the initial value of $s_0(n)$ is known, the digital multilevel sequence $w_0(n)$ can be reconstructed without error directly from $y_0(n)$. With an unknown initial value of $s_0(n)$, an initial dc error may occur. However, this error is reduced each time the sequence $s_0(n)$ reaches particular (numerical) limits which are defined by the adaptation algorithm.
5) If an adaptive sigma–delta modulator is compared to a multi-bit sigma–delta modulator with similar SNR performance at the same sampling rate, two advantages become obvious. First, the multi-bit quantizer can be omitted. Although there are only modest requirements with respect to the accuracy of multi-bit A/D converters in sigma–delta applications (because of differentiation of the generated noise), the implementation requires several comparators which contribute both to chip size and power consumption. The second advantage concerns the feature addressed in (4), i.e., the information characterizing the input signal is contained in the single-bit sequence $y_0(n)$ in the adaptive sigma–delta modulator, instead of a multi-bit sequence as for the multi-bit sigma–delta modulator. According to information theory, this means a significant enhancement of information per bit. In applications where the high-rate digital sigma–delta information has to be stored or transmitted before further processing, this feature can be extremely advantageous with respect to memory size or bandwidth of the transmission channel.
6) The approach presented is not restricted to sigma–delta modulators of first order. With higher order modulators, stability problems may occur. However, these problems

have successfully been solved for an adaptive sigma–delta modulator of second order, which will be published in the near future.

REFERENCES

[1] J. C. Candy and G. C. Temes, Eds., *Oversampling Delta-Sigma Data Converters*. Piscataway, NJ: IEEE Press, 1992, ISBN 0-87 942-285-8.

[2] S. R. Northworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters*. Piscataway, NJ: IEEE Press, 1997, ISBN 0-7803-1045-4.

[3] N. T. Thao and M. Vetterli, "Deterministic analysis of oversampled A/D conversion and decoding improvement based on consistent estimates," *IEEE Trans. Signal Processing*, vol. 42, pp. 519–531, Mar. 1994.

[4] N. S. Jayant, "Adaptive delta modulation with a one-bit memory," *Bell System Tech. J.*, pp. 321–342, Mar. 1970.

[5] C. M. Zierhofer, "Numerical adaptive delta modulation—A technique for digital signal representation in ASIC applications," in *Proc. IEEE Melecon'91*, vol. 1, Ljubljana, Yugoslavia, May 1991, pp. 789–792.

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