

# Wash Machine Controller

## 1 Objectives

- Understand functionalities and operation of a simple wash machine.
- Appreciate the importance of timers and single-bit I/O for microcontroller design
- Decide which features are implemented by the controller and which features are delegated to digital logic.
- Transform a controller word description or specifications into a finite-state machine (FSM) transition diagram.
- Write VHDL code for the FSM and synthesize the code on FPGA using the Xilinx ISE tools.
- Study the synthesis performance parameters (delay, FPGA resources, power consumption, equivalent gate count).

## 2 Introduction

The controller to be designed controls the actions of the wash machine. A user typically selects the amount of wash load (light, normal, or heavy). Based on that, the controller controls the amount of water to fill the drum. Some wash machines wash clothes by agitation where the drum spins clockwise and counterclockwise once every second or so. This is accomplished by mechanical gearing. Newer machines change the direction of rotation of the drum every minute or so accomplished by electrically changing the direction of the drum motor. We chose the former option for simplicity and assumed that the drum agitation is accomplished through a gearing mechanism that is engaged electrically. Typically, the water temperature is selected by the user and the controller opens or shuts the cold and hot water valves by two control signals. Again for simplicity we assumed that the controller issues a single water shut or open signal. The user manually controls the water temperature by opening or closing the water valves feeding a water mixer.

Figure 1 shows the circuit symbol, or icon, of the wash machine controller. Table 1 identifies the I/O signals of the controller and their functionality.

### 2.1 Wash Machine Controller Specifications

The functionality of the wash machine is implicitly included in the wash machine controller which has the following functionalities:

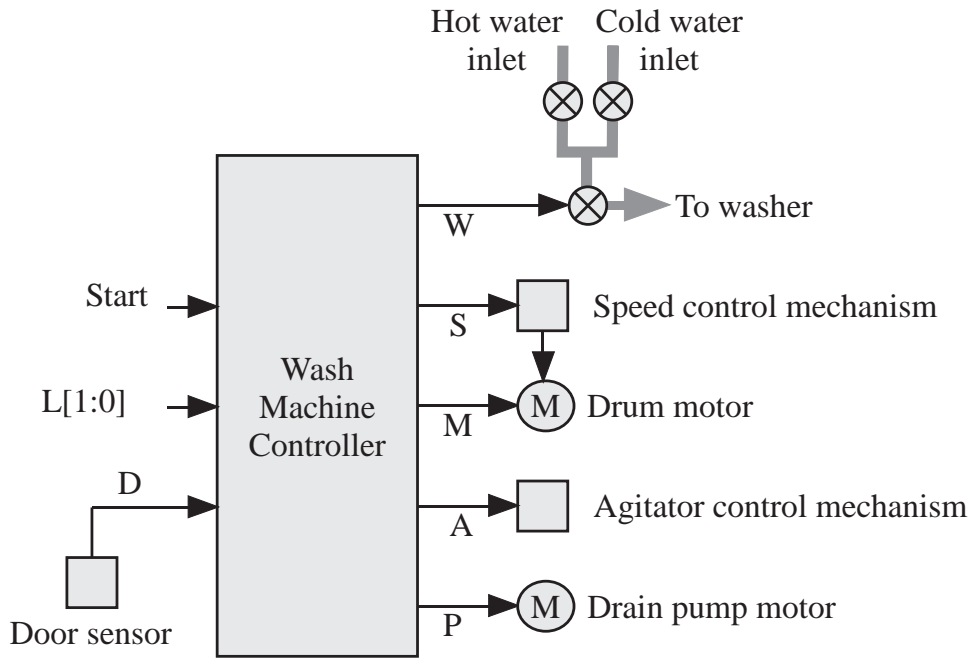


Figure 1: Icon for the wash machine controller indicating main input and output lines.

Table 1: Alphabetical listing of input and output signals for the wash machine controller. All signals are active high.

<i>A</i>	Out	Active high	Activate the agitator mechanism								
<i>D</i>	In	Active high	Machine door (lid) is open								
<i>L(1 : 0)</i>	In	Active high	Load (amount of clothes to be washed)								
			<table border="1" style="width: 100%;"> <tbody> <tr> <td>00</td> <td>1/3 load</td> </tr> <tr> <td>01</td> <td>half load</td> </tr> <tr> <td>10</td> <td>full load</td> </tr> <tr> <td>11</td> <td>not used (don't care)</td> </tr> </tbody> </table>	00	1/3 load	01	half load	10	full load	11	not used (don't care)
00	1/3 load										
01	half load										
10	full load										
11	not used (don't care)										
<i>M</i>	Out	Active high	Enable motor								
<i>P</i>	Out	Active high	Activate the pump mechanism to drain the water								
<i>S</i>	Out	Active high	Activate motor speed control mechanism								
<i>Start</i>	In	Active high	Start the washer								
<i>W</i>	Out	Active high	Activate water source solenoid								

1. The wash machine has the following consecutive states: *idle, fill, wash, drain, fill, rinse, drain, spin*
2. There is one control line to the washer water feed. Choice of hot or cold water wash is done manually by the user for simplicity.
3. There are two drum rotation speeds: low speed for wash cycle and high speed for the spin cycle. Speed control is accomplished through an electrically controlled mechanism.
4. During the wash cycle, the drum direction of rotation is controlled through the agitator mechanism.
5. During the spin cycle the controller stops the drum motor if the door is sensed open.

### 3 Wash Machine Controller Detail

Figure 2 shows the main components of the wash machine controller. The controller is

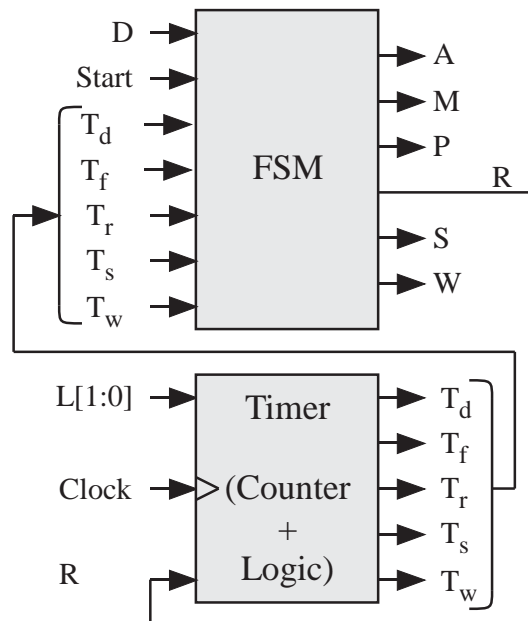


Figure 2: The main components of the wash machine controller.

composed of two blocks: a finite-state machine (FSM) block and a timer block. The FSM block receives some signals from the user, from the timer, and from other hardware parts such as the door sensor. FSM block outputs control the timer block and other hardware components of the wash machine.

Table 2 identifies the FSM input and output signals and their functionality. The timer block generates the correct time periods required for each cycle after it has been reset. The timer block itself is composed of an up-counter and combinational logic to give the correct time

Table 2: Alphabetical listing of input and output signals for the FSM. All signals are active high.

$A$	Out	Activate the agitator mechanism
$D$	In	Machine door (lid) is open
$M$	Out	Enable motor
$P$	Out	Activate the pump mechanism to drain the water
$R$	Out	Timer reset
$S$	Out	Activate motor speed control mechanism
$Start$	In	Start wash machine
$T_d$	In	Drain time required to empty the machine tub
$T_f$	In	Fill time required to fill the machine tub
$T_r$	In	Rinse time
$T_s$	In	Spin time
$T_w$	In	Wash time
$W$	Out	Activate water source solenoid

signals once certain count values have been achieved. Of course the time values will be determined by the clock frequency being used in the system. This, however, is beyond the purpose of this project.

## 4 Pitfalls of Asynchronous Signals

The FSM resets the counter each time it starts a new phase (e.g. wash, drain, etc.) in response to the timer outputs. However, for the combination of a Mealy machine and an asynchronous counter reset creates problems. Issuing a reset signal immediately resets the timer before the Mealy machine had a chance to change states. The end result is that the Mealy FSM will be stuck in its present state.

This is best illustrated with the detailed timing diagram in Figure 3. The present state (PS) of the washer is *Fill* where the drum is being filled with water until the timer asserts the signal  $T_f$ . When this condition happens, the FSM must do two actions:

1. Move to the next state *Wash*
2. Rest the timer
3. Wash clothes until the wash time period  $T_w$  is asserted

We see from the figure that when the reset signal  $R$  is asserted, the timer immediately zeros its count and all its output signals are zeroed. This includes the signal  $T_f$ .

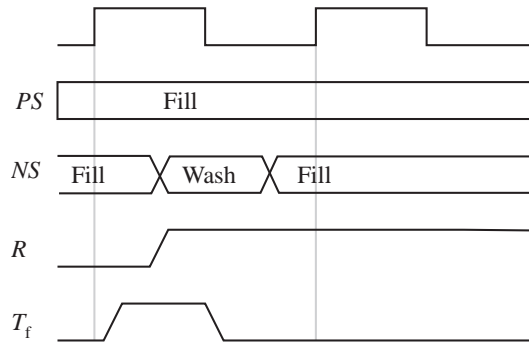


Figure 3: A timing problem for a Mealy FSM communicating with an asynchronous timer.

Now we have a problem: The present state of the wash machine is in the fill cycle *Fill* and the signal  $T_f$  is zero. Hence the next state switches back to *Fill*. The machine will remain stuck in this state and overflow the drum with water!

The main problem is that signals like  $T_f$  were allowed to change values more than once within the same clock period. This is unacceptable especially for a Mealy FSM. The correct sequence should have been:

$$Fill \rightarrow Wash$$

but now our sequence will be

$$Fill \rightarrow Fill$$

And the machine will never get past the fill phase.

One obvious solution to this problem is to use synchronous reset for the counter. Another solution is to add an extra state after each operation phase of the washer so that checking the time signal and resetting the counter are accomplished in two different states.

## 5 Pre-Lab Report

For your prelab report, you are required to do the following.

1. Design the Mealy state diagram for the wash machine whose specifications are listed in Section 2.1. Use the diagrams and specifications of the machine as explained in this project.
2. In a table, list the states of your state transition diagram and comment on their meaning.

- Design the timer in Fig. 2 by using a counter similar to the one you did in the tutorial but having the timing specs in Table 3.
- In newer wash machines the door is locked as long as the machine is in operation. Draw the Mealy state diagram that satisfies this requirement.
- Suggest a solution for the FSM timing problem discussed in relation to Fig. 3.

Table 3: Approximate timing specs for the washer timer.

Time Signal	Approximate Duration (s)	Comment
$T_d$	1	
$T_f$	2	
$T_r$	4	
$T_s$	8	
$T_w$	2, 4, 8	For L=00, 01, 10, respectively

## 6 Project Requirements

In this project you are required to design, model, and simulate a wash machine controller.

- Use a two- or a three-process FSM VHDL coding style for the FSM block. Make sure you have adequate and clear comments in your code.
- Write a testbench or show waveforms to verify the operation of the FSM.
- Write a VHDL code for the timer you have designed.
- Write a testbench to verify the operation of the timer.
- Synthesize the controller on FPGA and study the performance parameters (delay, FPGA resources, power consumption, equivalent gate count).
- Use an external clock with 1 Hz frequency to drive the timer.

## 7 Lab Report

Your lab report should include the following.

- Refer to the lab report grading scheme for items that must be present in your lab report. The grading scheme can be accessed on-line at:  
[http://www.ece.uvic.ca/~fayez/courses/ceng441/lab/lab\\_grading\\_scheme.html](http://www.ece.uvic.ca/~fayez/courses/ceng441/lab/lab_grading_scheme.html)

2. Draw a neat Mealy-style state-diagram with all the states used and the transitions clearly labeled. Write a brief note about what is being done in each state.