

	Date	Topics	Ass	Lab	Done
1	3 May	Course information, VLSI Overview (pp. 1–5)			■
2	4 May	VLSI Overview (pp. 6–16)			■
3	6 May	Class postponed			■
4	10 May	VLSI Overview (pp. 16–19)			■
5	11 May	VLSI Overview (pp.19–38)			■
6	13 May	VHDL language (pp. 1–12)	Ass 1		■
7	17 May	VHDL language (pp. 12–22)			■
8	18 May	VHDL language (pp. 22–33)			■
9	20 May	VHDL language (pp. 33-48)			■
10	24 May	VHDL language (pp. 48–57), VHDL language basics (pp. 1–12)			■
11	25 May	VHDL language basics (pp. 12–20)		Lab 1, LK03 24 May	■
12	27 May	Extra makeup class, VHDL language basics (pp. 20–28)			■
13	31 May	VHDL language basics (pp. 28–33)		Lab 1, LK02 30 May	■
14	1 Jun	VHDL language basics (pp. 33–51)			■
15	3 Jun	VHDL language basics (pp. 52–68)	Ass 2		■
16	7 Jun	VHDL combinational modeling (pp. 1–12)			■
17	8 Jun	VHDL combinational modeling (pp. 12–43)		Lab 2, LK03 7 Jun	■
18	10 Jun	VHDL combinational modeling	Ass 3		■
19	14 Jun	VHDL sequential modeling (pp. 1–12)		Lab 2, LK02 13 Jun	■
20	15 Jun	VHDL sequential modeling (pp. 12–20)			■
21	17 Jun	In class midterm			
22	21 Jun	VHDL sequential modeling (pp. 20–37)			■
23	22 Jun	VHDL sequential modeling (pp. 37-44)	Ass 4	Lab 3, LK03 21 Jun	■
24	24 Jun	VHDL sequential modeling (pp. 45–62)			■
25	28 Jun	VHDL synthesis (pp. 1–20)		Lab 3, LK02 4 Jul	■
26	29 Jun	VHDL synthesis (pp. 21–33)			■
27	5 Jul	VHDL synthesis (pp. 33–58), VLSI Methodology (pp. 1–9)			■
28	6 Jul	VLSI Methodology (pp. 9–18), ASIC's (pp. 1–7)		Lab 4, LK03 12 Jul	■
29	8 Jul	ASIC's (pp. 7–36)			
30	12 Jul	Design for testability (pp. 1–12)		Lab 4, LK02 18 Jul	■

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	Date	Topics	Ass	Lab	Done
31	13 Jul	Design for testability (pp. 13-24)			■
32	15 Jul	Design for testability (pp. 25-29)			■
33	19 Jul	Design for testability (pp. 29-39)	Ass 5		■
34	20 Jul	Design for testability (pp. 40-46)			■
35	22 Jul	Design for testability (pp. 47-57)			■
36	26 Jul	Design for testability (pp. 58-62)			■
37	27 Jul	Design for testability (pp. 63-77)			■
38	29 Jul	Design for testability (pp. 78-86) & Review			■