Traffic-light controller

1 Objectives

- Transform a controller word description into a finite-state machine (FSM) transition diagram.
- Decide which features are implemented by FSM and which features are delegated to digital logic.
- Implement a simple finite-state machine using VHDL.
- Simulate the operation of the FSM.

2 Introduction

The controller to be designed controls the traffic lights of a busy highway (HWY) intersecting a side road (SRD) that has relatively lighter traffic load. Figure 1 shows the location of the traffic lights. Sensors at the intersection detect the presence of cars on the highway and side road. The figures implies that both the highway and side roads offer single lanes for traffic in each direction.

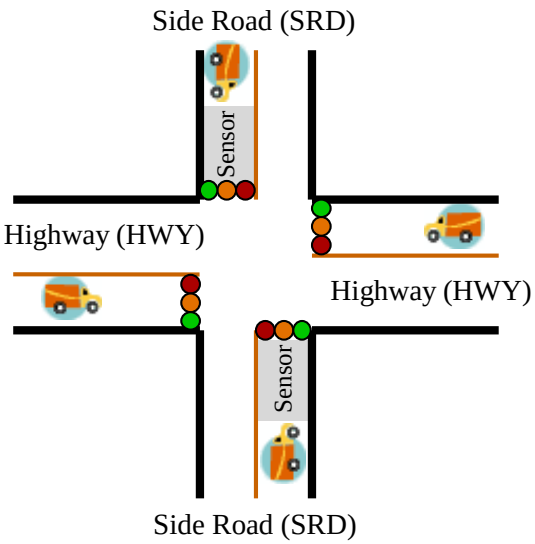

Figure 1: Highway and a side road intersection

2.1 Finite-state machine specifications

The traffic light controller works in the following way.

1. The lights controller makes use of car sensors at the intersection of the side road with the highway, to sense presence of cars.
2. The lights controller makes use of three timers: a 60 seconds timer (T_{60}), a 30 seconds timer (T_{30}), and a 10 seconds timer (T_{10}). Once a *trigger* signal is applied to a timer, the timer output is zero and becomes 1 after the programmed time period. For example, upon reset, the T_{30} timer output is '0' and will become '1' after 30 s have elapsed and stays '1' until reset by the controller.
3. Pedestrians can use the intersection by pressing buttons and debouncing switches. Pedestrians will need to cross the highway only since crossing the side road is assured most of the time.
4. HWY lights remain green as long as there are no cars triggering the SRD sensors.
5. When HWY lights have been green for a minimum of 60 seconds, a car on SRD may cause HWY lights to cycle through yellow to red states.
6. Meanwhile, SRD lights will turn green and remain green for a minimum of 30 seconds. further application of SRD sensors beyond the 30 seconds will enable SRD to remain green for a maximum of 60 seconds.
7. SRD lights will cycle through yellow and red states and HWY lights will then turn green.
8. The lights stay yellow for 10 seconds.
9. Each traffic post has three lights GREEN, YELLOW and RED.
10. In the default state, HWY lights show GREEN and SRD lights show RED.

2.2 Traffic light FSM Interface signals

The FSM to the traffic lights controller has the input signals shown in Table 1

Table 1: Input signals to the traffic lights controller.

Signal	Comment
clk	System clock
$reset$	System asynchronous reset
car	A car wants to cross HWY
$pedestrian$	A pedestrian wants to cross HWY
T_{60}	Sixty-second timer signal
T_{30}	Thirty-second timer signal
T_{10}	Ten-second timer signal

The controller has the output signals shown in Table 2

Table 2: Output signals from the traffic lights controller.

Signal	Comment
trigger	Reset all timers
r_h	HWY red light enable
y_h	HWY yellow light enable
g_h	HWY green light enable
r_s	SRD red light enable
y_s	SRD yellow light enable
g_s	SRD green light enable

3 Pre-Lab Report

1. Draw the traffic-light controller as an icon indicating the I/O control signals.
2. Draw a block diagram for the traffic lights controller indicating clearly the main system blocks and interface signals.
3. Draw a Mealy-style state diagram which covers all legal state transitions of the machine.

4 Project Requirements

In this project you are required to design, model and simulate the finite-state machine for the traffic light controller.

1. Use a two- or three-process FSM VHDL coding style. Make sure you have adequate and clear comments in your code.
2. Write a testbench to verify the operation of the FSM. The testbench should try different scenarios for cars or pedestrians attempting to cross HWY or SRD at different traffic loads.
3. Simulate the behavior of the FSM using the testbench you developed.

5 Lab Report

1. Refer to the lab report grading scheme for items that must be present in your report.
2. Provide a table indicating all the input and output signals of the traffic lights controller and the traffic lights FSM.
3. Draw a neat Mealy-style state-diagram with all the states used and the transitions clearly labeled. Write a brief note about what is being done in each state.