# An Active Dual-Gate GaAs FET Mixer for 800 MHz Low Current Consumption Mountain Top Repeaters

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#### **Abstract**

A dual gate GaAs FET mixer for use in a low noise receiver front end in the frequency range of 800 to 900 MHz is presented. The circuit is made on a low cost 0.062 inch fiber glass substrate with  $\varepsilon_{\rm T}$  of 4.2 and is designed with inexpensive common surface mount components. The prototype has a third order intercept of 9 dBm, with respect to the output level, a minimum gain of 13.9 dB, and a sensitivity of -119.3 dBm when driven with an LO power of -2 dBm and with a drain current of 3.0 mA. For improved performance and for easier integration into the receiver, the output impedance is set at 1500  $\Omega$ .

#### Introduction

This paper describes the development and electrical performance of a receiver front end for use in mountain top repeater communication systems. Using a dual gate Gallium Arsenide Field Effect Transistor (DGFET) mixer, cost, size as well as current consumption, intermodulation distortion and LO drive level could be improved significantly. For comparison, a passive front end using a low noise amplifier and passive diode mixer only has an average intermodulation distortion, because cascading several circuits reduces the overall intercept point when several circuits are cascaded. The intercept point can be calculated using Nortons' equation [1]. For example, assuming a low power amplifier with a third order intercept of 14 dBm and a passive diode mixer with a third order intercept of 1 dBm (with respect to the output) the overall figure would be 0 dBm.

Although this is sufficient for most system requirements, the increased use of the high UHF band, (i.e. cellular telephones), requires an additional 10 dB margin for the intercept point. Furthermore, a typical a low noise amplifier in front of a passive diode mixer and a local oscillator drive amplifier would have together a current consumption of 10-13 mA.

To reduce this high current consumption and at the same time eliminate the need for the amplifiers in the RF and LO chain, an active DGFET mixer with a higher intercept point is an attractive solution. In addition, increasing the intercept point by 9 to 14 dB gives the margin needed for highly congested areas and improves performance, when the receiver is in close proximity to high power transmitters. An active mixer can have a gain of 8 to 13 dB and only requires a low local oscillator drive of -5 to 3 dBm. The LNA and local oscillator amplifier are therefore no longer required because the DGFET mixer provides the extra gain. With the two circuits removed (LNA and local oscillator amplifier), the current consumption is reduced by 10 mA, the component count is reduced by half, and the space requirements are half to a third that of the passive circuit. This leads to increased reliability and improves the MTBF (mean time before failure). The reduction in power consumption and an increase in the MTBF prolongs the service

# Mixer Design

The mixer design for this application mainly follows design criteria given in [2]. The basic steps are described below. For details, the reader is referred to [2].

When using a dual gate FET (DGFET) as a mixer, the gates are used as the inputs for the local oscillator power and the signal. S parameter and noise matching data are only provided for gate 1 so for simplicity it is used for the signal and gate 2 is used for the local oscillator. The connections to the DGFET are shown in Figure 1.

Figure 2 shows a graph of the transfer characteristics of a typical DGFET. The indicated area on the transfer characteristics is called the low noise mode [3]. However, for maximum conversion gain the gate bias should be near pinch off [2]. With both gates near pinch off, the optimum noise figure cannot be obtained, and adjustments to the gate voltages must be made empirically for the desired performance. As the bias is adjusted to improve the noise figure, the maximum gain is reduced.

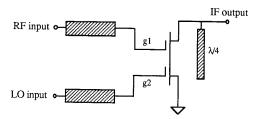


Figure 1, DGFET connections.

The DGFET has gain at the RF, LO and IF frequencies. To eliminate noise and interference caused by amplifying the IF, RF and LO frequencies, it is important to short the gates at the IF frequency, and to short the drain at the RF and LO frequencies and at their harmonics. To make a short at the drain, it is recommended [2] to use a low pass filter instead of a quarter wavelength open circuit stub, e.g. [3,4], because it provides a short to the even harmonics where as the open stub does not. Another possible shorting technique suggested in [3] for MMIC applications is to use a shunt capacitor resonant at the LO frequency.

When a DGFET is biased in the low noise mode, several elements have nonlinear behavior. Figure 3 shows the equivalent circuit of a DGFET. The nonlinear elements are indicated with solid bars. The mixing takes place in FET 1 with FET 2 acting mainly as an IF postamplifier. There are four nonlinear elements in FET 1,

transconductance  $\mathbf{g}_{\mathbf{m}}$  , channel resistance  $\mathbf{R}_{\mathbf{d}}$  , input capacitance  $\mathbf{C}_{\mathbf{g}\mathbf{s}}$  , and gate drain capacitance  $C_{gd}$ . Only  $g_m$  and  $R_d$  significantly contribute to the mixing in FET 1. The mixing due to  $C_{gs}$  and  $C_{gd}$  is considered negligible. To produce maximum mixing, the DGFET must be biased close to pinch off (low gate voltages), so the excursions of transconductance and drain current are maximized by the applied local oscillator signal at the second gate.

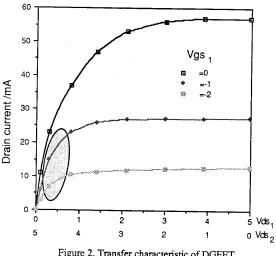


Figure 2, Transfer characteristic of DGFET.

To design the matching networks, the S parameters are used to calculate the input reflection coefficient[2].

$$\Gamma_{\text{in}} = S_{11} - \left[ S_{21} S_{12} / (1 + S_{22}) \right]$$
 (1)

This equation is valid only if the optimum short circuit embedding impedances are applied as described above. The output impedance for most FETs at low frequency is very high, in the order of 1000 ohms, with a very small reactive component. So matching at the IF is difficult and depends on the LO drive level and bias conditions. Shunt resistive loads are used in [2,3] to swamp out the drain source impedance but at the expense of the gain. To maximize the gain and to make matching to the IF filter circuit easier, an IF impedance of 1500  $\Omega$  was selected. Since the mixing occurs in the first FET [3], and the second FET acts mainly as an IF post amplifier, the gain and LO power are calculated using the equations for a single gate FET. The gain can be estimated by (2) using element values from the small signal linear time varying FET equivalent circuit in Figure 3 [3].

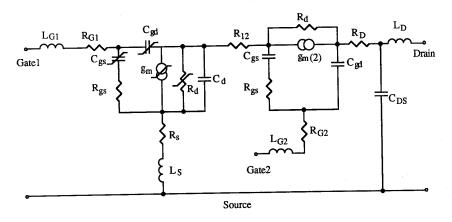


Figure 3, Equivalent Circuit of DGFET.

$$G_t(\omega_0, \omega_1) = g_{mmax}^2 Q_{in}^2 (R_s + R_i + R_g) \operatorname{Re} \{ Z_L(\omega_0) \} / 16$$
 (2)

where

$$Q_{in} = 1/j\omega_1 C_{gs0} (R_s + R_i + R_g)$$
 (3)

 $\begin{array}{lll} R_i & - & \text{Intrinsic channel resistance} \\ R_s & - & \text{parasitic source resistance} \\ R_g & - & \text{parasitic gate resistance} \\ \omega_1 & - & \text{RF center frequency} \\ \omega_0 & - & \text{IF center frequency} \\ \end{array}$ 

g<sub>mmax</sub> - maximum dc transconductance

The equations are relatively close estimations as long as the optimum short circuit embedding impedances are present and the proper gate bias is applied. Assuming the same conditions, the required LO power can be estimated[2].

$$P_{LO} = (V_{max} - V_t)^2 / 2Q_{inLO}^2 (R_s + R_i + R_g)$$
 (4)

V<sub>max</sub> - voltage for maximum transconductance. V. - the turn on voltage.

The  $Q_{inLO}$  is calculated using (3) but at the LO frequency and with the second gate capacitance. The calculated LO power will produce maximum gain but for the best noise performance, the power requirements are typically 2-4 dB lower [2].

#### Results

A mixer for 851 - 866 MHz RF and with a fixed IF of 21.4 MHz was designed using a  $0.5~\mu m$  gate length DGFET with a  $800~\mu m$  gate width. The S parameter data for the transistor was obtained from the manufacturer as well as the optimum conjugate reflection coefficients for best noise figure. However, the manufacturers' data

was valid only at the specified bias voltages, and no S parameter data were given for the second gate. The parasitic parameters for the device were estimated as  $R_s = 2 \Omega$ ,  $R_i = 1.6 \Omega$ ,  $R_g = 1.5 \Omega$ ,  $C_{g1s0}$ =1.5 pF,  $C_{g2d0}$ =5.0 pF and  $g_{mmax}$ = 12 mS. S parameter measurements for the transistor indicated that the IF impedance would be approximately 1700  $\Omega$  with some parallel capacitive reactance. Using equation (1), the reflection coefficient approaches  $S_{11}\,$  at the 800 to 900 MHz range, so the manufacturers data for best noise match was used. Touchstone™ software was used to verify the matching network for best noise performance. The matching circuit consists of a simple two element network of a series capacitance and a shunt inductance. The short at the gates, for removal of IF noise, is provided by using short circuit stubs in the matching network. The stubs act as inductors at the RF and LO frequencies and as virtual shorts at the IF. A quarter wavelength open circuit stub at the drain provides the required short at the LO frequency. The calculated conversion gain using equation (2) is 16 dB. The calculated LO power for maximum gain is -3.5 dBm. The IF is matched to 1500  $\Omega$ by a shunt inductance and a series capacitance. A chip inductor was used at the drain for the required shunt inductance.

The measured gain of the mixer is shown in Figure 4. The sensitivity is -119.3 dBm at an LO power of -2 dBm. However, the sensitivity deteriorates when the LO power is increased as predicted in [2]. The quarter wavelength open circuit stub which was added to short the LO, increases the LO to IF isolation by 24 dB. The mixer occupies a surface area of 9.3 cm<sup>2</sup> and consumes 3.0 mA of current.

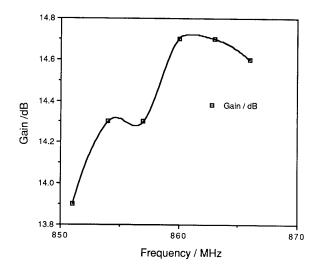


Figure 4, Gain of DGFET Mixer with -2 dBm LO power.

The deviations between estimates and measurements are  $+1.6~\mathrm{dB}$  for the gain and  $-1.5~\mathrm{dB}$  for the LO power. These differences are attributed to the estimated  $g_{mmax}$  and the reflection losses of the LO and RF ports. The LO power also affects the predicted gain. The short circuit embedding impedance, the quarter wavelength stub, is very frequency selective and does not present a short circuit at the even harmonics of the LO frequency to the drain which is assumed by the gain equation (2). Also since a packaged transistor is used, the parasitic parameters may not be accurate.

### Conclusions

The presented DGFET mixer has improved electrical performance over an existing circuit involving a passive diode mixer. A minimum conversion gain of 13.9 dB, a sensitivity of -119.3 dBm, and a third order intercept of 9 dBm with a LO power of -2 dBm and a drain current of 3 mA are achieved. The reduction of LO power from 7 dBm, the required power for a diode mixer, to -5 to 0 dBm reduces the current consumption of the LO circuit and reduces the area of the receiver front end.

## References

- [1] S.J. Erst, <u>Receiving Systems Design</u>. Dedham, MA.:Artech House, 1984.
- [2] Stephen A Maas, <u>Microwave Mixers</u>. Dedham, MA.: Artech House, 1986.
- [3] C. Tsironis, R. Meierer and R Stahlmann, "Dual-Gate MESFET Mixers," IEEE Trans. <u>Microwave Theory Tech.</u>, MTT-32, 1984, pp.248-255.
- [4] T. Sugiura, K. Honjo and T. Tsuji, "12-GHz-Band GaAs Dual-Gate MESFET Monolithic Mixers," IEEE Trans. <u>Microwave Theory Tech.</u>, MTT-33, 1985, pp.105-110.

### Acknowledgement

This work was performed under a contract with Daniels Electronics Ltd, Victoria. The authors would like to thank the company for their financial support.