

# New Substrate-Integrated to Coplanar Waveguide Transition

Farzaneh Taringou and Jens Bornemann

*Department of Electrical and Computer Engineering, University of Victoria  
Victoria, BC, V8W 2Y2, Canada*

ftarango@uvic.ca

**Abstract**— A novel design for a transition from substrate-integrated waveguide (SIW) to regular coplanar waveguide (CPW) is presented. In comparison with previously published transitions, which employ conductor-backed CPWs and via holes, the new design achieves better return-loss performance. Dispersion curves highlight the related modes and the available bandwidths. The new design is optimized in an HFSS environment and is presented as a single transition and as a back-to-back version with more than 30 dB and 26 dB return loss, respectively, over a bandwidth of 19.5 GHz to 27 GHz. All design parameters are specified. A SIW-to-conductor-backed CPW and via holes is presented for comparison, showing return-loss values of only 21 dB and 14.5 dB. All presented performances include dielectric and metallic losses and are verified by comparisons between HFSS and CST Microwave Studio.

**Index Terms** — Substrate-integrated waveguide technology, coplanar waveguide, transitions.

## I. INTRODUCTION

For the purpose of circuit integration in the millimeter-wave frequency regime, substrate-integrated waveguide (SIW) technology has emerged as a successful compromise between all-metal waveguide and microstrip components, e.g. [1]. The boundary conditions and principal design guidelines of SIW are meanwhile well understood [2], and applications have been demonstrated up to the 100 GHz range [3], [4].

As SIW technology is meant to replace that of all-metal waveguides, one port of the SIW circuitry will be connected to an antenna. This is demonstrated in [5] and [6] by employing linearly tapered slot antennas. The other SIW port will have to be integrated with active devices, e.g., low-noise amplifiers (LNAs) in millimeter-wave receiver systems, which commonly use coaxial (quasi-TEM-type) ports.

It is common to interface SIW with microstrip lines, and design guidelines are available for single layered [7] and double layered [8] SIW-to-microstrip transitions. In order to exploit connectivity to a higher level of integrated circuits, coplanar waveguide (CPW) technology is more amenable to integration with MMICs or MHMICs [9]. Thus SIW transitions to CPW have been proposed [1] and are realized in double layered [10] and single layered [11], [12] substrate configurations. However, both single layered configurations

employ conductor-backed CPWs which are prone to higher-order (waveguide-type) mode excitation.

Therefore, this paper focuses on a transition from SIW to regular CPW with removed ground plane. The advantages of such a transition compared to those in [11], [12] include wider bandwidth and more design flexibility for the integration of active components. A larger substrate area can be viewed as a disadvantage. Compared to the design in [12], however, this follows logically from the simultaneous removal of the ground plane and associated vias.

## II. DESIGN

The application for the SIW-to-CPW transition is set for a frequency range of 19.5 GHz to 27 GHz. After consulting fabrication guidelines and tolerances, Rogers' low-permittivity substrate RT Duroid 5880 was selected. The relevant parameters are:  $\epsilon_r=2.2$ ,  $\tan\delta=0.0009$ , substrate height  $h=0.508$  mm, metallization thickness  $t=26$   $\mu\text{m}$ , conductivity  $\sigma=5.8\times 10^7$  S/m. Via-hole dimensions and spacing are selected according to [2], giving via diameters of 0.72 mm and center-to-center spacing of 1.02 mm. For this application, the SIW width measured between the centers of the via holes is chosen as 7.28 mm. This results in a fundamental-mode cutoff frequency of 15 GHz as shown as dotted lines in the normalized dispersion diagram of Fig. 1. Due to the symmetry of the transitions (c.f. Fig. 2), the next propagating mode in the SIW occurs at 45 GHz.

Also shown in Fig. 1 are the dispersion curves for a conductor-backed CPW with via holes (dashed lines), using design considerations similar to those in [11], [12] with a reduced SIW width of 3.64 mm and the regular CPW (solid line). For the substrate specified above, the center conductor of the 50 $\Omega$  regular CPW is 2.3 mm wide; its slot widths are 0.1 mm.

It is noted that in the conductor-backed CPW, the main waveguide mode due to vias and conductor backing appears at 34 GHz (dashed line) and thus limits the operational bandwidth of an SIW-to-CPW transition which, due to the second mode in the SIW, could potentially extend to 45 GHz (dotted line). This limitation is not present in the regular CPW (solid line) whose surface wave will start propagating at beyond 100 GHz [13]. The propagation constant of the quasi-TEM mode is higher in the conductor-backed CPW (dashed line) since the field is more concentrated in the dielectric than in the regular CPW. The normalized propagation constant of

the fundamental mode in the SIW (dotted line) approaches  $\sqrt{\epsilon_r} \approx 1.48$ .

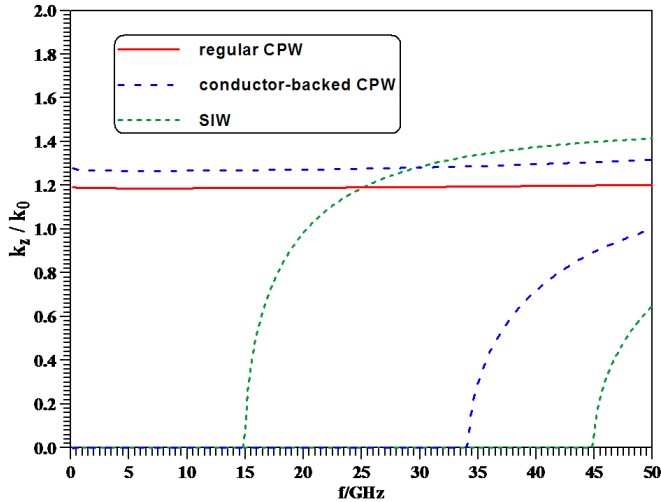


Fig. 1. Dispersion diagram for regular CPW and SIW as used in this paper, conductor-backed CPW with via holes according to [12];  $k_z$  and  $k_0$  are the propagation constants in the transmission line and in free space, respectively.

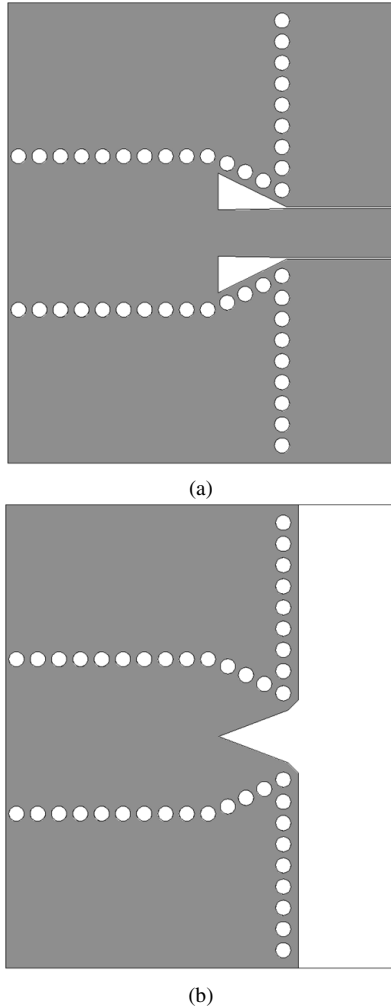


Fig. 2. Transition from SIW to regular CPW; (a) top view, (b) bottom view.

Based on this investigation, a transition from SIW to regular CPW is presented in Fig. 2. The SIW is first connected to a quasi-microstrip line (Fig. 2a) while its bottom metallization is gradually removed (Fig. 2b). Another gradual transition involving via holes brings the top ground planes closer to the microstrip line to form a regular CPW, with the bottom ground plane removed, when the via holes are lined up towards the edges of the substrate. The overall transition length from the SIW to the CPW is 3.27 mm; the width of the microstrip line extends from 2.19 mm to 2.3 mm. The dimensions of the triangular area with removed top metallization are 1.74 mm x 3.27 mm. The entire substrate width is 21.85 mm.

### III. RESULTS

The transition shown in Fig. 2 has been optimized in an HFSS environment for a return loss of 30 dB or better between 19.5 GHz and 27 GHz. Note that this and all following responses include the full dielectric and conductor losses as specified in the previous section.

Fig. 3 shows the response of the transition of Fig. 2 as predicted by HFSS and CST. The maximum insertion loss occurs at the higher frequency and is computed by HFSS and CST as 0.30 dB. The return loss curves are very similar with a slight frequency shift. However, both field solvers agree that the return loss is below 30 dB over the above frequency range

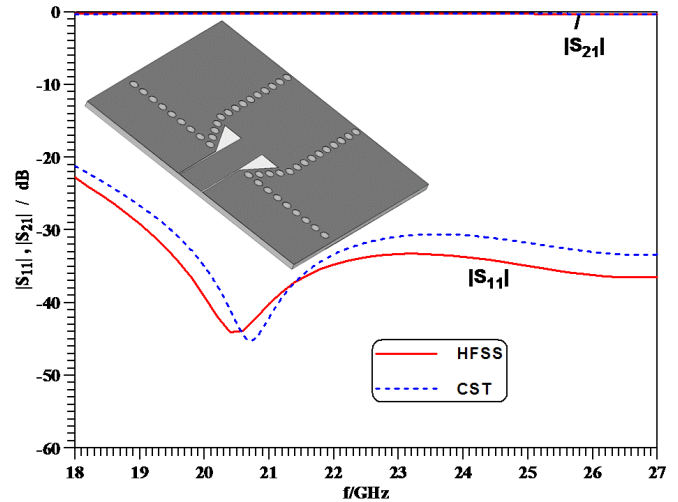


Fig. 3. Performance of the transition of Fig. 2, and comparison between results obtained with HFSS and CST; maximum insertion loss is 0.30 dB.

In order to compare this transition with the design of [12], Fig. 4 shows the performance of the respective transition to a conductor-backed CPW with via holes. Since the propagation characteristics for the conductor-backed and via-holed CPW are different (c.f. Fig. 1), the CPW center conductor and slot widths have been adjusted to resemble 50Ω line impedance.

The maximum insertion loss including all losses is 0.30 dB which is comparable with the new design presented in Fig. 2 and Fig. 3. However, the return loss predictions in Fig. 4 are not as good as the ones for the new design in Fig. 3. Moreover, they differ between HFSS (24 dB, solid line) and CST (21 dB, dotted line). Note that for future broadband

transitions, the circuit in Fig. 4 is limited to operation below 34 GHz (Fig. 1) by the conductor-backed and via-holed CPW whereas that of Fig. 3 actually extends all the way to 45 GHz as limited by the next symmetric higher-order mode in the feeding SIW.

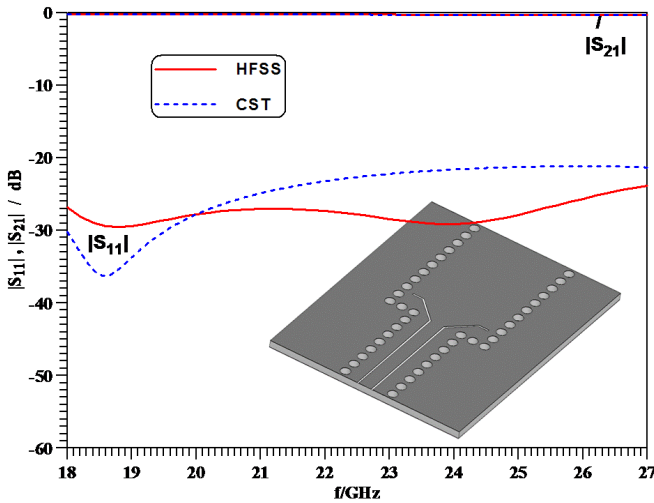


Fig. 4. Performance of a SIW-to-conductor-backed CPW with via holes as calculated by HFSS and CST; maximum insertion loss is 0.30 dB.

One of the best ways to test and measure a transition is to investigate two transitions connected back-to-back. We have opted for this scenario in order to first assure that the two individual transitions still meet the requirements and, secondly, that their mutual interactions do not influence the overall performance. Therefore, the circuits shown in the insets of Fig. 3 and Fig. 4 are simply mirrored to form CPW-to-SIW-to-CPW transitions without any consideration given to the actual length between the two transitions.

Fig. 5 shows the performance obtained from the back-to-back transitions of Fig. 3. (Note that the inset only shows the top view; the bottom view is a mirror image of Fig. 2b.) The agreement between the results obtained with HFSS and CST is very good. Both field solvers predict the insertion loss to be better than 26 dB over the 19.5-27 GHz frequency range. The maximum insertion loss is 0.65 dB (HFSS) and 0.60 dB (CST).

In comparing this performance to one obtainable from the back-to-back conductor-backed and via-holed CPW-to-SIW transition, it is obvious from Fig. 6 that the simple mirroring of transitions is not as straightforward as with the transition proposed in this paper. Although the insertion loss (HFSS: 0.72 dB, CST: 0.69 dB) is comparable to that of Fig. 5, the return loss exceeds the 20 dB mark at several frequencies as predicted by both HFSS (15.4 dB) and CST (14.5). It is assumed that the SIW-to-SIW discontinuities at either end contribute largely to the performance displayed in Fig. 6. That would suggest that the overall performance of a back-to-back transition depends on the length of SIW line between the individual transitions. Note that a back-to-back transition in [12] achieved a return loss of 20 dB over the entire Ka-band whereas a similar one in [11] failed to achieve 20 dB over a frequency range from 6 GHz to 10 GHz.

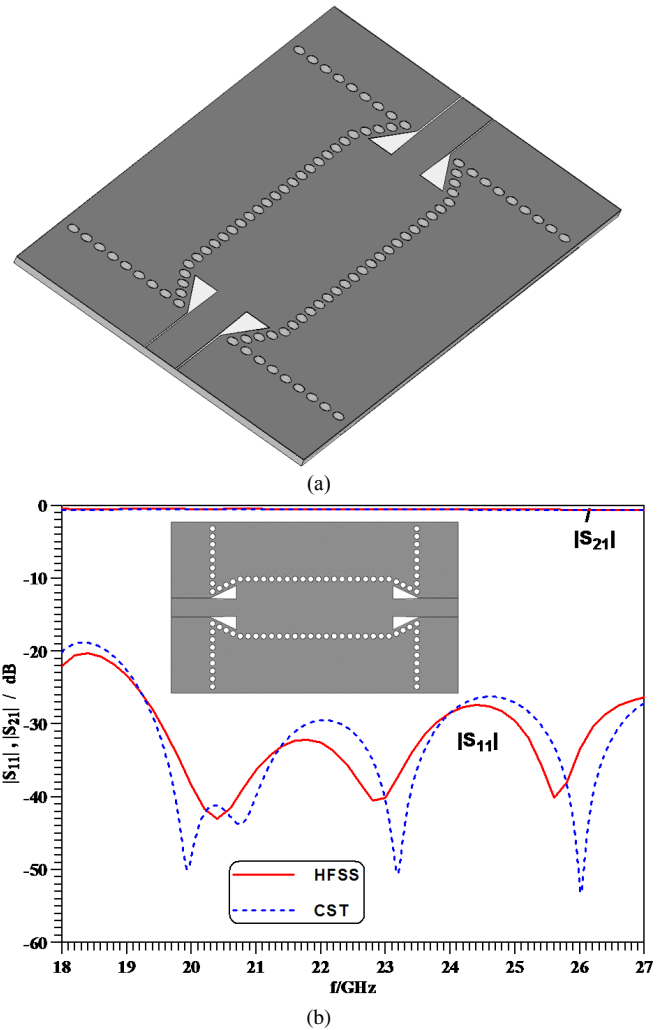


Fig. 5. 3D view (a), performance of the back-to-back transition of Fig. 3, and comparison with results obtained with HFSS and CST; maximum insertion loss is 0.64 dB.

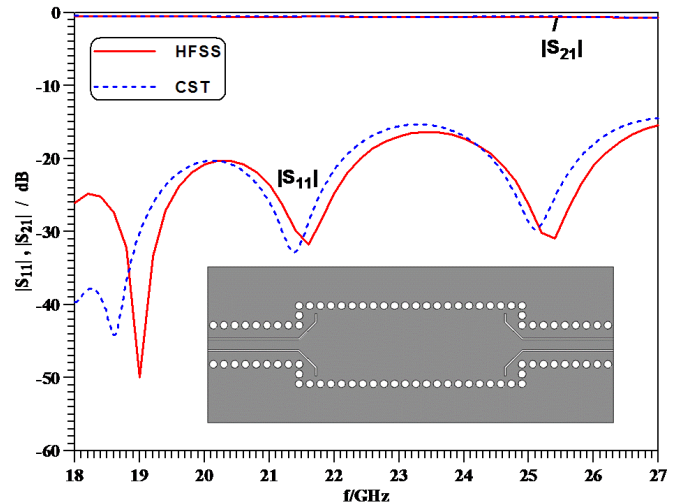


Fig. 6. Performance of a SIW-to-conductor-backed CPW with via holes as calculated by HFSS; maximum insertion loss is 0.72 dB; for direct comparison with Fig. 5.

#### IV. CONCLUSIONS

It is demonstrated that the new design for a transition from substrate-integrated waveguide to regular coplanar waveguide outperforms a similar one proposed in the literature, which involves a conductor-backed and via-holed CPW. First, the bandwidth of the regular CPW is wider and thus permits utilization of the full bandwidth provided by a symmetric transition with the incoming SIW. Secondly, the new transition is clearly better than one that uses a conductor-backed CPW and, thirdly, due to its better performance, is less sensitive to back-to-back connections as shown in a direct comparison.

Over a bandwidth of 19.5 GHz to 27 GHz, the new design achieves a return loss better than 30 dB for the single and better than 26 dB for the double transition. The respective performances include dielectric and metallic losses and are individually verified by comparison with two commercially available field solver packages. All design parameters are specified in the text.

#### ACKNOWLEDGMENT

The authors acknowledge support for this work from the Natural Sciences and Engineering Research Council of Canada.

#### REFERENCES

- [1] K. Wu, D. Deslandes, and Y. Cassivi, "The substrate integrated circuits - A new concept for high-frequency electronics and optoelectronics," *Proc. 6th Int. Conf. Telecommunications in Modern Satellite, Cable and Broadcasting Service (TELSIKS 2003)*, vol. 1, pp. PIII-PX, Oct. 2003.
- [2] Y. Cassivi, L. Perregrini, P. Arcioni, M. Bressan, K. Wu, and G. Conciauro, "Dispersion characteristics of substrate integrated rectangular waveguide," *IEEE Microwave Wireless Comp. Lett.*, vol. 12, pp. 333-335, Sep. 2002.
- [3] D. Stephens, P.R. Young, and I.D. Robertson, "Millimeter-wave substrate integrated waveguides and filters in photoimageable thick-film technology," *IEEE Trans. Microwave Theory Tech.*, Vol. 53, pp. 3832-3838, Dec. 2005.
- [4] E. Moldovan, R.G. Bosisio, and K. Wu, "W-band multiport substrate-integrated waveguide circuits," *IEEE Trans. Microwave Theory & Tech.*, vol. 54, pp. 625-632, February 2006.
- [5] I. Wood, D. Dousset, J. Bornemann, and S. Claude, "Linear tapered slot antenna with substrate integrated waveguide feed," *IEEE AP-S Int. Symp. Dig.*, pp. 4761-4764, Honolulu, USA, June 2007.
- [6] Y.J. Cheng, W. Hong, and K. Wu, "Design of a monopulse antenna using a dual V-type linearly tapered slot antenna (DVL TSA)," *IEEE Trans. Antennas Propagat.*, vol. 56, pp. 2903-2909, Sep. 2008.
- [7] D. Deslandes, "Design equations for tapered microstrip-to-substrate integrated waveguide transitions," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 704-704, Anaheim, May 2010.
- [8] A. Suntives and R. Abhari, "Transition structures for 3-D integration of substrate integrated waveguide interconnects," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, pp. 697-699, Oct. 2007.
- [9] I. Wolff, "Design rules and realisation of coplanar circuits for communication applications," *Proc. European Microwave Conf.*, pp. 36-41, Sep. 1993.
- [10] S. Lee, S. Jung, and H.-Y. Lee, "Ultra-wideband CPW-to-substrate integrated waveguide transition using an elevated-CPW section," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, pp. 746-748, Nov. 2008.
- [11] S. Lin, S. Yang, A.E. Fathy, and A. Elsherbini, "Development of a novel UWB Vivaldi antenna array using SIW technology," *Progress In Electromagnetics Research*, PIER 90, pp. 369-384, 2009.
- [12] X.-P. Chen and K. Wu, "Low-loss ultra-wideband transition between conductor-backed coplanar waveguide and substrate integrated waveguide," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 349-352, Boston, June 2010.
- [13] C.A. Balanis, *Antenna Theory: Analysis and Design*. John Wiley and Sons, Hoboken, New Jersey, 2005.