New Interface Design from Substrate-Integrated to Regular Coplanar Waveguide

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***Abstract* — A new design for a substrate-integrated waveguide (SIW) interfacing a regular coplanar waveguide (CPW) is reported and compared to a transition employing conductor-backed CPWs and via holed side walls. The new interface provides, first, better return loss and, secondly, larger bandwidth as demonstrated by the related modes in a dispersion diagram. The interface is optimized in an HFSS environment for single and back-to-back transition. Both single and back-to-back designs achieve more than 24 dB return loss between 18.5 GHz and 27 GHz. Their improved performances, which include dielectric and all metallic losses, are demonstrated by direct comparison with a transition involving conductor-backed CPWs and via holed side walls. Verification by CST Microwave Studio validates the designs. All dimensional parameters are specified.**

***Index Terms* — Substrate-integrated waveguides, coplanar waveguides, interfaces, transitions.**

I. Introduction

Substrate-integrated circuits (SICs) comprise a number of technologies which aim at replacing regular waveguide technology in integrated millimeter-wave applications [1], [2]. Particularly the substrate-integrated waveguide (SIW) has emerged as a planar-circuit alternative to all-metal waveguide, e.g. [3]. Basic conversion guidelines between the rectangular waveguide and the via-hole parameters in a SIW are reported, e.g., in [4] - [6].

For integrated receiver applications, transitions of SIW circuits to linearly tapered slot antennas are demonstrated in [7], [8]. An interface to a low-noise amplifier (LNA) is not as straightforward since LNAs employ coaxial-type technology such as microstrip lines or coplanar waveguides (CPWs).

Design guidelines to interface SIW with microstrip lines are available in [9] and [10] for single-layered and double-layered transitions, respectively. However, chip-type LNA integration is more amenable to CPW circuitry due to the uniplanar arrangement of center conductor and ground planes. To accommodate such an interface, SIW-to-CPW transitions are reported in [1], [11], [12] using single-layer circuitry, and one involving two substrate layers is proposed in [13]. However, all such designs employ conductor-backed CPWs with via-holed side walls which are known to be bandwidth-restricted due to higher-order mode propagation if the via holes are not extremely close to the CPW slots, e.g. [14], [15].

Therefore, this paper presents a new interface design from SIW to regular CPW (without conductor backing and via-holed side walls). Compared to [11], [12], the new interface provides good return loss, design flexibility for active component integration and, for future applications, a larger bandwidth.

II. Design

Fig. 1 shows the new interface design from SIW to regular CPW in a three-dimensional view (Fig. 1a), top side (Fig. 1b) and bottom view (Fig. 1c). The frequency range of interest is 18.5 - 27 GHz, and the substrate is selected as RT Duroid 5880 with ε_r=2.2, tanδ=0.0009, substrate height h=0.508mm, metallization thickness t=26μm, and conductivity σ=5.8x10^{7}S/m. For a cutoff frequency of 15 GHz, the via-hole diameter is 0.72mm; the center-to-center longitudinal and transverse spacings are 1.02mm and 7.28 mm, respectively, according to [4]. Since the transition is symmetric, the next propagating mode in the SIW is excited at 45 GHz. For the CPW, the center conductor of the 50Ω regular CPW is 2.3mm wide and its slot widths are 0.1mm.

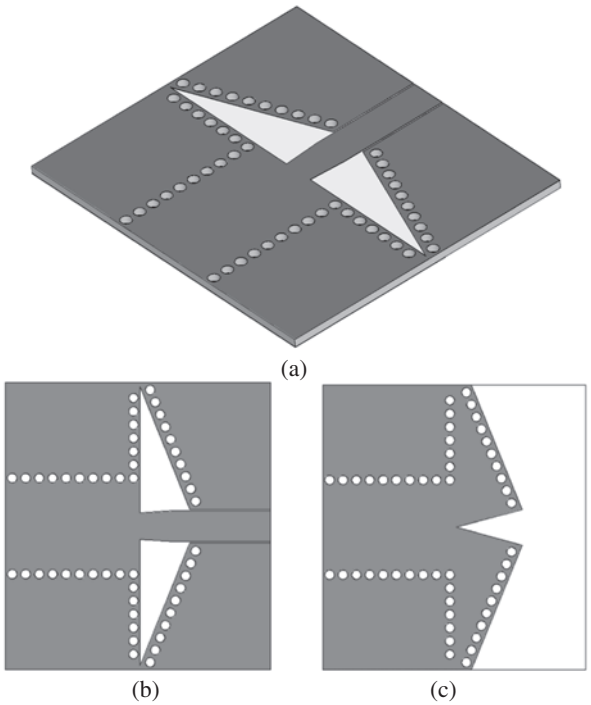

Fig. 1. Three-dimensional (a), top (b) and bottom view (c) of the new interface design from substrate-integrated to regular coplanar waveguide.

The SIW is first connected to a quasi-microstrip line (Fig. 1b) while its bottom metallization is gradually removed (Fig. 1c). Another gradual transition involving via holes brings the top ground planes closer to the microstrip line to form a regular CPW with the bottom ground plane removed. The overall transition length from the SIW to the CPW is 3.75mm; the microstrip line width extends from 1.59mm to 2.3mm over a length of 2.05mm. The entire substrate width is 21.85mm.

Since this new design will have to be compared to the transitions proposed in [11] and [12], Fig. 2 shows the interface of [12] that has been redesigned for the frequency range considered in this paper. In order to explain the different modes involved in the circuits shown in Fig. 1 and Fig. 2, a dispersion diagram with the respective modes is shown in Fig. 3.

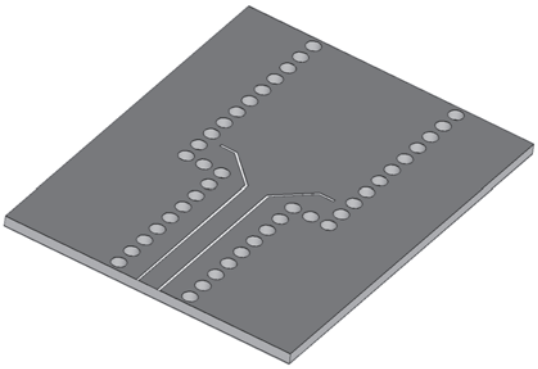

Fig. 2. Transition from SIW to conductor-backed CPW with via-holed side walls according to [12].

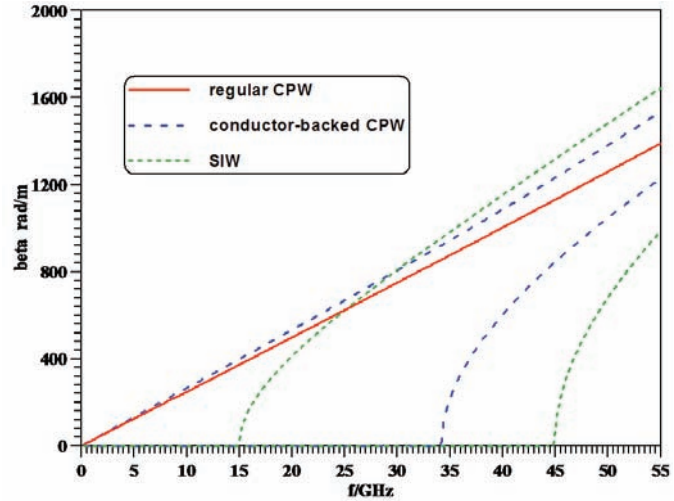

Fig. 3. Dispersion diagram for regular CPW as used in this paper, conductor-backed CPW with via-holed side walls according to [12] and SIW.

The solid line in Fig. 3 represents the regular CPW without conductor backing. The dashed lines are those of the conductor-backed CPW with via-holed side walls, using design considerations similar to those in [11], [12] with a reduced SIW width of 3.64mm. It is noted that the main waveguide mode due to via-holed side walls and conductor backing appears at 34 GHz (dashed line) and thus limits the operational bandwidth of the SIW-to-CPW transition in Fig. 2. Such a limitation is not present for the new design in Fig. 1.

The SIW curves are shown as dotted lines with the fundamental and next higher-order modes at 15 GHz and 45 GHz, respectively. Thus the bandwidth of the new interface design (Fig. 1) could potentially be extended to 45 GHz since the surface wave on the regular CPW will start propagating at beyond 100 GHz, e.g. [16].

The behavior of the three fundamental modes in Fig. 3 is explained as follows. The propagation constant of the quasi-TEM mode in the conductor-backed, via-holed CPW (dashed line) is higher than that of the regular CPW (solid line) since the field of the conductor-backed, via-holed CPW is more concentrated in the dielectric than that of the regular CPW. The fundamental mode in the SIW (dashed line) propagates entirely within the dielectric substrate and thus, towards higher frequencies, shows the highest propagation constant

III. Results

Fig. 4 shows the response of the new interface design of Fig. 1 as predicted by HFSS and CST. The maximum insertion loss between 18.5 GHz and 27 GHz is computed by HFSS as 0.31 dB and by CST as 0.30 dB. The return loss curves are very similar, and both field solvers agree that the return loss is below 24 dB over the specified frequency range. Note that this response and all following ones include full dielectric and conductor losses according to tanδ and conductivity specifications provided in the first paragraph of Section II.

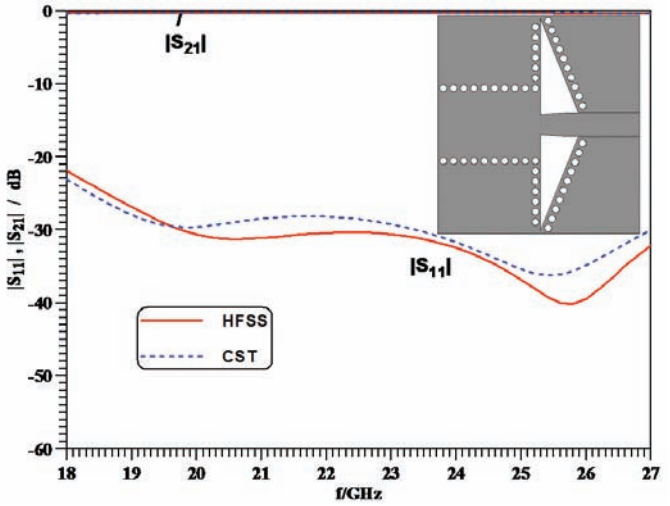

Fig. 4. Performance of the new interface design of Fig. 1, and comparison between results obtained with HFSS and CST; maximum insertion loss is 0.31 dB.

For comparison with Fig. 4, the performance of the respective interface to a conductor-backed CPW with via-holed side walls is shown in Fig. 5. Note that the center conductor and slot widths have been adjusted for 50Ω line

impedance since the propagation characteristics of the conductor-backed and via-holed CPW are different from those of the regular CPW (c.f. Fig. 3).

Return loss computations in Fig. 5 differ between HFSS (22 dB, solid line) and CST (19.9 dB, dotted line). The maximum insertion loss is 0.35 dB and is slightly higher than that of the new interface design in Fig. 4. As pointed out earlier, the circuit in Fig. 5 is limited to operation below 34 GHz (Fig. 3). The circuit of Fig. 4 can be extended, if required in future broadband applications, up to 45 GHz. It is important to note that this frequency limit is imposed by the next higher-order mode in the SIW, not by the regular CPW.

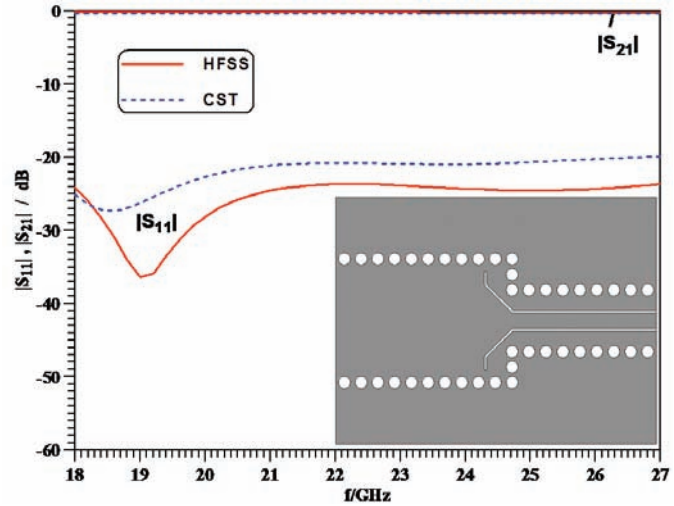

Fig. 5. Performance of a SIW-to-conductor-backed CPW with via-holed side walls as calculated by HFSS and CST; maximum insertion loss is 0.35 dB; for direct comparison with Fig. 4.

It is common practice to measure the quality of an interface between two different transition line technologies by connecting two individual interfaces back-to-back. Such investigation assures that the two individual transitions meet specifications. Moreover, mutual interactions between the two interfaces are not supposed to influence the overall performance of the back-to-back connection, and thus no consideration has been given to the actual length between the two transitions.

The performance of the back-to-back connection of two of the new interface designs is shown in Fig. 6. (Note that the inset only shows the top view; the bottom view is a mirror image of Fig. 1c.) Good agreement is observed between the results of HFSS and CST. The return loss predictions are better than 24 dB (for both field solvers) over 18.5 GHz to 27 GHz. Thus the back-to-back connection does not affect the return loss predicted for the individual interface. The maximum insertion loss is increased, of course, compared to a single interface and is at 0.59 dB (HFSS) and 0.63 dB (CST).

Fig. 7 shows the performance of a back-to-back connection of the transition involving a conductor-backed and via-holed CPW. The insertion loss (HFSS: 0.69 dB, CST: 0.73 dB) is comparable with the new design in Fig. 6. However, compared with the single transition in Fig. 5, the return loss is significantly increased by the back-to-back connection and stands at 15.8 dB (HFSS) and 13.7 dB (CST). Obviously, the increase in return loss compared to the single transition is due to interactions between the two SIW-to-SIW discontinuities at either end of the circuit in Fig. 7. It is thus concluded that the overall performance of this back-to-back transition is sensitive to the overall length between the individual transitions. In this respect it is explainable that a back-to-back transition in [12] achieves a return loss of 20 dB over the entire Ka-band whereas a very similar one in [11] barely reaches 13 dB between 6 GHz and 10 GHz.

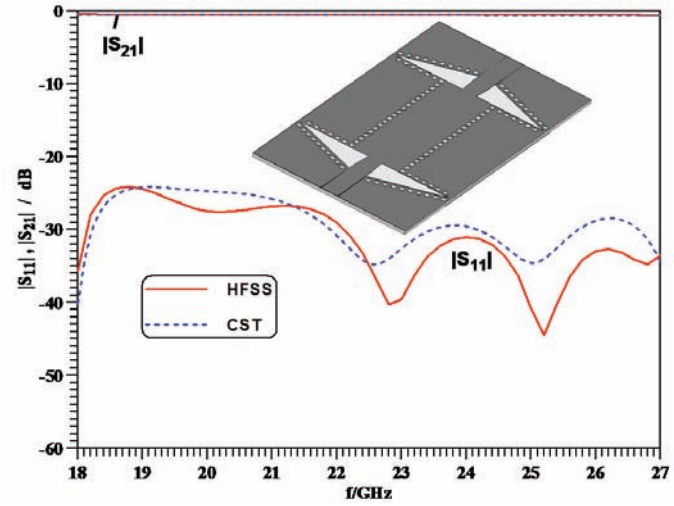

Fig. 6. Performance of the back-to-back transition of Fig. 1, and comparison between results obtained with HFSS and CST; maximum insertion loss is 0.63 dB.

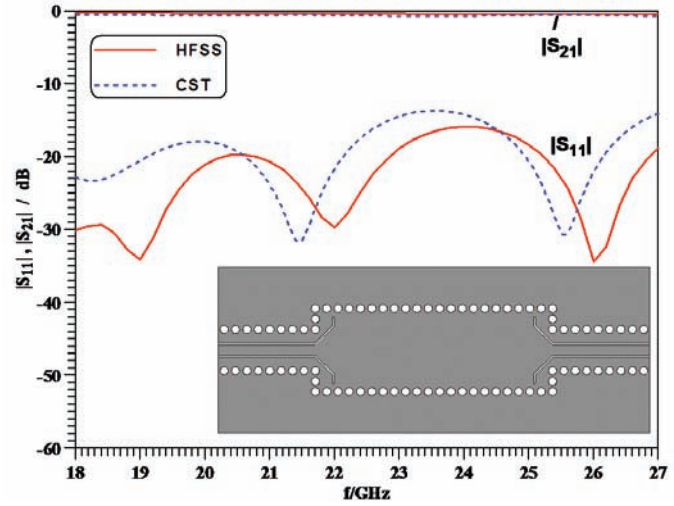

Fig. 7. Performance of the back-to-back transition of Fig. 2 as calculated by HFSS and CST; maximum insertion loss is 0.7 dB; for direct comparison with Fig. 6.

IV. Conclusions

The new design of a substrate-integrated waveguide (SIW) interfacing a regular coplanar waveguide (CPW) presents a viable option for microwave and millimeter-wave integrated

circuit applications. Compared to previous transitions employing conductor-backed CPWs and via holed side walls, the new interface provides not only better return loss but also larger bandwidth. Moreover, the performance of its back-to-back connection appears to be less dependent on the length between the two transitions. The single design is optimized in an HFSS environment and includes dielectric and all metallic losses. Both single and back-to-back interfaces achieve a return loss of better than 24 dB between 18.5 GHz and 27 GHz. All performances are validated by comparison with data obtained by CST Microwave Studio. Dimensional parameters are described and specified in the text.

ACKNOWLEDGEMENT

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