

Inverted Interconnect Between Substrate Integrated Waveguide and Coplanar Waveguide

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Abstract — A new interconnect between substrate integrated waveguide (SIW) and coplanar waveguide (CPW) is introduced. Contrary to similar interconnects to CPW or grounded CPW (GCPW), in which the top plate of the SIW is transitioned to the center conductor of the CPW, the new design connects the bottom plate of the SIW to the center conductor of the CPW by means of a row of via holes. It is thus termed ‘inverted’ interconnect. A parametric analysis of the two design parameters involved determines the interconnect design which is validated by two commercially available field solvers. A back-to-back transition is prototyped and measured. Experimental results agree well with theoretical predictions and achieve a return loss of better than 16 dB over the entire 18 – 28 GHz range with a maximum insertion loss of 1.2 dB. The comparative values of a non-inverted back-to-back SIW-to-CPW prototype are 15 dB and 1.5 dB, respectively. Moreover, the non-inverted transition requires a larger substrate area.

Index Terms — Integrated circuit interconnections, integrated circuit measurements, dielectric substrates, wideband.

I. INTRODUCTION

Since its introduction in 2001 [1], substrate integrated waveguide (SIW) technology has been the focus of intensive design and prototyping activities. In order to interface SIW with other printed-circuit transmission lines, either for measurement purposes or amplifier integration [2], interconnects with adequate return or minimum insertion loss over the monomode bandwidth of the SIW must be provided. Interconnects between SIW and microstrip are common, e.g. [3], but transitions to grounded CPW [4], [5] and regular CPW [6], [7] have also been reported.

Common to all such interconnects is the fact that the top plate of the SIW is interfaced with the center conductor of the CPW or microstrip line while the bottom plate of the SIW either remains as ground in case of the microstrip transition, or is transitioned to the two top grounds of a CPW.

This paper focuses on a so-called ‘inverted’ interconnect between SIW and CPW in which the bottom plate of the SIW becomes the center conductor of the CPW. The design is achieved by opening the top plate of the SIW and connecting its bottom plate to the CPW’s center conductor by a row of additional via holes. At the same location, the remaining ground plane metallization of the SIW is removed, thus obtaining an inverted interconnect from SIW to regular CPW.

II. DESIGN OF INVERTED INTERCONNECT

Fig. 1 shows the principal design layouts of the inverted SIW-to-CPW interconnect. The substrate is selected as RT/Duroid 6002 with $\epsilon_r=2.94$, $\tan\delta=0.0012$, substrate thickness $h=508\ \mu\text{m}$, metallization thickness $t=17.5\ \mu\text{m}$, and conductivity $\sigma=5.8\times 10^7\ \text{S/m}$. The bandwidth is fixed from 18 GHz to 28 GHz, and the cutoff frequency of the SIW is 15 GHz. The center conductor of the 50 Ω CPW line is 3.1 mm wide and its slot widths are 0.15 mm. Via diameters and center-to-center spacing of the SIW are chosen as 0.61 mm and 0.866 mm, respectively.

Fig. 1 shows how the top metallization of the SIW opens up to a width that includes the CPW center conductor plus the two slots. The length of this linear transition is the design parameter L_{trans} . The bottom metallization of the SIW is abruptly terminated, as shown in Fig. 1b, except for the strip line taper of initial width W_{trans} . Since the final width of this taper equals that of the CPW’s center conductor and the length of the taper equals L_{trans} , only two parameters are required for the design of this interconnect. The small array of via holes, which connect the strip taper in Fig. 1b with the center conductor in Fig. 1a, have via diameters of 0.25 mm and center-to-center spacing of 0.5 mm.

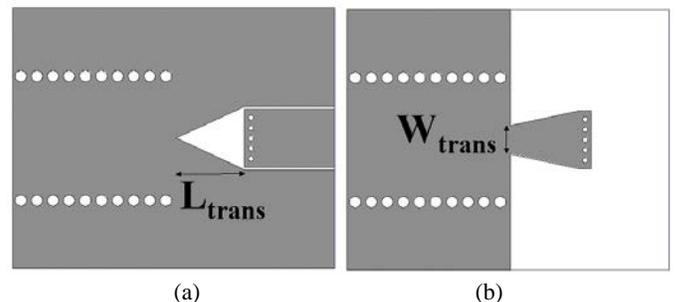


Fig. 1. Top (a) and bottom (b) view of the inverted SIW-to-CPW interconnect and its principal design parameters: transition length L_{trans} and strip width W_{trans} .

In order to design the interconnect over the bandwidth specified above, a parametric analysis with respect to the two design parameters is performed. Fig. 2a shows the variation of the length L_{trans} for a given width W_{trans} , which was initially

selected as half the center conductor width. It is observed that as the interconnect length increases from 0.5 mm to 2.3 mm, the reflection coefficient goes through a minimum which is shown in Fig. 2a by the dash-dotted curve referring to $L_{\text{trans}}=1.4$ mm. Similarly, for $L_{\text{trans}}=1.4$ mm, Fig. 2b shows that the reflection coefficient goes through a minimum as W_{trans} increases from 0.5 mm to 2.3 mm.

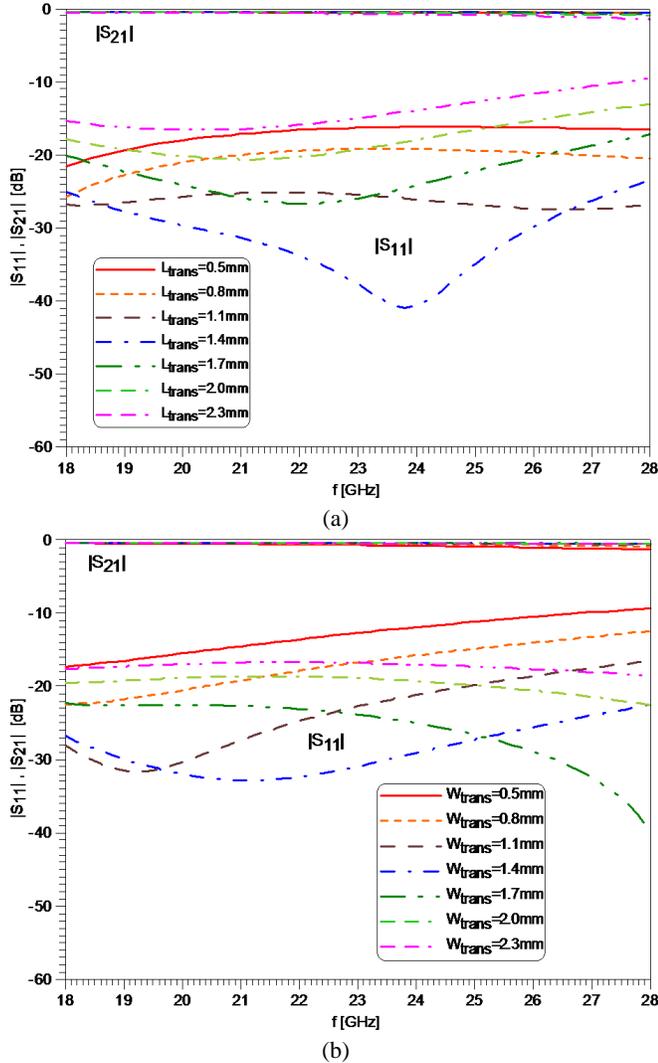


Fig. 2. Influences of the two design parameters shown in Fig. 1 on the reflection coefficient of the SIW-to-CPW interconnect. (a) Length variation for given width; (b) width variation for given length.

The final dimensions are $L_{\text{trans}}=3.6$ mm and $W_{\text{trans}}=1.46$ mm. Note that the final length of the transition is larger than the values in the parametric analysis. This is due to limitations in the fabrication process. If the length of the transition is too small, the clearance gap at the opening of the slot becomes very small and hard to fabricate.

This interconnect is now analyzed with both the frequency-domain solver HFSS and the time-domain solver of CST. Fig. 3 shows the respective performances. The agreement between both field solvers is very good. The minimum return loss is

20.5 dB and occurs at the highest frequency of 28 GHz. The maximum insertion loss is 0.6 dB at the same frequency.

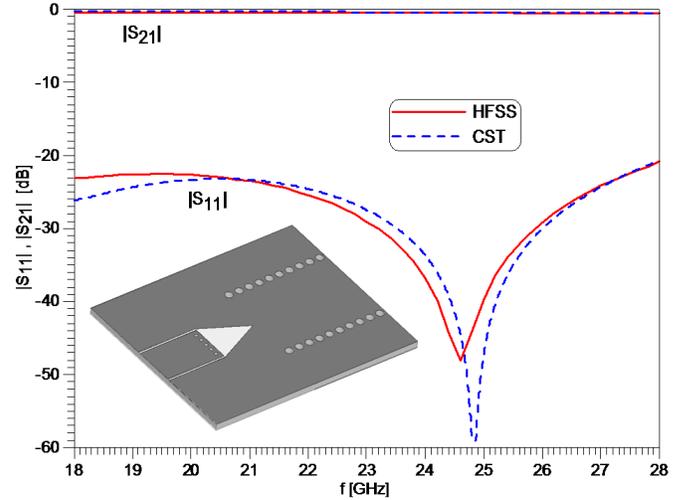


Fig. 3. Performance of the SIW-to-CPW interconnect and comparison between HFSS and CST.

III. EXPERIMENTAL RESULTS

Since the SIW port is not directly accessible with measurement equipment, it is common practice to verify such interconnects in a back-to-back arrangement. Front and back photographs of the manufactured prototype are displayed in the inset of Fig. 4. Note that no attempt has been made to alter the length between the transitions. The back-to-back prototype is simply a mirrored version of the single interconnect shown in the inset of Fig. 3.

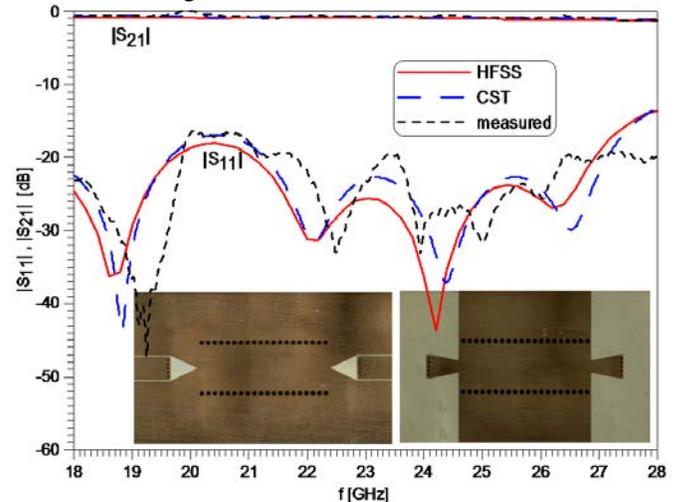


Fig. 4. Measurement of the inverted SIW-to-CPW interconnect prototype in back-to-back arrangement and comparison with HFSS and CST.

Fig. 4 shows a comparison between the measured data and results obtained with HFSS and the time-domain solver of CST. Both simulations agree reasonably well, and the experimental results validate the design. The measured return loss is better than 16 dB over the entire 18 GHz to 28 GHz frequency range. The maximum measured insertion loss is 1.2

dB and occurs at 28 GHz. This agrees well with the insertion loss of 0.6 dB predicted for the single interconnect for the same frequency in Fig. 3. Note that all other transitions and connectors for measurements with the network analyzer have been deembedded by using TRL calibration standards .

For comparison, Fig. 5 shows measurements and simulations of a non-inverted back-to-back SIW-CPW interconnect where the top metallization of the SIW is connected to the center conductor of the CPW, e.g. [6]. The front and back metallization are shown in the inset. It is obvious that this transition requires more real estate due to the fact that it is wider than the inverted one shown in the inset of Fig. 4.

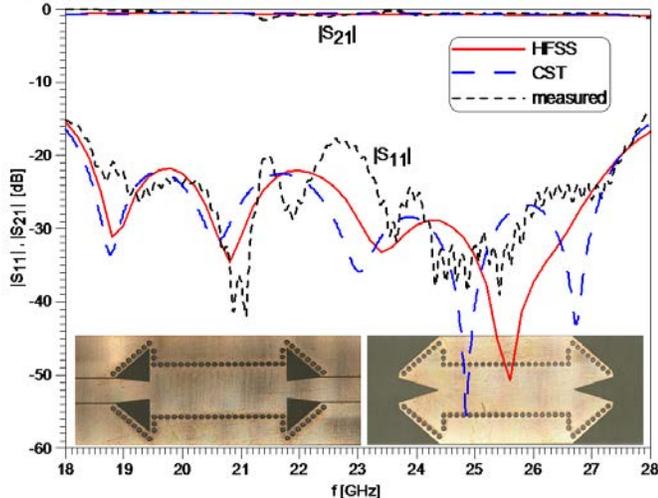


Fig. 5. Measurement of the non-inverted SIW-to-CPW prototype in back-to-back arrangement and comparison with HFSS and CST.

It is observed that measurements agree with simulations in principal. The calculated minimum return and maximum insertion losses occur at 28 GHz and are 15.4 dB and 0.97 dB, respectively. The corresponding measured values are 15.0 dB and 1.5 dB. Thus over the same bandwidth, the new inverted interconnect performs slightly better and requires less space than the non-inverted one.

IV. CONCLUSION

A new SIW-to-CPW interconnect is presented. Contrary to previously published transitions, this interconnect connects the bottom plate of the SIW to the center conductor of the CPW. It is just termed 'inverted'. It is first demonstrated that the inverted interconnect presents a viable alternative compared to the traditional ones. Secondly, measurements on back-to-back prototypes over a frequency range of 18 GHz to 28 GHz show that the inverted interconnect performs slightly better. Thirdly, by comparing the two different interconnects, it is obvious that the new interconnect requires less area on the printed-circuit board and thus is better suited for dense packaging.

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