Experimental Verification of Coplanar-to-Substrate-Integrated-Waveguide Interconnect on Low-Permittivity Substrate

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Abstract — **An interconnect between coplanar waveguide (CPW) and substrate integrated waveguide (SIW) is designed and experimentally verified. Common to regular SIW circuits is a low-permittivity substrate, whereas design formulas CPW usually assume a high permittivity. Therefore, commercially available field solvers are used in a parametric study to optimize the interconnect over a wide bandwidth between 18 GHz and 28 GHz. Cross-sectional field plots demonstrate its basic operation. The individual interconnect achieves return and insertion losses better than 20 dB and 0.5 dB, respectively, over the entire frequency range. The respective values for a measured back-to-back transition are 17 dB and 1.45 dB which are in good agreement with simulations.**

Index Terms — **Integrated circuit interconnections, integrated circuit measurements, dielectric substrates, wideband.**

I. INTRODUCTION

Amplifiers and other nonlinear-circuit integrations in substrate integrated waveguides (SIWs) require interconnects between SIW and transmission lines that support (quasi-) TEM mode propagation [1], [2]. Therefore, a number of such transitions have been proposed which can roughly be divided in dual- or multi-layer substrate circuits [3], [4] and single-layer interconnects [5] – [11].

For broadband operation and for simplicity, single-layer transitions are often preferred as they do not suffer from issues related to the mechanical alignment of individual boards. Interconnects between microstrip and SIW are well documented [5]. Other interconnects include transitions from SIW to coupled microstrip lines [6], conductor-backed (or grounded) CPW (GCPW) [7], [8], coplanar stripline (CPS) and slotline (SL) [9]. Apart from CPS and SL, particular emphasis is placed on CPW due its versatility in uniplanar surface-mount component integration [9], [10] and potentially wider bandwidth compared to GCPW [11], [12]..

This paper presents an interconnect between CPW and SIW on low-permittivity substrate. It is based on a modification of the circuit in [9] in that the lateral via holes are removed. Thus the width of the circuit is reduced to the width of the SIW which provides for smaller circuitry and denser packaging. Moreover, back-to-back connected interconnects are prototyped and experimentally verified.

II. SINGLE INTERCONNECT

The low-permittivity substrate is chosen as RT/Duroid 6002 with ε_r=2.94, tanδ=0.0012, substrate thickness h=0.508 mm, metallization thickness t=17.5 μm, and conductivity σ=5.8x10^7 S/m. The operating frequency range is 18 GHz to 28 GHz. The center conductor of the CPW is 3.1mm wide and its slot widths are 0.15mm, thus forming an impedance of 50 Ω. For the SIW, via diameters and center-to-center spacing are 0.61 mm and 0.866 mm, respectively. The SIW cutoff frequency is 15 GHz. Fig. 1 shows the top and bottom layout of the single interconnect. It is based on [9] in principle but features an immense reduction in width due to the omission of two rows of lateral via holes. Also shown in Fig. 1 are locations labeled A – F for which cross-sectional field plots will be presented in Fig. 2.
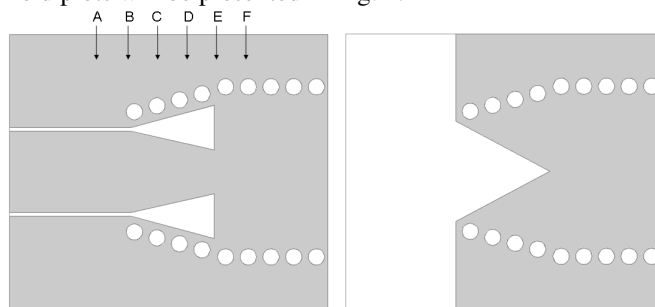

Fig. 1.   Front and back metallization of CPW-to-SIW interconnect on low-permittivity substrate and locations A –F of cross-sectional field plots in Fig. 2.

Note that closed-form expressions for the characterization of CPW circuits, e.g. [13], are valid only for high-permittivity substrates. Therefore, the design of this interconnect on low-permittivity substrate is based on a parametric study involving commercially available field solvers such as HFSS and CST. For given substrate, via-hole and frequency specifications, the design of this interconnect uses two dimensional parameters: the length of the transition, and the width of the strip line that is connected to the SIW at location E (Fig. 1). Other parameters such as the angle of the via holes in the transition or the cut-out areas in the top and bottom metallization follow directly from these two parameters.
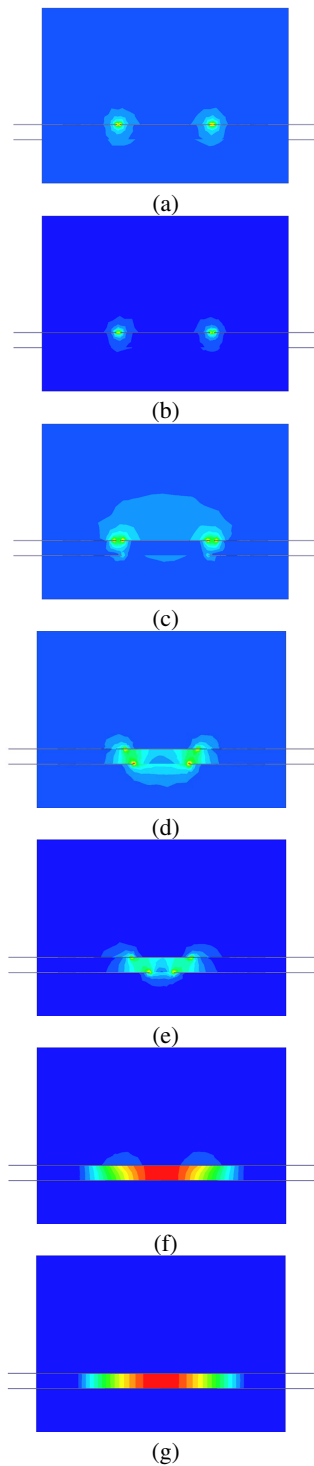
(a)

(b)

(c)

(d)

(e)

(f)

(g)

Fig. 2.   Electric fields in cross sections at locations A to F ((a) – (g)) in Fig. 1 at 23 GHz. (Note that field levels are arbitrarily scaled for better visibility.)

Fig. 2 shows the cross-sectional electric field at the individual locations marked in Fig. 1. The operation of the interconnect is based on a field rotation. In the CPW, the field is most located in the slots (Fig. 2a, b). When the center conductor narrows, the slots widen and a ground plane is gradually introduced; the field starts to rotate and accepts the bottom metallization as ground rather than the top grounds of the CPW (Fig. 2c, 2d, 2e). As the slot in the bottom metallization vanishes, the rotation is completed with only a small field present in the triangular cut-out area (Fig. 2f). Finally, the field settles as the fundamental TE_{10} mode in the SIW (Fig. 2g).

A parametric study and fine optimization of the width and length of the interconnect determines the final dimensions: They are L =3.18 mm for the length and W=1.68 mm for the width of the center conductor at the SIW. Note that the width of the CPW's center conductor is 3.1 mm.

Fig. 3 shows the performance of the single interconnect and a comparison between results obtained with the frequency-domain solver HFSS and the time-domain solver of CST.
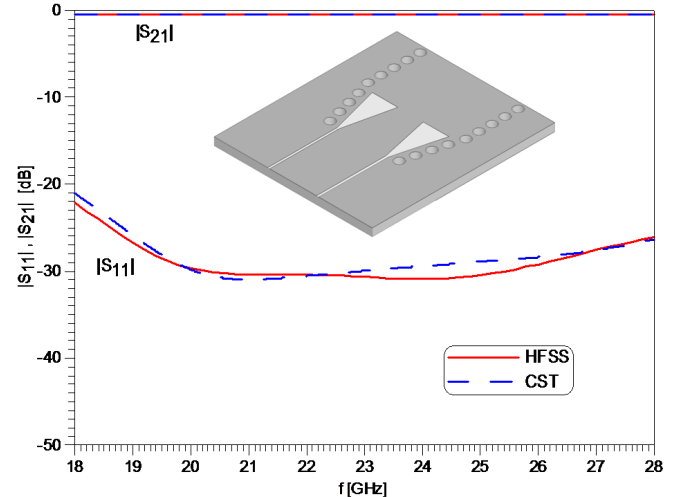

Fig. 3.   Performance of single CPW-to-SIW interconnect and comparison between HFSS and CST.

Very good agreement is observed between HFSS and CST. The input reflection coefficient is below -20 dB over the entire frequency range and below -25 dB from 18.8 GHz upward. The computed insertion loss is between 0.41 and 0.46 dB.

III. EXPERIMENTAL RESULTS

For the purpose of experimental validation, back-to-back transitions are more appropriate in a measurement setup [7], [8]. Thus the single CPW-to-SIW interconnect of Fig. 1 was mirrored to form a back-to-back transition. Note that no attempts have been made to change the length of the SIW between the two interconnects. Fig. 4 shows photographs of the top and bottom views of the prototype.
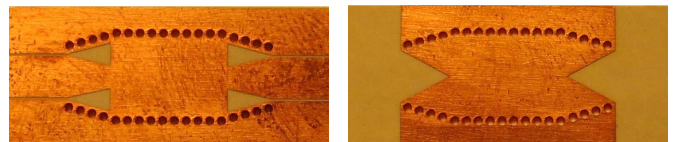

Fig. 4.   Photographs (top and bottom) of the fabricated prototype of the back-to-back CPW-to-SIW interconnect.

The measurements are shown in Fig. 5 together with simulated results of HFSS and CST. In order to eliminate influences of the universal test fixture on the measurements, LRL calibration standards are used. The two simulations agree reasonably well, and the discrepancies between results obtained with CST and HFSS are in the same order of magnitude as observed elsewhere [10] – [12] for back-to-back connections.

The $|S_{11}|$ measurement is generally in good agreement with simulations. The measured return loss is better than 17 dB over the entire frequency range, and the maximum insertion loss is 1.45 dB and occurs at 19 GHz. For most of the center band (19.4 GHz – 26 GHz), however, the measured insertion loss is less than 1 dB.
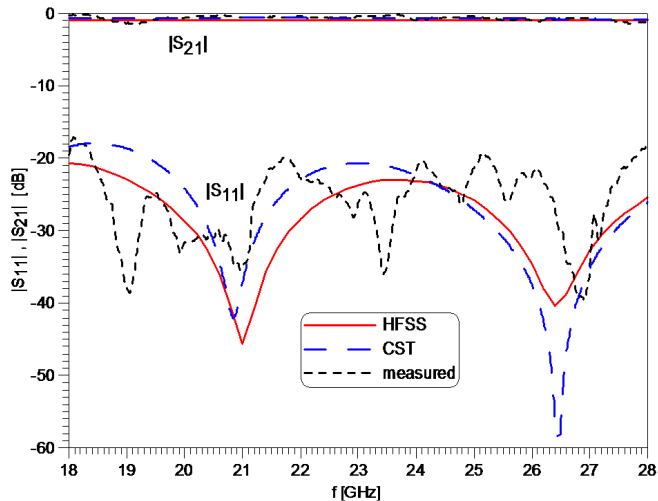

Fig. 5. Measured performance of back-to-back CPW-to-SIW interconnect and comparison with HFSS and CST.

IV. CONCLUSIONS

The interconnect between CPW and SIW offers a wideband transition between the two transmission-line media that can be used to integrate active components within SIW circuitry. As SIW technology is geared to replace many all-metal waveguide components, it is usually realized on low-dielectric substrates to keep dielectric losses to a minimum. On the other hand, CPW is often used on high-permittivity substrate where closed-form design equations are available. In order to combine the two technologies, the interconnect is designed on low-permittivity substrate. Its performance is validated by two commercially available field solvers, and a back-to-back transition is experimentally verified. The good performance and low space requirements of this interconnect make it an ideal candidate for CPW surface-mounted device integration within larger SIW cuircuits and subsystems.

ACKNOWLEDGEMENT

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