Broadband Design of Substrate Integrated Waveguide to Stripline Interconnect

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***Abstract* — A broadband design of substrate integrated waveguide (SIW) to stripline interconnects is presented for the first time. The transition shows a wideband performance and, contrary to microstrip and coplanar waveguide circuitry, interconnects two planar transmission-line media that are both capable of medium-level power handling capabilities. Over a bandwidth of 18 GHz to 28 GHz (43.4 percent), the single interconnect shows a worst-case return loss of 24 dB and maximum insertion losses of 0.44 dB. For a back-to-back connection, the return loss reduces to 19 dB and insertion loss increases to 0.87 dB. All dimensional parameters are specified, and the design is validated by two commercially available field-solver packages. Moreover, field plots are presented that highlight the step-by-step mode conversion from SIW to stripline.**

***Index Terms* — Integrated circuit interconnections; substrate integrated waveguide; stripline; transitions; wideband.**

I. Introduction

Substrate integrated waveguide (SIW) circuitry has developed into a mature technology over the last decade, [1], [2]. However, as waveguide components have to interconnect with (mostly) coaxial components for the integration of amplifiers and other non-linear components, so do SIW circuits, e.g. [3]. Therefore, and due to the planar nature of SIW, a number of transitions from SIW to other planar transmission lines have been developed. For access with measurement equipment, SIW is usually interfaced with microstip [4]. Other transitions, mostly for integration with surface-mount components, include coplanar waveguide (CPW), coplanar stripline (CPS), slotline [5] and grounded CPW [6].

All such interconnects assume low power levels that planar transmission lines can handle. As a waveguide-based technology with quality factors one order of magnitude higher than microstrip [7], SIW is able to manage medium-level power applications that the above-mentioned planar transmission-line circuits would not be able to handle.

Stripline is a dual-layer planar transmission line that can handle medium-level power applications [8], [9]. So far, however, stripline interconnects have only be designed to interface with microstrip [10], [11] or CPW technology [12] – [15]. The only published stripline configuration in connection with SIW is part of a triple-layered magic-T in SIW technology [16]. However, this circuit does not contain a direct SIW-to-stripline interconnect. Moreover, a microstrip-to-stripline transition is used for measurement purposes.

Therefore, for the first time, this paper presents a SIW-to-stripline interconnect design that is capable of exploiting the medium-level power handling capability of both SIW and stripline. The design is based on an SIW-to-microstrip transition, but with a second substrate layer added so that the stripline mode is directly excited from the end of the SIW. An array of via holes connect the top and bottom plates of the stripline for proper ground connection.

II. Interconnect Design

Fig. 1 shows a three-dimensional view of the SIW-to-stripline interconnect. The substrate is selected as Rogers RT/Duroid 6002 with ε_r=2.94, tanδ=0.0012, substrate height h=0.508 mm, metallization thickness t=17.5 μm, and conductivity σ=5.8x10^{7}S/m. The width of the SIW between via hole centers is a=6.71 mm, thus setting a cutoff frequency of f_c=14.1 GHz when considering via hole diameter and spacing as specified in Table I. The stripline is formed by adding a second substrate layer so that its height is $2h+t$=1.0335 mm. Together with the conductor width of 0.63 mm, this forms a 50 Ω stripline.

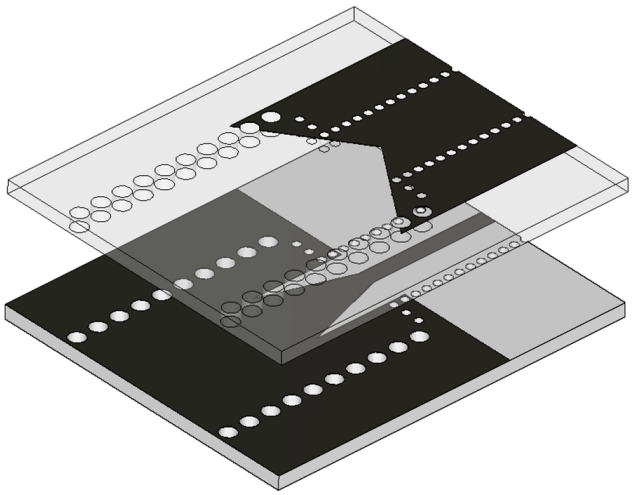

Fig. 1 3-D view of the two substrate layers that form the wideband SIW-to-stripline interconnect.

The lower substrate layer holds the SIW and a tapered transition that forms the central conductor of the stripline with side via holes and then continues like a microstrip line when the side conductors are abruptly terminated. The top layer introduces the top plate of the stripline which is tapered in order to gradually form the stripline mode. The smaller and narrower array of via holes serves to suppress both parallel-plate TEM and waveguide TE_{10} mode excitations in the stripline.

Fig. 2 shows the top view of the SIW-to-stripline interconnect, identifying all design parameters whose values are depicted in Table I. Together with the substrate and SIW information provided earlier, this completely specifies all dimensions of the interconnect.

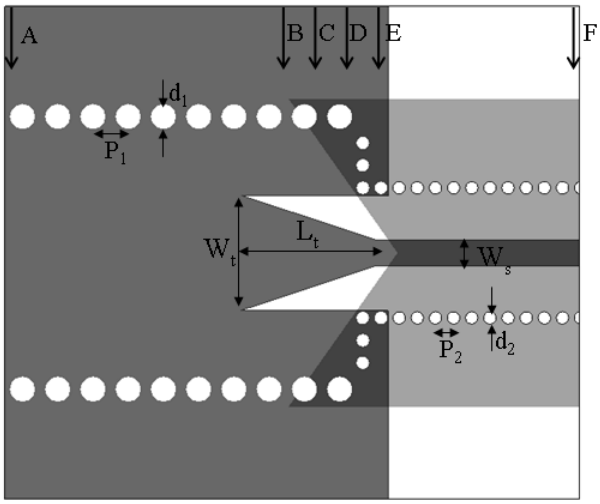

Fig. 2 Top view of the broadband SIW-to-stripline interconnect and design parameters.

TABLE I: DIMENSIONS OF INTERCONNECT IN MM

W_t	L_t	W_s	P_1	d_1	P_2	d_2
2.83	3.32	0.63	0.86	0.62	0.44	0.31

In order to explain and demonstrate the operation of the SIW-to-stripline interconnect, Fig. 3 presents the cross-sectional electric field plots at various stages within the transition. These are the locations labeled A to F in Fig. 2.

Fig. 3(A) shows the electric field of the fundamental mode in the SIW. The mode is confined within the SIW, and there is no field in the upper substrate layer. Upon entering the tapered section in Fig. 3(B), the electric field partly rotates and concentrates within the slots but also extends into and above the top substrate layer. This could potentially give rise to radiation, but a few facts discourage the field from radiating: first, the symmetric nature of the field which prevents a significant field accumulation above the top substrate, secondly, the introduction of the tapered top metallization and finally, the continuous presence of a bottom ground which binds the electric field lines. The respective part of the field is thus forced back into the top-layer substrate as shown in Fig. 3(C) and Fig. 3(D) and accumulates between the center conductor and the top ground plane (Fig. 3(E)). This field configuration then continues through the interconnect and forms the stripline mode (Fig. 3(F)). Note that the parallel-plate mode of the stripline is not excited due to the small vias shown towards the right of Fig. 2.

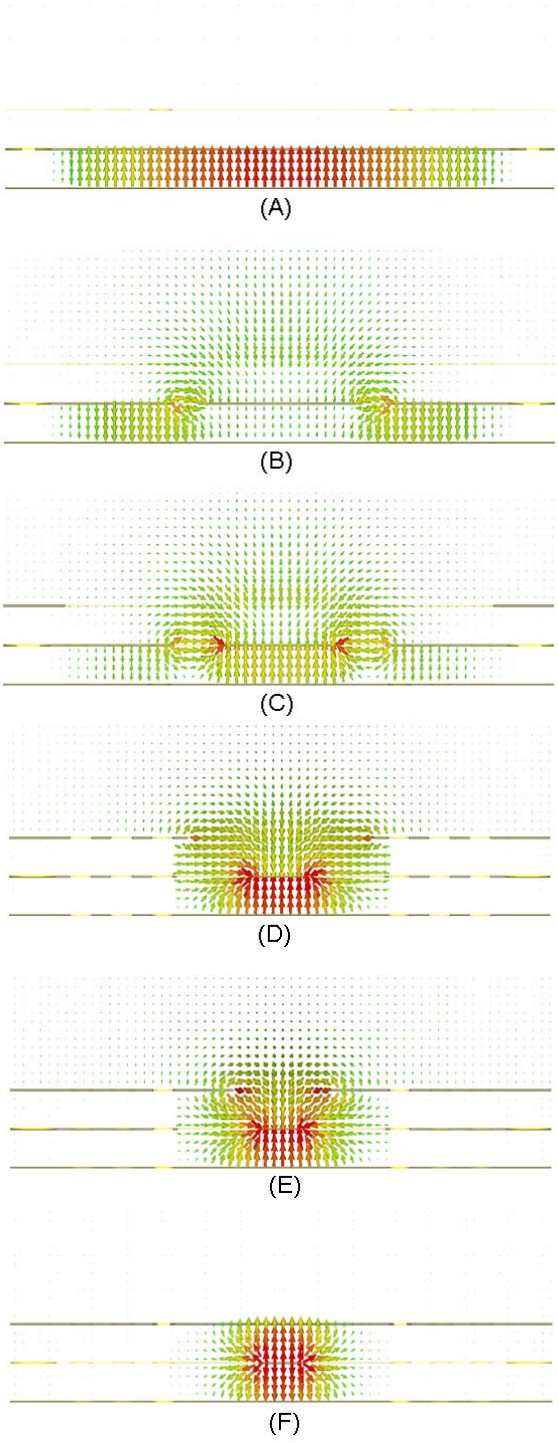

Fig. 3 Cross-sectional electric field plots of the interconnect at locations A to F as labeled in Fig. 2.

Moreover, the waveguide mode in the SIW does not propagate through the interconnect due to the reduced width of the vias in the stripline section. The lateral distance between these vias is half of that of the SIW, thus setting the cutoff frequency of the waveguide mode in the stripline to slightly above 28 GHz which is beyond the operating frequency range of the interconnect.

III. Results

Fig. 4 shows the performance of the SIW-to-stripline interconnect, using all dimensions specified in the previous section, and including dielectric and conductor losses of both substrate layers. The simulations are carried out by using the time-domain solver of CST MWS and the frequency-domain simulator HFSS. A very broadband behavior is displayed with a worst-case return loss better than 24 dB over the entire 18 GHz to 28 GHz frequency range (43.4 percent). The highest insertion loss occurs at the highest frequency and is computed as 0.44 dB in HFSS and 0.36 dB in CST. The slight differences between results obtained with the two full-wave field solvers is mainly the result of the fact that CST and HFSS treat sharp conducting edges with high field concentration and singularities differently. Furthermore, the built-in adaptive mesh refinement algorithms operate differently in each case. Similar discrepancies between these two solvers have been observed previously, e.g. [5], [17], [18].

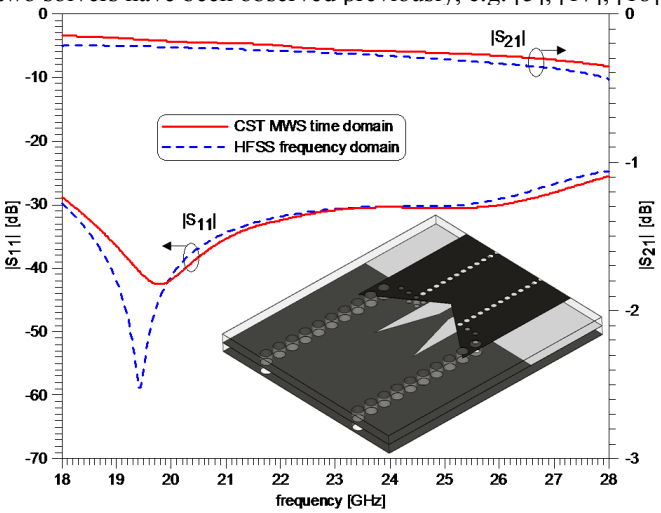

Fig. 4 Performance of wideband SIW-to-stripline interconnect and comparison between CST and HFSS.

In order to assess the quality of the single interconnect and for access to measurement equipment, it is common practice to investigate back-to-back transitions. Fig. 5 shows the performance of the single interconnect of Fig. 4 in a back-to-back (mirrored) arrangement. Due to the number of maxima and minima in the return loss ($|S_{11}|$) response, it is expected that the two interconnects interact and that this interaction is mainly due to the two discontinuities formed by the abrupt reduction of the via widths within the transitions. Similar behavior has been observed in back-to-back transitions of SIW-to-GCPW interconnects [6], [19]. Nevertheless, the worst-case return loss of the back-to-back connection remains at 19 dB in both CST and HFSS simulations.

As far as insertion loss is concerned, the differences between the two solvers in Fig. 5 reflect those in Fig. 4 with the discrepancies enhanced due to the back-to-back configuration. The worst-case insertion losses are again predicted at the end of the band and amount to 0.79 dB in CST and 0.87 dB in HFSS calculations. These values are well within the range of simulated and measured back-to-back transitions, e.g., between SIW and CPW [17] and SIW to GCPW [19]. This confirms our earlier statement that the loss of power due to radiation out of the interconnect is of no concern.

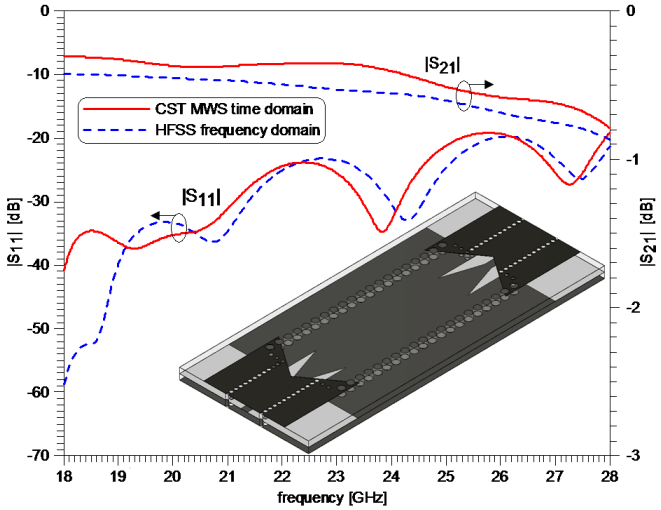

Fig. 5 Performance comparisons between CST and HFSS for the wideband SIW-to-stripline interconnect of Fig. 4 in a back-to-back arrangement.

IV. Conclusion

The new broadband interconnect between SIW and stripline presents a viable option for applications in which a medium power level within SIW has to be transferred to a TEM type transmission line. The designed prototype is shown to perform well over a 43.3 percent bandwidth centered at 23 GHz. Return and insertion losses of 24 dB and 0.44 dB, respectively, demonstrate excellent performance in comparison with other known interconnects involving SIW and, e.g., microstrip, CPW, or GCPW. All dimensional and substrate parameters are presented, thus providing the design engineer with valuable guidelines. Moreover, the operation of the interconnect is explained in terms of field plots that highlight the functions of individual circuit elements as the electromagnetic wave propagates through the transition. The performance of a back-to-back configuration of this interconnect compares well with simulated and measured results of SIW transitions to microstrip and coplanar waveguide.

ACKNOWLEDGEMENT

The authors wish to acknowledge funding for this work by the Graduate School Computational Engineering in Darmstadt, Germany and the Natural Science and Engineering Research Council of Canada.

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