

Broadband Interconnects Between Coplanar Waveguide and Substrate Integrated Waveguide for Dense Packaging and Integration

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Abstract — Two new interconnects between coplanar waveguide (CPW) and substrate integrated waveguide (SIW) are introduced and studied. Contrary to previously published interconnects, the new ones are shorter and require less space on the printed-circuit board. Thus they are ideally suited for dense packaging and integration. The first one is a regular interconnect that runs the slots of the CPW directly into the SIW. It is straightforwardly designed and achieves 26 dB return loss over a 10 GHz bandwidth centered at 23 GHz. The second interconnect is of the inverted type. It is 43 percent shorter than the first one over the same frequency range and at the same return loss level. Experimental results conducted at back-to-back transitions agree well with theoretical predictions. The shortest inverted interconnect achieves a measured back-to-back return loss of better than 18.5 dB over the entire frequency range with a maximum insertion loss of 1.28 dB. The comparative values of the regular back-to-back CPW-to-SIW prototype are 23 dB and 1.0 dB, respectively.

Index Terms — Integrated circuit interconnections, integrated circuit measurements, dielectric substrates, wideband.

I. INTRODUCTION

Since its inception in the early two thousands [1], substrate integrated waveguide (SIW) technology has been the focus of intensive investigation, design and prototyping activities [2]. For measurement purposes or active component integration [3], interfaces between SIW and other printed-circuit transmission lines are necessary. Such interconnects must provide adequate return loss and minimum insertion loss over the entire mono-mode bandwidth of the SIW.

Interconnects between SIW and microstrip are common, e.g. [4], but transitions to grounded CPW [5], [6], regular CPW [7], [8], and coplanar strip and slotline [9] have also been reported. Common to such interconnects is the fact that they require a certain amount of space on the board to provide a broadband transition to SIW.

This paper focuses on two CPW-to-SIW interconnects that are geared towards dense packaging and integration. Both regular and inverted [10] interconnects are presented. The regular CPW-to-SIW interconnect connects the center conductor of the CPW to the top metallization of the SIW. It is short due to the fact that the CPW slots are directly run into the SIW. An inverted interconnect is obtained by connecting

the CPW's center conductor to the bottom plate of the SIW. This is achieved by an extra set of small via holes. In comparison to the inverted interconnect presented in [10], this one is 62 percent shorter and provides similar performance.

II. INTERCONNECT DESIGNS

For the simplicity regarding the following SIW-to-CPW interconnect designs and discussions, both interconnects described in this paper make use of RT/Duroid 6002 substrate with $\epsilon_r=2.94$, $\tan\delta=0.0012$, substrate thickness $h=0.508$ mm, metallization thickness $t=17.5$ μm , and conductivity $\sigma=5.8\times 10^7$ S/m. The frequency range of interest is fixed from 18 GHz to 28 GHz, and the cutoff frequency of the SIW is 14.5 GHz. For the CPW, the center conductor of the 50 Ω line is 3.1mm wide and its slot widths are 0.15 mm. Via diameters and center-to-center spacing of the SIW are chosen as 0.61 mm and 0.866 mm, respectively.

Fig. 1 shows the field configurations in SIW and CPW as well as the connections required to achieve a regular or inverted interconnect. In Fig. 1a, the fundamental TE_{10} mode in the SIW is converted to the CPW mode by connecting the top plate of the SIW to the center conductor of the CPW. This connection is inverted in Fig. 1b that connects the bottom plate of the SIW to the center conductor of the CPW. The same field configuration is obtained in the CPW, albeit with opposite phase.

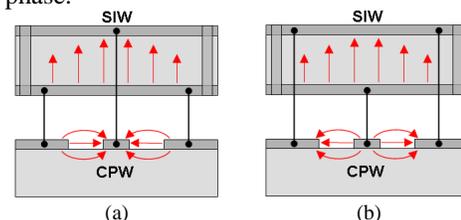


Fig. 1. Electric fields in SIW and CPW and connections required to obtain a regular (a) and inverted (b) interconnect.

A. Regular CPW-to-SIW Interconnect

The easiest interconnect between CPW and SIW is obtained by running the slots of the CPW directly into the SIW and

tapering the ground plane and vias over the length of the transition which is indicated as L_{trans} in the inset of Fig. 2. Thus the only design parameter is L_{trans} whose initial value is one quarter of the CPW wavelength (2.58 mm) at the midband frequency of 23 GHz. After a slight adjustment in the time-domain solver of CST, the length is adjusted to $L_{trans}=2.96$ mm.

Fig. 2 shows a performance comparison between the time-domain solver of CST and the frequency-domain solver HFSS. Good agreement between the results is obtained. The maximum insertion loss of this interconnect is 0.45 dB for both CST and HFSS simulations, and the worst-case return loss is 26 dB (CST at 28 GHz).

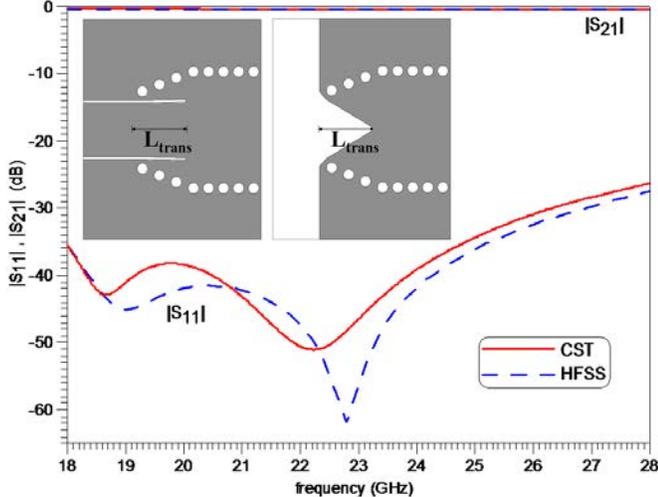


Fig. 2. Performance comparison between CST and HFSS of regular CPW-to-SIW interconnect according to Fig. 1a. Inset: Top (left) and bottom (right) metallization.

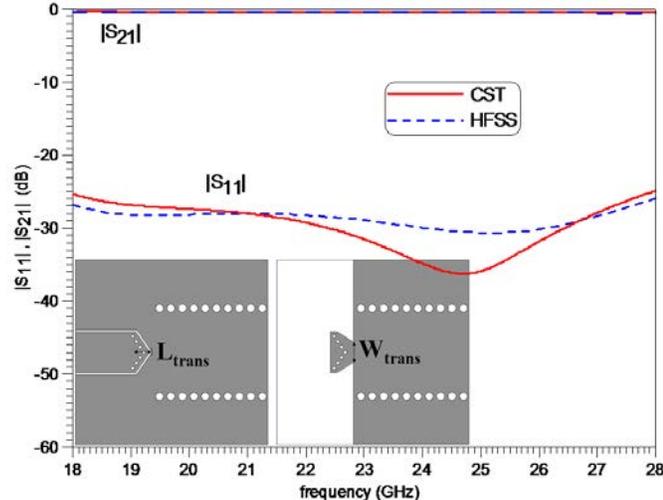


Fig. 3. Performance comparison between CST and HFSS of inverted CPW-to-SIW interconnect according to Fig. 1b. Inset: Top (left) and bottom (right) metallization.

B. Inverted CPW-to-SIW Interconnect

The inset in Fig. 3 shows the top and bottom metallization of the inverted interconnect. It combines the two slots of the CPW at a 45-degree angle and adjusts the positions of the

small vias (via diameters of 0.25 mm and center-to-center spacing of 0.5 mm) accordingly. The design is carried out by a parametric analysis of transition length L_{trans} and width W_{trans} and results in $L_{trans}=1.24$ mm and $W_{trans}=1.46$ mm. After fine optimization, the final length is obtained as $L_{trans}=1.68$ mm. Note that even after length adjustment, this transition is significantly shorter than the regular one.

The frequency-dependent performance of the inverted interconnect is shown in Fig. 3 where a good agreement between CST and HFSS is observed. The minimum return loss is better than 26 dB between 18 GHz and 28 GHz, and the maximum predicted insertion loss is 0.55 dB (worst cases of both simulations).

III. EXPERIMENTAL RESULTS

Since the SIW port is not directly accessible with measurement equipment, it is common practice to verify such interconnects in a back-to-back arrangement. The following figures display the measured performances of the two interconnects introduced in Section II as well as photographs of their top and bottom metallization. Note that no attempts have been made to optimize the length of the SIW between the two interconnects. The back-to-back circuits have simply been prototyped by mirroring the single interconnects of Fig. 2 and Fig. 3. During measurements, the circuits have been accessed by a universal test fixture, and all other transitions and connectors for measurements with a vector network analyzer have been de-embedded using TRL calibration standards.

Fig. 4 shows photographs, simulated and measured performances of the regular interconnect that runs the slots of the CPW straight into the SIW. The simulated response by CST is in reasonable agreement with measurements. The level of the experimental result agrees very well with simulations except for the slight increase in return loss at 22.5 GHz. Nevertheless, the measured return loss is better than 23 dB over the entire 10 GHz bandwidth. The maximum measured insertion loss is 1 dB which agrees well with the prediction of 0.45 dB for a single transition in Fig. 2.

Fig. 5 compares the performance predicted by the time-domain solver of CST with that obtained by measurements for the inverted interconnect. The overall agreement is reasonable, but the number of measured reflection minima (as in the previous measurements) seems to indicate that small reflections between the test fixture ports influence the measurements. Over the entire bandwidth, the measured return loss is better than 18.5 dB with its minimum occurring at 27.2 GHz. The maximum insertion loss is 1.28 dB which is a reasonable value considering the predictions of 0.55 dB for a single interconnect in Fig. 3.

Table I compares the results of this work with respect to minimum return loss, maximum insertion loss and space requirements. According to the simulations, the inverted interconnect is as good as the regular CPW-to-SIW interconnect, except for slightly increased losses. However, it

is 43 percent shorter than the regular one and thus is well suited for dense packaging of SIW systems when integrated with other transmission line technologies. (Note that the width of the main SIW including via holes is 7.36 mm.) The measured return loss of the back-to-back connection of the inverted interconnect is slightly worse than that of the regular one but would still be acceptable considering the smaller footprint.

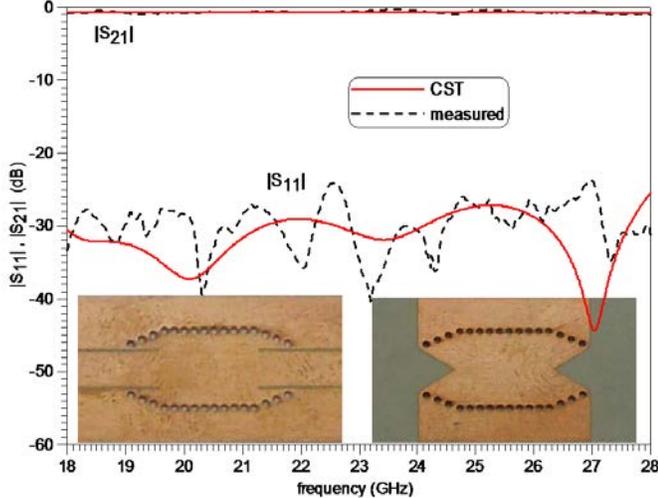


Fig. 4. Photograph (top and bottom), measured and simulated performances of the back-to-back regular CPW-to-SIW interconnect according to Fig. 2.

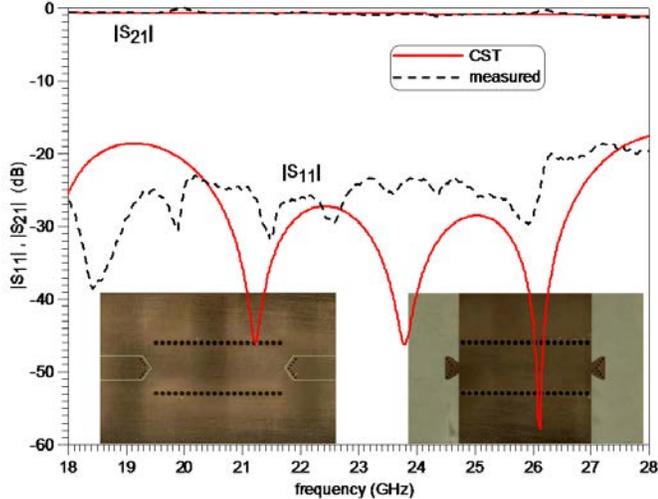


Fig. 5. Photograph (top and bottom), measured and simulated performances of the back-to-back inverted CPW-to-SIW interconnect according to Fig. 3.

TABLE I. PERFORMANCE AND LENGTH COMPARISON BETWEEN DIFFERENT CPW-TO-SIW INTERCONNECTS

Interconnect	Regular	Inverted
Min RL (dB) single (simulation)	26	26
Min RL (dB) back-to-back (measured)	23	18.5
Max IL (dB) single (simulation)	0.45	0.55
Max IL (dB) back-to-back (measured)	1.0	1.28
Length (mm) single	2.96	1.68

IV. CONCLUSIONS

Two new short CPW-to-SIW interconnects, a regular and an inverted one, are presented. It is first demonstrated that the inverted interconnect presents a viable option compared to the regular counterpart. Secondly, measurements on the back-to-back prototypes over a frequency range of 18 GHz to 28 GHz show that the inverted interconnect performs comparably with the regular one with only slightly reduced return loss and increased insertion loss. Thirdly, by comparing the two different interconnect types, it is obvious that the inverted interconnect requires 43 percent less space on the printed-circuit board and thus is better suited for dense packaging and integration.

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