

A Wideband MMIC Low Noise Amplifier with Series and Shunt Feedback

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Abstract—A two-stage MMIC low noise amplifier design is presented using series and shunt feedbacks to achieve simultaneously low noise, input matching and gain flatness performances across the frequency range of 4 to 12 GHz. The amplifier fits into a small die of $2 \times 1 \text{ mm}^2$, and achieves a flat gain of 20 dB and a minimum noise figure of 1.5 dB.

Keywords—MMIC, LNA, Low noise amplifier, Noise figure

I. INTRODUCTION

Modern radio telescope receivers demand low noise performance as well as wide operational bandwidths. The Atacama Large Millimetre Array (ALMA) radio telescope will cover the bands from 31 to 950 GHz [1]. This frequency range is divided into 10 bands, where each band requires a front-end receiver. The down-converted Intermediate Frequency (IF) for each band is 4 to 12 GHz. A two-stage MMIC Low Noise Amplifier (LNA) design for the IF band is demonstrated by the series inductor feedback at the FET source to optimize the noise matching and return loss[2], and the shunt RC feedback between the drain and gate to tune the gain flatness. This work is to explore the design of a simple and compact two-stage MMIC LNA at X-band.

II. AMPLIFIER DESIGN

This IF LNA has to fit into a small size of $2 \times 1 \text{ mm}^2$ with all of the matching networks and DC bias components. GaAs $0.15 \mu\text{m}$ pHEMT FETs with a gate width of $2 \times 100 \mu\text{m}$ are used. Two-stage LNA architecture can be adopted with lumped elements to minimize the elements' size. A common challenge in LNA design [3, 4] is to match the input stage to achieve the lowest noise figure while simultaneously obtaining a good input return loss. This is due to the fact that the optimum reflection coefficient Γ_{opt} for the minimum noise figure of FETs is not the same as the conjugate input reflection coefficient S_{11}^* of FETs. Luckily, S_{11}^* can be tuned or shifted closer to Γ_{opt} by feedback techniques and matching circuits.

The series feedback technique is exploited to shift S_{11}^* . A simple way is to use a series inductor at the FET's source. Fig. 1 shows the simulation results of a FET with a series feedback inductor and DC bias circuits (not including any matching networks). Adding a proper inductance of 265 pH at the FET's source, the FET's S_{11}^* shifts closer to Γ_{opt} . Note that Γ_{opt} changes little. This indicates that the FET with the inductor at the source has the similar minimum noise figure as before. The series feedback inductor also improves the stability of the FET as shown in Fig. 1, where the stability circle shifts further towards the outside of the Smith Chart.

The shunt feedback technique and its influence on the FET

performance are also investigated. Fig. 2 illustrates the simulation results of the FET with a shunt RC feedback and DC bias circuits (not including any matching networks). In contrast to the series inductor feedback, the shunt feedback significantly changes Γ_{opt} and causes the FET's noise figure to increase. It is observed in Fig. 2 that the shunt RC feedback shifts both S_{11}^* and Γ_{opt} closer together. Gain characteristics of a FET and the FET with series or shunt feedbacks are compared in Fig. 3. Due to the increase of the series inductive reactance of the inductor with frequency, it causes the FET gain to roll-off faster as frequency increases. On the other hand, the capacitive reactance of the shunt RC circuit decreases with increasing frequency, thus providing a smaller feedback effect as frequency increases. Therefore the gain flatness can be tuned by adjusting the values of R and C.

When the matching networks are added at the input, inter-stage and output, the series and shunt feedback characteristics become more complicated as the frequency changes. Carefully tuning the matching networks and feedback components, one can achieve the LNA performance to meet specifications.

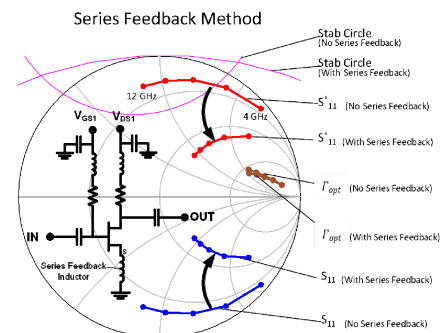


Fig. 1: Series inductor feedback applied at a FET source shifts S_{11}^* closer to Γ_{opt} for low noise matching.

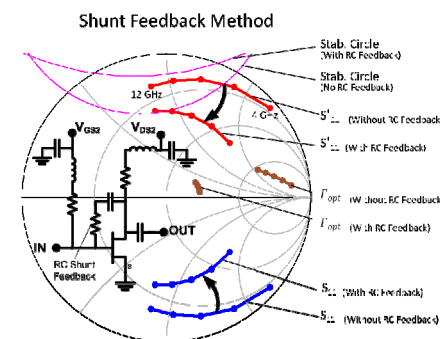


Fig. 2: Shunt RC feedback applied to a FET significantly changes Γ_{opt} and shifts both Γ_{opt} and S_{11}^* closer.

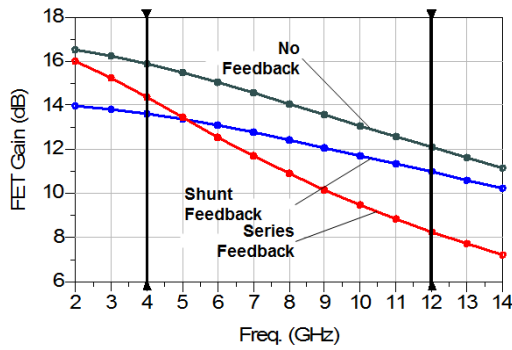


Fig. 3: FET gain compared to the FET with series or shunt feedback (FET gain results are obtained without any matching networks).

III. SIMULATED AND MEASURED RESULTS

The schematic circuit was optimized with the series feedback 1st stage and the shunt RC feedback 2nd stage. The cross coupling among the passive components were analyzed in Sonnet, and the network models were used to fine tune and optimize the LNA performance and ensure the LNA unconditionally stable. The 2-stage LNA design was fabricated on the 100 μm thick substrate as shown in Fig. 4. The LNA achieved more than 20 dB gain across the frequency band, and 0.4 dB/GHz gain flatness. The measured gain is plotted with the simulation results in Fig. 5. The measured and simulated noise figures are shown in Fig. 6 and are below 2 dB for most of the bandwidth. Measured and simulated input and output reflection coefficients are illustrated in Fig. 7 and Fig. 8. Simulated values are better than -10 dB in the band compared to measurements of -8 dB (input) and -10 dB (output).

IV. SUMMARY

The simulated noise figure, gain and gain flatness have a

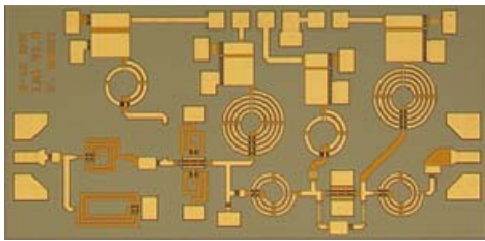


Fig. 4: The photo of a two-stage LNA chip (size 2x1 mm²).

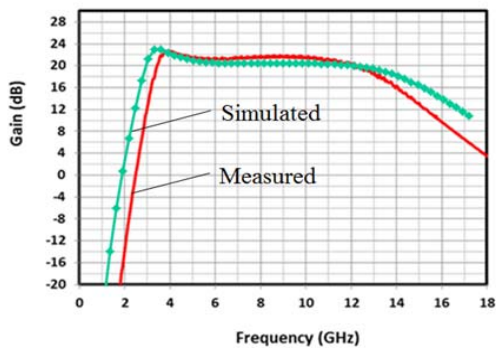


Fig. 5: The measured LNA gain comparison with the simulation gain.

good agreement with the measured results. The return losses show small deviations. Since the second stage has to manipulate the gain flatness and output return loss, and only the first stage can be dedicated to low noise and input return loss matching, it is hard for the two-stage amplifier to achieve the best noise figure close to the FET's minimum noise figure. If not limited by the chip size, adding a second stage FET for low noise matching, thus a three-stage LNA design, would achieve a better noise performance.

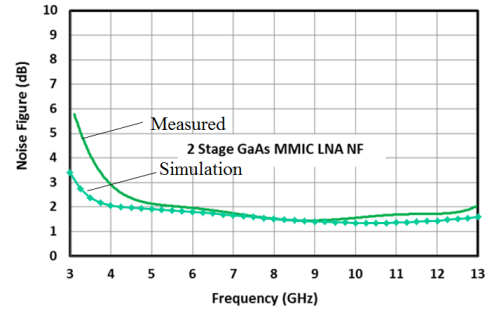


Fig. 6: Comparison between measured and simulated LNA noise figure.

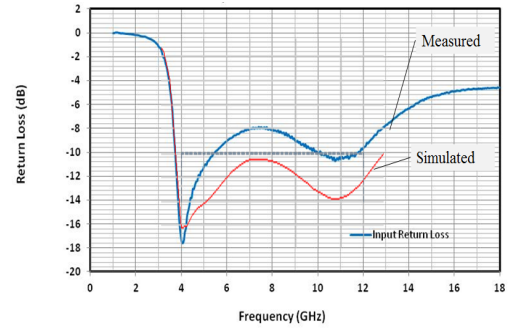


Figure 7: Measured and simulated input return losses.

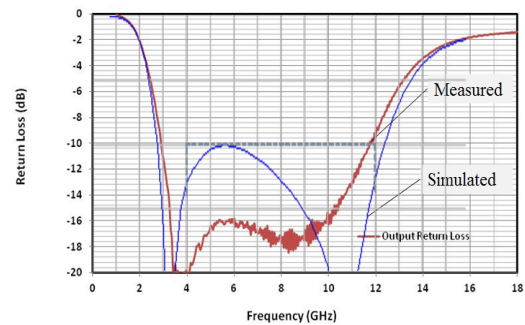


Fig. 8: Measured and simulated output return losses.

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