A Wideband Artificial Magnetic Conductor Yagi Antenna For 60-GHz Standard 0.13-µm CMOS Applications

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Abstract

This paper presents a low-cost wideband 60-GHz on-chip Artificial Magnetic Conductor (AMC) Yagi antenna utilizing a standard 0.13-µm CMOS process. The stand-alone Yagi antenna is designed based on a four-element topology in coplanar waveguide (CPW), using the top thick metal and metal layer M2. Furthermore, by designing and integrating an optimized AMC plane, which has a very wide fractional bandwidth of 31%, the radiation efficiency of this novel AMC Yagi antenna is significantly improved by more than 90% compared to a common Yagi antenna without AMC. The simulation results in HFSS also indicate that the impedance bandwidth (S_{11}<-10 dB) covers 53.5 GHz to 69 GHz, while an excellent peak power gain of -0.2 dBi is obtained. The proposed antenna occupies an area of 2.2 × 1.3 mm^2.

1. Introduction

The unlicensed 57-64 GHz millimeter-wave (mm-wave) band defined by FCC has attracted tremendous efforts in applications for short-range communication, and other standardization progresses, e.g. IEEE 802.11ad developed by the Wi-Fi Alliance. The aggressive advancement of the low-cost CMOS process has facilitated mass production of 60-GHz system-on-chip (SoC) circuits in recently reported works [1], [2].

In antenna applications, the antenna dimensions scale down to the millimeter range when the frequency enters the 60-GHz band, which makes antenna design more subtle and delicate. In a compact 60-GHz commercial product that favors a low-cost planar antenna instead of an expensive and bulky horn antenna, several mainstream antenna design approaches have been proposed in recent years, such as the multichip module (MCM) [3] and system-in-package (SiP) [4]. Nevertheless, these solutions are constrained by occupying large module size or high-cost packaging, and more critically, the interconnection between the 60-GHz integrated circuits (ICs) and the antenna introduces considerably larger loss at such high frequency.

To solve this dilemma, the approach of integrating antennas on chip has triggered large interest as it facilitates the monolithic integration of the entire RF system with the antenna and, therefore, significantly reduces the loss and expense. Moreover, the synthesized design of IC and antenna on one single chip makes impedance matching more controllable [5].

In this paper, a wideband 60-GHz CMOS on-chip Yagi antenna in 0.13-µm CMOS process is designed using the HFSS electromagnetic (EM) solver based on the finite element method (FEM). To improve the radiation efficiency, an angularly stable AMCs structure with optimized bandwidth is designed. The fabrication requirement is verified by the Cadence Assura tool.

Section II features the contemporary CMOS process. Section III presents the design and analysis of a wideband AMC structure. The synthesized design of the AMC Yagi antenna is presented in Section IV.

2. Antenna CMOS Process Features

Today's standard CMOS process provides multiple metal layers and, especially, one or two thick top metals with high conductivity as shown in Fig. 1, which makes passive components with high quality factor available. However, on-chip antenna design is still confronted with several main challenges. The first one is related to the silicon substrate with a low bulk resistivity of around 10 Ω-cm. This low resistivity provides a path for the antenna to dissipate its EM radiation and consequently decreases the radiation efficiency. Secondly, the high dielectric constant of ε_r=11.9 confines the radiated power in the lossy substrate, which furthermore deteriorates the radiation efficiency. On the other hand, the on-chip antenna layout needs to comply with the fabrication design rule check (DRC) which may cause more difficulties considering the spacing and maximum available width of the metals.

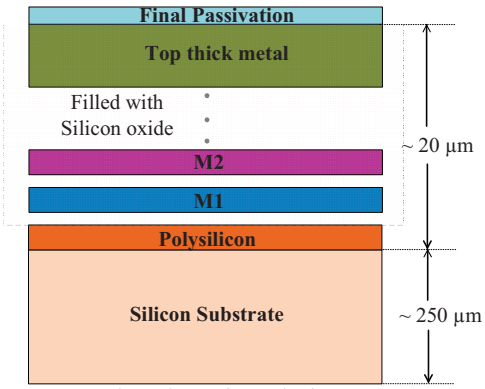

Fig. 1. Cross-section view of standard CMOS process with multi-layered structure.

In the CMOS process, the effective dielectric constant makes the effective wavelength much shorter than in vacuum. It can be quantified using the following quasi-static approximation [6]:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\left(\frac{h}{W}\right)\right)^{-1/2} + 0.04\left(1 - \left(\frac{W}{h}\right)\right)^2\right] \quad (1)$$

where the metal width W is considered to be smaller than the substrate thickness h (=250 μm) in most of on-chip antenna designs. Thus the wavelength λ_e is calculated as:

$$\lambda_e = \frac{c_0}{f\sqrt{\varepsilon_e}}. \quad (2)$$

For a typical 60-GHz design assuming W=5 μm, ε_e is calculated to be 6.88, and λ_e equals 1906 μm. Due to fringing effects, the actual physical size is even smaller.

3. Artificial Magnetic Conductor Design

To combat the above mentioned intrinsic issues of the CMOS process, an AMC surface, also known as high impedance surface (HIS) or perfect magnetic conductor (PMC), is employed. At some specific frequencies, the AMC operates with a reflection coefficient of Γ=+1, which means the phase of the reflected wave is zero compared with the incident wave. As a result, within some frequency range, the dissipation path to the substrate is blocked, and the EM radiation is enhanced.

As depicted in Fig. 2, a single AMC unit is based on the optimized structure of a Jerusalem cross frequency-selective surface (JC-FSS) [7] and implemented using metal M1 as the bottom layer. Moreover, the JC-FSS structure fulfills the strict DRC rules in the standard 0.13-μm CMOS process. The HFSS model employs a simple, fast and accurate method [8]; it consists of a waveguide port, two perfect electric conductor (PEC) walls and two perfect magnetic conductor (PMC) walls.

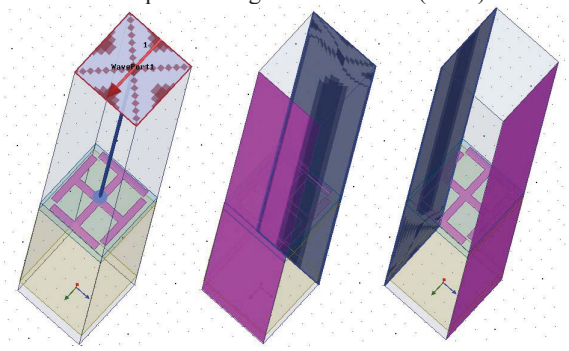

Fig. 2. AMC unit modeling in HFSS. Geometry and wave-port excitation (left), PEC walls (center), and PMC walls (right).

The dimensions of an AMC unit are dependent on the operating frequency and the effective wavelength. As shown in Fig. 3, the reflected phase of the AMC unit at 60 GHz is close to 0°, and the frequency bandwidth extends 50.5 GHz to 69 GHz over which the reflection phase varies from +90° to –90°, consequently a very wide bandwidth of 31% is realized. Furthermore, the reflection phase corresponding to the frequency range from 57 GHz to 64 GHz is well controlled between +35° and –51°.

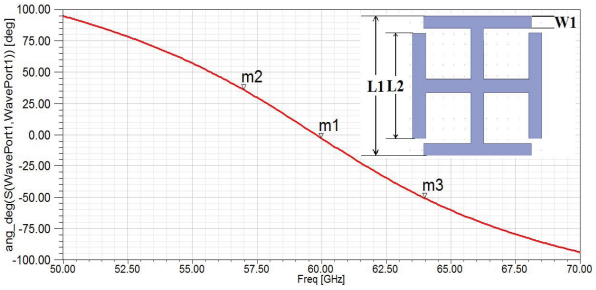

Fig. 3. Reflection phase versus frequency of AMC unit.

As depicted in Fig. 4, each AMC unit has its own equivalent distributed circuit components. The gap between unit cells determines the value of C_g on which the resonance frequnecy depends. The entire AMC structure can be analyzed by using a lumped-circuit model represented by a parallel RLC resonance circuit as shown in Fig. 4 (right). L_T is the total equivalent inductance, C_T stands for the total equivalent capacitance mainly contributed by the gap capacitance, the coupling capacitance between the metal traces, and the fringing capacitance. Moreover, R_T consists of the metal resistance, skin-effect resistance, and also the resistance of the silicon substrate.

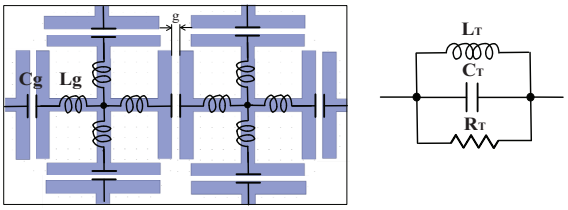

Fig. 4. AMC and its equivalent lumped-circuit model.

4. On-Chip AMC Yagi Antenna Design

Yagi antennas obtain higher directivity than other wire antennas and therefore are very suitable for 60-GHz applications with high path loss and strong atmospheric absorption. As shown in Fig. 5, the proposed Yagi antenna consists of a reflector implemented in metal layer M2, a driven element and two directors which are realized on the top thick metal layer. The off-chip differential signals are fed into the antenna driver through the ground-signal-signal-ground (G-S-S-G) probing pads, which are sperated by a pitch of 100 μm, and then into the coplanar waveguide (CPW).

The dimentions of L_1, L_2, L_3, L_4, S_1, S_2, S_3 are, respectively, 0.64 λ_e, 0.26 λ_e, 0.28 λ_e, 0.14 λ_e, 0.137 λ_e, 0.069 λ_e and 0.069 λ_e, following both the design principles in [9] and practical design trade-offs. An appropriate

TABLE I. PERFORMANCE COMPARISON WITH REPORTED WORKS

Type of Antenna	CMOS Process	Frequency	Bandwidth (S_{11})	Gain	Efficiency
AMC loop [8]	standard 0.18-µm	65 GHz	57-67 GHz	-4.4 dBi (Measured)	N.A.
2-element Yagi [10]	N.A.	60 GHz	53-65 GHz	-3.5 dBi (Simulated)	15.8%
This work	standard 0.13-µm	60 GHz	53.5 - 69 GHz	-0.2 dBi (Simulated)	19.6%

distance is kept between the AMC plane and the antenna as too close a promixty can only worsen the antenna's performance,due to the mutual coupling effects, instead of improving it. The layout area is 2.2 × 1.3 mm^2 including the G-S-S-G pads and the AMC plane.

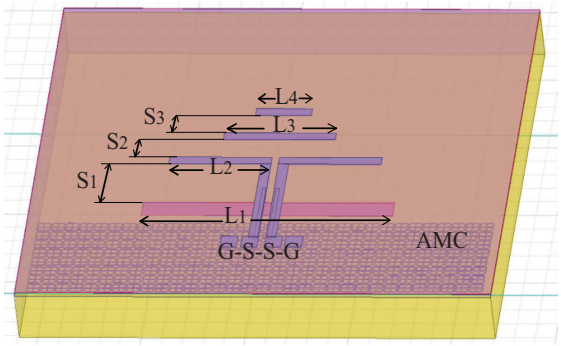

Fig. 5. On-chip AMC Yagi antenna in 0.13-µm CMOS.

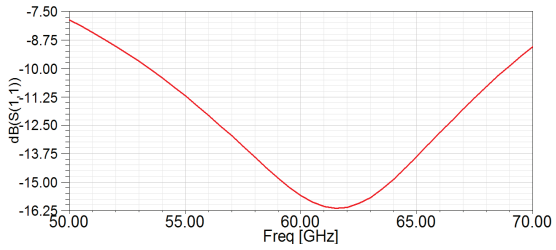

Fig. 6. S_{11} simulation versus frequency.

The input reflection coefficient in Fig. 6 shows that the 10-dB bandwith covers a range from 53.5 GHz to 69 GHz. The directivity is 6.83 dBi, and the radiation efficiency increases from less than 10% to 19.6%. The 3D and 2D radiation patterns are drawn in Fig. 7. The E-plane radiation exhibits a maximum gain of -0.22 dBi with a half power beamwidth (HPBW) of 92° around the 40° direction. Table I sumarizes the performance comparison with other state-of-the-art works. A special loop antenna with AMC is designed in [8], and [10] shows a 2-element Yagi antenna without AMC.

Summary

An integrated AMC Yagi antenna is designed for a standard 0.13-µm CMOS process and ready for fabrication. The radiation efficiency is greatly improved by the high performance AMC plane; consequently, a high power gain over a wide bandwidth is achieved.

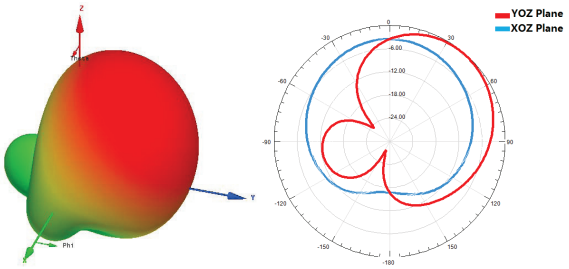

Fig. 7. 3-D and 2-D gain radiation patterns.

Acknowledgment

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