Full-Wave Analysis and Design of a Wideband GaAs pHEMT MMIC LNA

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***Abstract*—This paper presents the design of a wideband monolithic microwave integrated circuit (MMIC) low noise amplifier (LNA) using GaAs pseudomorphic high electron mobility transistor (pHEMT) technology. The flat gain of 30 dB ± 0.5 dB is achieved using a three-stage amplifier topology over 4-12 GHz. The minimum noise figure of 1.0 dB is achieved in a packaging chassis within the frequency band. In order to achieve such a low noise over a wideband, several bandwidth enhancement techniques are applied in the design. An inductive feedback at the source of the first stage results in a very wideband input matching ($|S_{11}| < -12$ dB) over 3-15 GHz. The gold wire bonds at the input and output of the chip are separately analyzed and modeled into matching networks to ensure wideband low noise behavior of the chip after packaging. This GaAs pHEMT LNA is suitable for radio astronomy receivers such as the Atacama Large Millimeter Array Band 3 IF warm amplifiers.**

Keywords—MMIC, LNA, wideband, low noise amplifier, GaAs pHEMT.

I. Introduction

Low noise amplifiers are critical components of radio receivers. In the case of the Atacama Large Millimeter Array (ALMA) Band 3 receivers [1], the incoming cosmic signals are collected by each of 15 m dish antenna in the array and fed to individual Band 3 cartridges (84−116 GHz). Inside the cartridge RF signals are down-converted by cryogenic SIS mixers to intermediate frequencies (IF) of 4−8 GHz in separate side bands for 2 orthogonal polarizations. The signals are amplified by cryogenic low noise amplifiers [2] and then output from the cartridge to a warm cartridge assembly where room temperature IF amplifiers are used to boost the signal power level to meet downstream digitizer requirements. Currently, the ALMA Band 3 receiver has an 8 GHz IF band width (2 side bands x 4 GHz) for each polarization. Increasing the IF bandwidth of operation would deliver significant benefit. For example, doubling the IF bandwidth while maintaining the signal to noise ratio would halve the required integration time during science observations of broadband astronomy sources and would increase the efficiency of wideband spectral line surveys. Expanding the IF bandwidth from 4–8 GHz to 4–12 GHz could be a very cost effective way to significantly improve ALMA Band 3 system performance [3].

Although discrete component approaches have traditionally been used for LNAs (including the present Band 3), GaAs MMIC technology is becoming a mature and reliable alternative which can provide a high reproducibility and low noise figure at low cost. The GaAs pHEMT process using 0.15 µm gate length with f_T = 90 GHz [4] and NF_{min} = 0.4 dB at 12 GHz is an appropriate choice for 4–12 GHz MMIC LNA design. In this work we describe the design of a three-stage feedback amplifier. Full-wave analysis is conducted to do EM simulation on the MMIC chip. In the 12 GHz frequency range packaging is critical for the MMIC chip to operate stably. Modeling of the packaging effect is part of this work. Generally, the wire bond connection degrades the performance as the frequency increases, which directly affects the input matching and the noise figure. Thus, the wire bond connections are modeled, simulated, and applied in the amplifier design. The chassis and DC bias circuit are carefully designed to avoid negative effects on the MMIC LNA performance.

II. Desing

The three-stage amplifier is designed based on GaAs pHEMTs with 0.15 µm gate length. The circuits are simulated by computer-aided design tools, and components are modeled in full-wave EM analysis.

A. First Stage

The first stage has the largest effect on the noise figure and input reflection coefficient of the LNA [5]. Careful design of the transistor size and configuration to increase the gain and lower the gate resistance will help improve noise performance. The gate resistor is a major thermal noise source at the input of the transistor. Gate metal is the smallest line feature in transistors. Given the gate finger width, the transistor having more gate fingers will have lower gate resistance than one with fewer gate fingers. Therefore, increasing the number of fingers by a factor of two helps reducing the gate resistance by half as the gate resistance is distributed [6]. Thus, a 4-finger transistor will have lower gate resistance than a 2-finger transistor if each gate finger width is the same.

For the first stage a 4×75 µm transistor is utilized for low noise and high gain. Fig. 1 shows the minimum noise figure over frequency for 2-finger and 4-finger transistors with a

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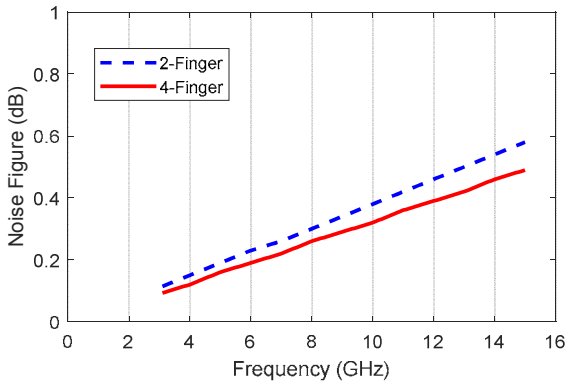

Fig. 1: Minimum noise figures of 2-finger transistor (solid red line) and 4-finger transistor (dashed blue line) with finger width of 75 µm. The drain voltage is 2 V and the drain current density is 100 mA/mm.

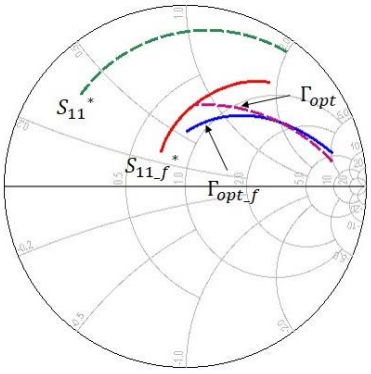

Fig. 2: S_{11}^* (dashed green line) and Γ_{opt} (dashed purple line) for a 4×75 µm transistor without feedback, $S_{11\text{-}f}^*$ (solid red line) and $\Gamma_{opt\text{-}f}$ (solid blue line) with feedback.

finger width of 75 µm. Although increasing the number of fingers lowers the minimum noise figure of the transistor, the best noise performance and the lowest input reflection cannot be achieved merely by impedance matching at the input. Thus, a source inductance feedback [7] is added to move S_{11}^* closer to Γ_{opt}. As shown in Fig. 2, not only S_{11}^* and Γ_{opt} get closer to each other, but they also move closer to the center of the Smith chart, making the impedance matching network design less complicated. Moreover, S_{11}^* has a shorter trajectory over the frequency band in the presence of the source inductance feedback, which is in favor of wideband impedance matching. A resistor is added at the drain loop of the transistor in order to stabilize the transistor at its operation bias point.

B. Second Stage

Although the second stage noise contribution is less than that of the first stage in cascade multistage amplifiers, its noise still needs to be minimized to lower the total noise figure. A 4×75 µm transistor is used in the second stage. A very short piece of microstrip line at the source can alter the input and output impedances for better matching. A resistor is used at the gate loop in order to add a small resistance to the circuit which helps to stabilize the amplifier. This resistor should be small to minimize the thermal noise effect on the noise performance. A drain resistor is also required for stabilizing the transistor at its operation bias point.

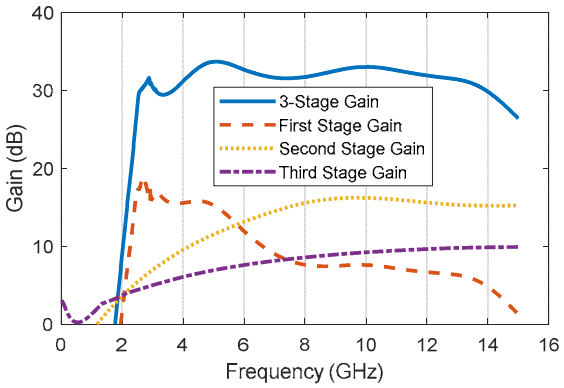

Fig. 3: Total gain of 3 stages and separated gains for each stage.

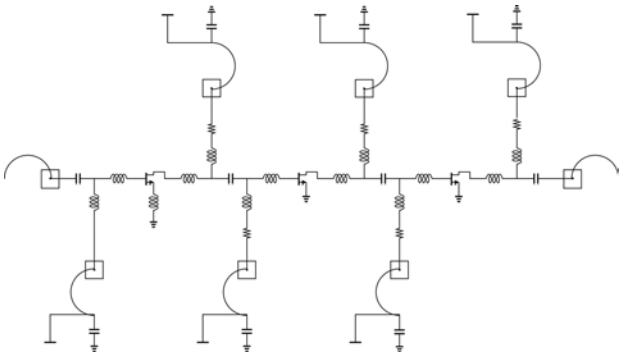

Fig. 4: Schematic diagram of the 3-stage GaAs pHEMT MMIC LNA.

C. Third Stage

The focus of the last stage is on low output reflection and gain flatness. The 2×75 µm device has less total gate width, which results in smaller gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}, and larger output resistance r_d [7]. These are good for output matching to 50 Ω and help extend the transistor gain roll-off to a higher frequency to compensate for the gain drop in the first and second stages. The third stage is designed to have a positive gain slope with frequency. This combination can balance the amplifier gain to make the gain flat over the frequency band. The separated gains of each stage and the total gain are plotted in Fig. 3.

The three-stage designs are put together in cascade. The inter-stage matching networks need to be tuned to make the best impedance transition from each transistor drain to the next gate. The whole circuit must be optimized for the lowest noise, flat high gain, and low reflection coefficients at the input and output. The schematic diagram of the 3-stage amplifier design is shown in Fig. 4.

III. EM Simulation

After laying out the entire circuit on a chip of size 3 x 1 mm^2,

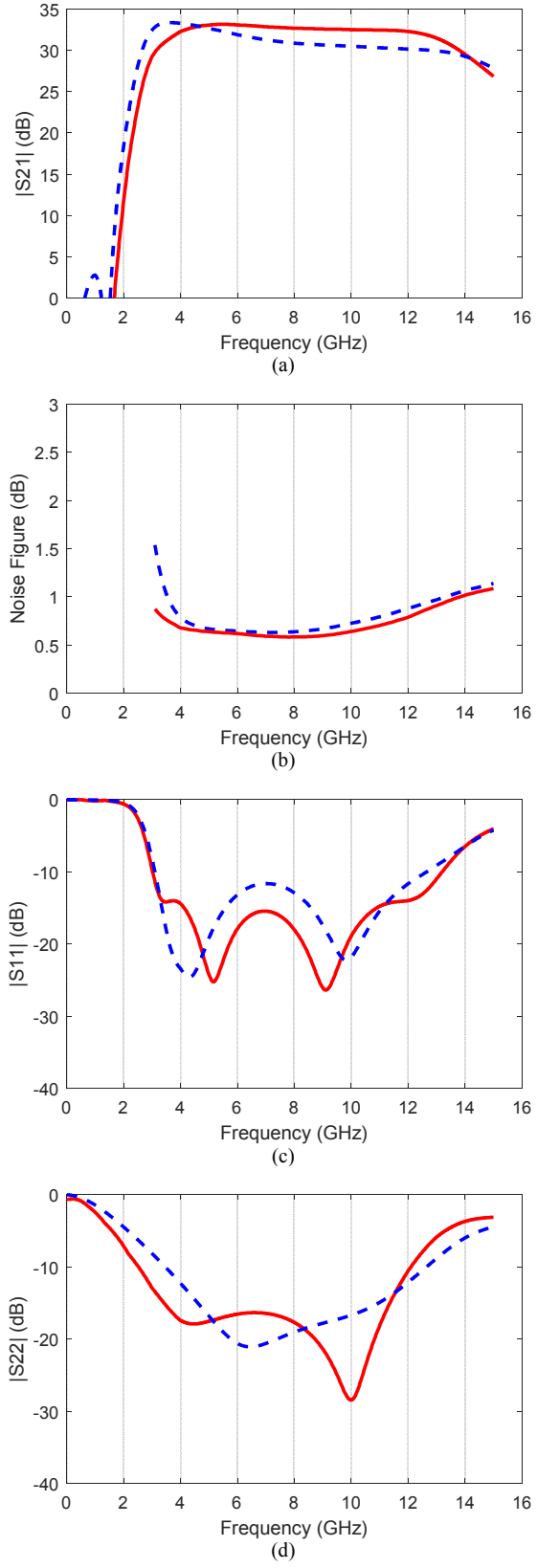

Fig. 5: The schematic circuit results (dashed blue lines) and EM simulated performance (solid red lines) for (a) LNA gain, (b) noise figure, (c) input return loss, and (d) output return loss.

each of the lumped components, such as spiral inductors, capacitors, resistors, and back visas, are modeled and analyzed in a full-wave EM simulation in order to include the loss from microstrip traces, parasitic capacitances of spiral inductors, and fringing fields of the MIM capacitors. All spiral inductors are separately simulated to confirm their self-resonance frequences are far above the operating frequency band. Element tuning in the full-wave EM simulations are the most time-consuming part of the design/optimization process.

Each section of the matching networks is EM modeled and tuned, changing the size of the lumped components and lengths of the microstrip lines to match to the schematic circuit results as much as possible. Finally, all matching networks are integrated with 3 transistors and EM simulated as one piece. The EM simulated chip results are shown in Fig. 5 in comparison with primary schematic results. Accurate full-wave EM modeling and analysis are critical to ensure that the circuit models embody all components characteristics and features, and to achieve good agreement between the fabricated MMIC chip and the designed performance.

IV. Wire Bond Model

When packaging MMIC devices, gold wires are used to bond from chips to input and output ports or DC bias circuits. Some of the DC decoupling capacitors are too large to be feasible on the limited chip size, so wire bonds are used to connect off-chip components. The bonded gold wires have

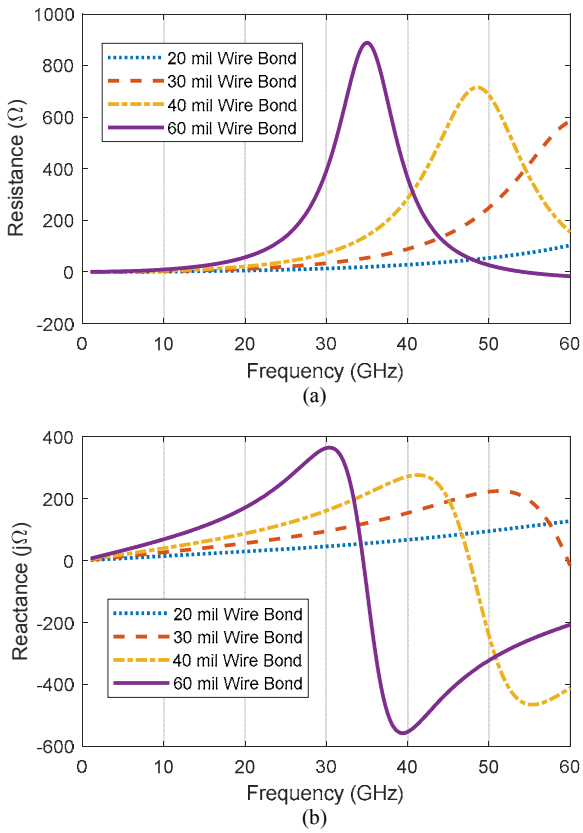

Fig. 6: Calculeted equivalent resistance (a) and reactance (b) for different wire bond lengths with 1 mil diameter from 1 to 60 GHz.

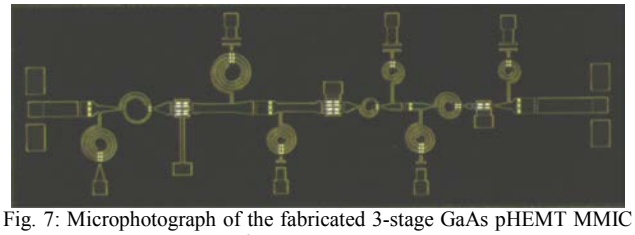

Fig. 7: Microphotograph of the fabricated 3-stage GaAs pHEMT MMIC LNA. Chip size is 3 × 1 mm^2.

high impedance in the gigahertz band and their inductive effect is significant as frequency increases. The design requires to include the wire bonds in the input and output matching networks and bias circuits.

In order to include the wire bonds into the design the profile of the parabolic wire bonds is modeled in a 3-D EM analysis tool and the *S*-parameters are extracted for different wire lengths and diameters. The calculated equivalent impedances over frequency of different bond wire lengths in terms of resistance and reactance are illustrated in Fig. 6. The longer wires have larger equivalent inductances. Note that due to the parasitic capacitance and the resistive metal loss, each wire has a self-resonance frequency at which the bond wires act as an open circuit and loses its ability to transfer the RF signal. This necessitates using wire bonds with a resonance frequency far above the highest frequency of the band in the circuit. For this work, wire lengths of 20 mil to 60 mil are used for input/output connections and DC biasing, and their self-resonance frequencies range from 60 GHz to 35 GHz.

An RT Duroid 5880 substrate with $\varepsilon_r = 2.2$ is used as the 50 Ω transmission lines at input/output ports for converting microstrip lines to coaxial connectors. Large value off-chip capacitors are mounted on the chassis to prevent the RF signal to leaking into the DC network and feedback into adjacent RF circuits.

V. Measurements

A microphotograph of the fabricated MMIC LNA chip is shown in Fig. 7. It is measured at room temperature within a packaging chassis designed specifically for C-to-X band applications.

The measured and simulation gains are shown in Fig. 8 (a). The measured gain is about 3 dB lower than the simulated one. Other MMIC circuit designs shared on the same wafer processing show the same 3 dB lower measured gain than their expected gains. This is due to the transconductance of the transistors being lower than the facility's model and is caused by a process variation in electron mobility in the wafer fabrication.

The noise figure of the packaged MMIC LNA is measured using a noise figure analyzer. The measured performance and simulated results are compared in Fig. 8 (b). The measured noise figure is about 0.5 dB higher than the simulation result. It should be noted that the measured noise figure included the losses of the SMA connector, the transition from coaxial to microstrip line, and then to chip. The lower than expected transconductance dominates the discrepancy between the measurement and simulation.

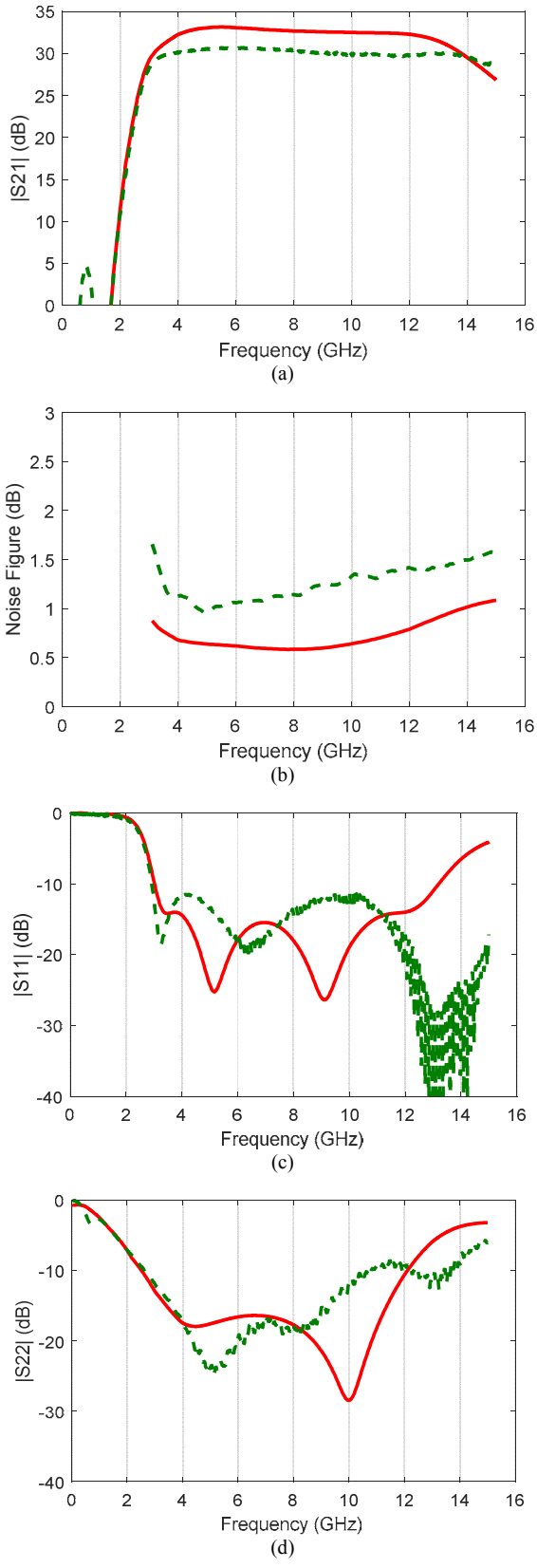

Fig. 8: The measured results (dashed green lines) and EM simulated performance (solid red lines), (a) LNA gain, (b) noise figure, (c) input return loss, and (d) output return loss.

The simulation results and input/output reflection coefficients measured in the chassis are illustrated Fig. 8 (c) and 8 (d), respectively. This wideband MMIC LNA has a low input reflection coefficient ≤ -12 dB from 3 to 15 GHz, inclusive of the SMA connector, the transition, and gold wire bond. Therefore, there is no need of an isolator at the input of this MMIC LNA in the radio receiver, thus avoiding a source of extra loss/noise. The output return loss meets the requirement, also including SMA connectors, the transition, and gold wire bond. Adding resistors in the biasing lines can help stabilize the transistor operation and it is better to place the resistor between the DC pads and the inductors to prevent the resistor's thermal noise from entering the signal path. Since the inductors have a high impedance at high frequencies, they can obstruct resistor noise getting into the circuits.

VI. Conclusion

Full-wave EM analysis of the laid-out MMIC circuits is essential for achieving a reliable design and good consistency between the design and the fabricated MMIC. The simulated *S*-parameters and noise figure of this GaAs pHEMT MMIC LNA agrees well with the measured results. For a wafer process achieving the expected transconductance, we would get 3 dB additional gain and a lower noise figure than the measured one. Even with this lower transconductance the realized MMIC LNA packaged in the chassis achieved wideband performance and a minimum noise figure ~1.0 dB below 8 GHz and a maximum noise figure of 1.4 dB at 12 GHz. This GaAs pHEMT LNA has good reflection coefficients, flat gain, and, to our knowledge, has the lowest noise figure for a packaged GaAs pHEMT MMIC LNAs in the same frequency band.

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