UHF Wideband GaAs MMIC LNA

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Abstract—A wideband room temperature UHF-band MMIC low noise amplifier based on 0.15 µm pHEMT GaAs technology is presented. The amplifier achieves about 30 dB gain over a fiveoctave frequency range from 300 MHz to 1.5 GHz with minimum noise of 0.55 dB at room temperature. The two-stage amplifier utilizes an on-chip gain equalizer at the output and has a gain flatness of 3 dB over the 5:1 band in the fully packaged enclosure.

Keywords—MMICs, low-noise amplifiers, GaAs pHEMT, wideband.

I. INTRODUCTION

Radio receivers cover very wideband frequency ranges from several hundred megahertz to gigahertz and require amplifiers to provide a consistent low noise performance over the entire band. The simultaneous low noise, wideband, high gain specifications present a challenge in the LNA design as it is a key component for technology development of wideband receivers. The GaAs pseudomorphic high electron mobility transistor (pHEMT) has good low noise performance, and the MMIC technology is available at reasonable cost to produce high numbers of MMIC LNAs with consistent and reproducible amplifier performance.

Various UHF low noise amplifier designs have been presented based on hybrid microwave integrated circuit (MIC) technology that offer very low noise and wideband performance [1], [2], [3]. However, high volume reproducibility and their larger size is a constraint in phased array receivers, which require integration of a large number of elements. On the other hand, InP MMIC LNAs offer great integration and the best noise performance [4], [5], especially in cryogenic receivers. However, the LNA cost would increase quickly, especially when large numbers of amplifiers are needed to build a large receiver array. GaAs MMICs with high level of integration, moderate price and good low noise performance are the best candidate for a large array of radio receivers at room temperature. Previously published MMIC low noise amplifiers that can cover the 300-1500 MHz frequency range, with more than 25 dB gain, had above 0.7 dB noise figure [6], [7], and some LNAs with lower noise did not cover the wide frequency band of interest with simultaneous noise and gain requirements [8], [9], [10].

In this work, a two-stage LNA is designed for wideband, low noise and high gain performance. In order to achieve a flat gain over the 5:1 bandwidth ratio, an on-chip gain equalization mechanism is employed at the LNA output. The MMIC LNA chip was designed and fabricated on the WIN 0.15 µm pHEMT process.

II. CIRCUIT DESIGN

The main challenge in designing a wideband LNA in the UHF band is to achieve optimum noise matching over the 5:1 bandwidth ratio as well as matching the input impedance to a standard 50 Ω interface. The authors of [4] had to trade off input matching as high as -5 dB to achieve low noise performance. This is due to the fact that the transistor input impedance is very high, like an open circuit, at low frequencies, but the impedance significantly decreases at 1.5 GHz. To overcome the high impedance issue, we can use a large number of transistor fingers to increase the gate capacitance. This can also help to reduce the device noise resistance, R_n , as well as decrease the device input/output impedances and relaxing the requirement of large value components for matching networks. An RC feedback network can be used at the first stage to achieve the desired input impedance matching. Fig. 1 shows the input impedance change before and after the RC feedback network is added in. As can be seen, the optimum noise reflection coefficient Γ_{opt} and transistor S_{11} move closer to the 50 Ohm centre point on the Smith Chart. Fig. 2 shows the minimum noise increasing due to thermal noise injected by the feedback resistor. The amount of feedback can be tuned for optimum noise and bandwidth performance.

Fig. 3 shows the schematic of the LNA where adding the RC feedback network changes the input impedance to be closer to 50 Ω without the need for any input matching component except for the large DC decoupling capacitor. The first stage includes a



Fig. 1. Optimum noise impedance (red) and conjugate of S_{11} (blue) without feedback (solid line), with 5 k Ω and 2 pF RF feedback (dashed line), and with 2 k Ω and 2 pF RF feedback (dotted line).



Fig. 2. Minimum noise figure before and after adding RF feedback network.



Fig. 4. Gain equalizer: (a) proposed circuit; (b) equivalent load at low frequencies; (c) equivalent load at high frequencies.

large number of transistor fingers while the second one utilizes a smaller size transistor. The first stage uses an off-chip 50 nH inductor, and the second gate is biased via a 50 k Ω resistor for stability purposes. The inductances of the wire bonds were included in the design phase. Although adding the RC network improves noise matching and input impedance matching, the resistor's thermal noise contributes extra noise to the overall amplifier noise. Decreasing the feedback resistance provides better input matching but it results in higher thermal noise at the input of the transistor as well as lower gain for the first stage. Thus, it was optimized to the lowest possible noise with acceptable input reflection of about -10 dB.

III. GAIN EQUALIZER

Increasing the size of transistors in the first stages lowers the input impedance for better results of a very high gain at 300 MHz; however, gain rolls off significantly over the 5-decade frequency range. Therefore, in order to have a flat gain, we employ the on-chip gain equalizer circuit Z_e in Fig. 4a at the output of the second stage to limit the low frequency gain with minimum change at the high end of the frequency band. Fig. 4a shows the proposed circuit that consists of a series RLC network. The L_e and C_e values are designed to have a resonance frequency at the low end of the band (f_{low}) , which results in the small load impedance of $(Z_e = R_e) ||Z_0$ as shown in Fig. 4b and reduces the amplifier gain. As the frequency increases, the series RLC network impedance shifts towards an open circuit as shown in Fig. 4c, and the amplifier sees a higher equivalent load impedance of $(Z_e \rightarrow \text{open}) || Z_0$ as that corresponds to a higher output power gain. This equalizer circuit adds a positive gain slope with respect to increasing frequency. It is worth noting that the value of R_e is optimized for wideband performance and higher gain.

IV. RESULTS

Fig. 5 depicts the simulation results of the LNA. The amplifier achieves 30 dB gain over the bandwidth of interest with better that 10 dB return loss. The noise figure of 0.4 dB is predicted for this design. The LNA is designed to be biased at 2.2 V, with total bias current of 150 mA.



V. CONCLUSIONS

A wideband UHF-band MMIC low noise amplifier is designed based on GaAs pHEMT technology and large finger number devices. The LNA design adopted an on-chip gain equalizer circuit to flatten the gain across the 5:1 band width. Results show good gain and S_{11} and S_{22} performances over the operating bandwidth between 300 MHz and 1.5 GHz with acceptable noise performance. Some deviation from the simulation was initially experienced in the low frequency noise mainly due to the limited accuracy of models for very large number of gate fingers and related device size. The final measured results along with chip photographs will be presented at the conference.

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