Design and packaging analysis of a Ku band high gain GaAs MMIC LNA

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***Abstract*— A Ku band high gain low noise amplifier (LNA) designed using the 0.15 µm GaAs pHEMT process is presented in this paper. Three types of connections between the MMIC (monolithic microwave integrated circuit) LNA chip and the input port are compared in terms of their loss and noise contribution. To achieve a very low noise figure, a gold bonding wire is used as a series matching inductor in the input matching circuit due to its minimal loss. The tolerance of the LNA related to the wire shape variation is also studied. EM-circuit co-simulation analysis of the LNA package is also carried out to detect higher mode resonances before fabrication. This MMIC LNA is designed, fabricated and packaged in a gold-plated chassis. The whole LNA module is measured through a coaxial system from 9 to 18 GHz. The gain ranges from 35 to 39.5 dB and the noise figure is lower than 1.75 dB. By de-embedding the noise contribution of the RF connector, the noise figure of the MMIC chip is lower than 1.26 dB from 9 to 18 GHz. Compared with other reported LNAs using a similar GaAs MMIC process in similar frequency bands, the presented LNA chip and module shows superior noise figure at room temperature.**

Keywords*— *GaAs HEMT, Ku band, low noise amplifier, MMIC, LNA, RF packaging.

I. INTRODUCTION

Low noise amplifiers (LNAs) are important components in RF/microwave applications such as satellite communication, mobile communication, automotive radar & imaging systems, radio astronomy receivers, and for many other applications. The design techniques of LNAs have been intensively investigated in the past decades and it is still an active research topic. Most LNAs presented in academic papers report their noise figures that are measured as a die on a wafer. However, the results measured on the wafer cannot be directly used in practice. Moreover, for LNAs measured on-wafer, they may require series inductors in input matching networks, which is realized by on-chip inductive components such as spiral inductors [1-3] or long series microstrip lines [4, 5]. The loss of on-chip inductive components severely deteriorates the noise performance.

This paper studies and compares the noise influences of on-chip inductive components and off-chip gold bonding wires. By utilizing component(s) with low loss, the noise figure of the designed LNA can be reduced. A high gain LNA designed on a 0.15 µm GaAs pHEMT process is presented where a gold bonding wire is used as a matching inductor at its input to improve noise performance. The noise influence of the bonding wire is studied and high tolerance of the LNA related to wire shape variation is verified. Furthermore, the load of the first stage of this LNA is designed to be capacitive in order to facilitate the design of the input impedance matching network. Inductive peaking [6, 7] is applied in this low noise amplifier to improve the gain. The LNA is fabricated and packaged inside a gold-plated copper chassis, which is proved to supress higher mode resonances up to the Ku band. The measured results show competitive performance compared with other Ku band GaAs MMIC LNAs. The designed LNA is shown to be a desirable candidate for Ku band receivers [8, 9].

II. CIRCUIT DESIGN

Fig. 1 illustrates the schematic diagram of the LNA. In order to achieve high gain and low noise, a cascading four-stage transistor design in common-source configuration was employed and a source degeneration inductor was used in the first and second stages [10-12].

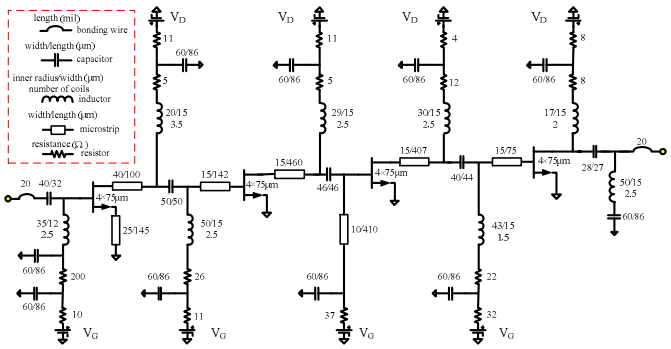


Fig. 1. Schematic diagram of the low noise amplifier.

As mentioned in [13-16], the load of the first stage should be capacitive to facilitate the optimal input matching condition. Therefore, the shunt inductor between stage 1 and 2 should have a large value and the series inductor should have a small value. In stages 2, 3 and 4, the inductors for the inter-stage matching networks were designed to optimize the gain performance by forming inductive-peaking structures [6, 7].

A. Loss at Input Matching

Inductors are usually required in the input matching network. The finite quality factor of an inductor brings loss to the circuit. The noise figure of an LNA is quite sensitive to this loss, so the loss should be minimized. Although applying some techniques such as using large size transistors in the first stage [17] can reduce the required inductance to reduce the loss, many

LNAs still utilize series input inductors. This inductor can be realized by use of an off-chip gold bonding wire, or an on-chip inductive component. Therefore, for the LNA packaging and measurement, there are three different types of connections for integrating and measuring MMIC LNAs with RF connectors:

1) The first one uses a gold bonding wire as a series inductor to connect the MMIC to the PCB microstrip and then to RF connectors at the input and output. The gold bonding wire is also used for impedance matching, thus on-chip series inductors can be avoided or their values can be reduced.

2) The second type is for the MMIC LNA chip to be measured with a RF probe station. In this case, the MMIC LNA chip usually needs on-chip series inductors for impedance matching. Therefore, the microstrip on PCB, bonding wire and coaxial connectors are not needed.

3) For the third type, the MMIC LNA is completely designed with all necessary RF components on chip, including on-chip inductor(s) for input matching as in the second type. Then the chip should be packaged. Therefore, extra bonding wires are required at the input and output for connecting the chip to the coaxial connectors. In order to compensate the extra inductance of the bonding wire at the input/output of the chip, two specially designed capacitive pads should be applied to form a wideband lowpass filter (LPF). The LPF is required to have very low reflection coefficient over the required bandwidth. Compared to the first type, this bonding wire is not included into the matching circuit of the MMIC chip.

These three types of input connection are illustrated in Fig. 2 where coaxial connectors are omitted for simplicity.

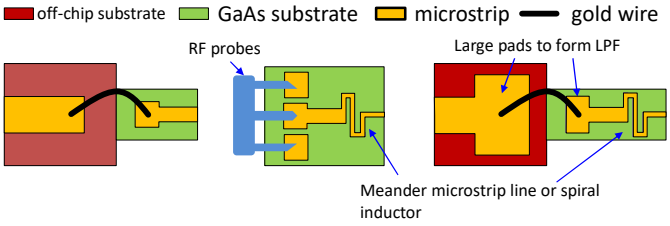


Fig. 2. Three types of input connection, (a) first type, (b) second type, (c) third type.

The noise figures of the three connection types were obtained by EM simulation as shown in Fig. 3. The cross-section of the gold wire was circular with a diameter of 25 μm, while the cross section of the on-chip line was a 3 μm × 15 μm rectangle. Meanwhile, the equivalent inductance of the gold wire (in the first type) and a meander line inductor (in the second and third types) were kept similar (390 pH). Due to a larger cross-sectional area and substrate dielectric loss of the on-chip inductor, the noise figure of the first type was 0.05 dB lower than that of the second type. For the third type, the LPF with bonding wire adds extra noise to the LNA. Therefore, the first type contributes the least noise to the circuit. The MMIC LNA should be co-designed with the bonding wire as the part of the series inductor for impedance matching and connection to 50 Ω PCB microstrip. In this way, the loss of the input network was minimized.

B. LNA Simulation

The MMIC LNA chip was designed and simulated in Advanced Design System (ADS) and CST software. The noise model and S-parameters of the GaAs pHEMT transistors provided by the wafer foundry were used in this design. Transistors with 4 × 75 μm gate width were selected and biased at 30 mA. The gain parameters (maximum available gain, maximum stable gain and optimal matching impedance) and noise parameters (NF_{min}, optimal noise impedance and equivalent noise resistance) were all considered suitable in this frequency band. The finite element method (FEM) simulator in ADS was employed for EM simulation of the chip. Gold bonding wires, which were 20 mil long, were simulated in CST. Then, its model was built and used in the ADS schematic.

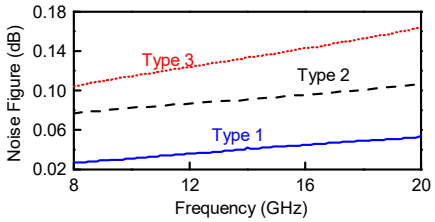


Fig. 3. Simulated noise figures of three connection types as shown in Fig. 2.

Fig. 4 shows the simulated performance of the low noise amplifier. From 10 GHz to 18 GHz, S11 and S22 were lower than -11 dB. The gain was higher than 42 dB and the noise figure was lower than 1.2 dB. Since the gain was very high, the stability was carefully investigated. Both the K factor and μ factor were larger than 1 as shown in Fig. 4 (c), so the LNA design is unconditionally stable. Furthermore, the normalized determinant function [18] and driving point admittance method with Kurokawa's oscillation condition were also applied to check stability.

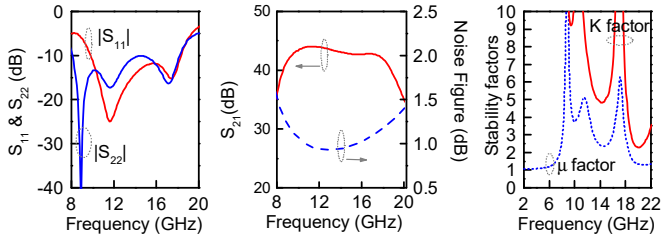
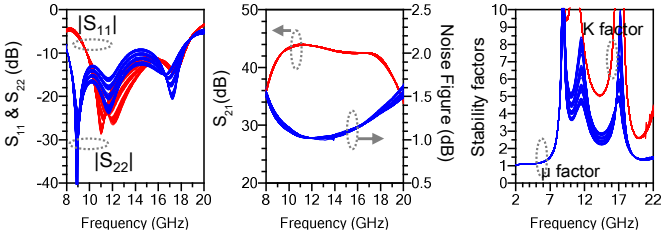


Fig. 4. Simulated performance of the LNA chip, (a) S11 and S22, (b) S21 and noise figure, (c) stability factors.

Since it is difficult to precisely control the length, height and shape of the bonding wires during fabrication, the tolerance of the proposed design was considered. Therefore, the physical parameters of the bonding wire were swept in CST and the simulated results were used in EM-circuit co-simulation to obtain the dependence on the LNA performance. The locations of bonding joints, position of highest point, length and height of a wire were swept, resulting in 100 different wire shapes. The curve length of each wire shape ranges from 15 mil to 25 mil. The simulated performance of the LNA is shown in Fig. 5. It is clear that the performance variation due to different wire shapes is acceptable.

A gold-plated copper chassis was used to package the MMIC chip. The important feature of the chassis was to prevent higher order mode resonances. A time-domain simulation as described in [19] was carried out with CST. Energy balance is defined as $|S11|^2+|S21|^2$, of which a spike corresponds to a higher order mode at the frequency. The EM simulation, whose first spike occurs at 23 GHz, proves that the chassis can suppress the higher mode resonances above the Ku band.



(a) (b) (c)

Fig. 5. Simulated performance of the LNA chip with different bonding wire shapes, (a) S_{11} and S_{22}, (b) S_{21} and noise figure, (c) stability factors.

III. MEASUREMENT

The LNA chip was designed and fabricated on 0.15 μm GaAs pHEMT process. The MMIC LNA chip (size: 3000 μm × 1000 μm) was packaged inside a gold-plated chassis.

Fig. 6 shows the photographs of the LNA module and bare chip. The DC bias was fed through a DC connector and some off-chip bypass components. Gold wires and microstrips were used to connect the chip and RF connectors (K connectors). It should be noted that the input microstrip should be kept as short as possible or it would increase the loss/noise to the LNA module.

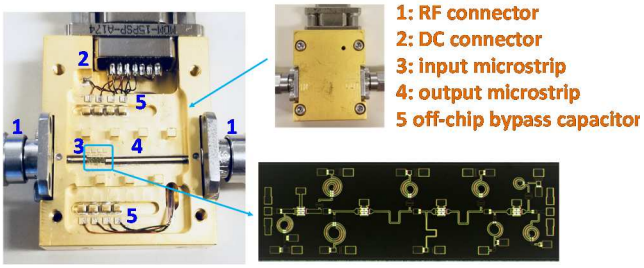
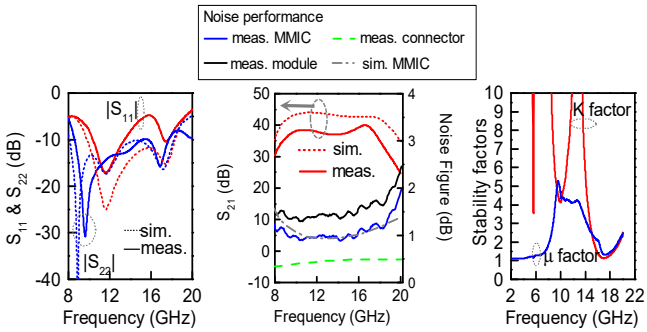


Fig. 6. A photograph of the LNA module and MMIC chip.

The noise figure of the LNA module was measured with an Agilent noise figure analyzer N8975A. The bias voltage was adjusted to obtain the minimal noise figure. The S-parameters of the LNA module, under the minimal noise bias voltage, were measured with an Anritsu vector network analyzer. The measured performances are shown in Fig. 7. From 9 to 18 GHz, S11 changes from -15 dB to -5 dB and S22 was lower than -10 dB. The gain was higher than 35 dB. The S11 and gain were offset by several dB from the simulation results, but the profiles of the curves have similar variations with frequency. By tuning the DC voltages, the S21 can be higher than 40 dB but the noise figure would increase. This higher gain bias was not selected since its noise measure was higher. The noise measure is defined in [20] and is valuable in designing multistage circuits/systems [21]. The measured K factor and μ factor are shown in Fig. 7 (c). The noise figure of the LNA module was lower than 1.75 dB. In addition, the loss of the K connectors was measured. Then, the noise figure of the chip with the input bonding wire was obtained by de-embedding the noise of the K connector, as shown in Fig. 7 (b) by the solid blue line. It ranges from 0.89 dB to 1.26 dB.

Table 1 shows a comparison with some Ku band LNAs from academic papers using a similar GaAs pHEMT MMIC process. LNAs in [1, 22-24] and the LNA in [25] when measured at room temperature present their noise figures measured on the wafer, which are all higher than this designed LNA. One of the reasons may be the loss issue discussed in Section 2.A. This designed LNA also has highest gain over the whole octave bandwidth with moderate DC power consumption (140 mW).



(a) (b) (c)

Fig. 7. Measured S parameters, (a) S11 and S22, (b) S21 and noise figure, (c) stability factors.

IV. CONCLUSION

The design and analysis of a Ku band high gain LNA module were presented in this paper. The losses of different input connection types were compared. A gold bonding wire as both a matching inductor and connection to the input was included in the MMIC design to have lowest possible noise contribution. Meanwhile, the influence of the wire shape and length variation was investigated and proved to be acceptable in the LNA module assembly. The MMIC chip was fabricated by the 0.15μm GaAs pHEMT process and packaged inside a gold-plated copper chassis. The chassis was carefully investigated to ensure higher order mode suppression with EM simulation before chassis fabrication and LNA chip packaging. The whole LNA module, containing connectors, off-chip capacitors, off-chip PCB microstrips, is measured through a coaxial system. The final results show low noise and performance advantages compared with relevant published LNAs.

TABLE I. COMPARISON WITH SIMILAR GAAS PHEMT MMIC LNAS

Ref.	Freq. (GHz)	NF (dB)	S_{11} (dB)	S_{22} (dB)	S_{21} (dB)	DC (mW)	Process gate length
[1]	7 ~ 14	1.1 ~ 1.6	<-10	<-10	24.5~ 27.5	90	0.15μm
[22]	12~18	1.2~1.8	-20~ -5	-14~ -9	21 ~ 23	250	0.13μm
[23]	12~18	1.22~1.8	< -8.5	< -7.7	25~ 27.5	275	0.13μm
[24]	12~20	1.23~1.51	<-10	<-10	20.1~ 28	227.5	0.15μm
[25]*	8 ~ 18	1.5 ~ 2.1	-5 ~ -20	-5 ~ -20	22 ~ 27	44	0.15μm
This work	9~18	0.89~1.26	-17~ -5	-36~-10	35~39.5	140	0.15μm

* Room temperature measurement

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