Quasi-Static Analysis of Circular Signal Tapping Pads

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***Abstract*—In this paper, analytical expressions for the capacitance of signal tapping pads are derived using a quasistatic analysis. The theory is validated by comparing our results with those of a commercial software package. As an application-oriented example, a new lowpass filter design is proposed which combines the signal tapping pads with lumped inductors.**

***Index Terms*—Lowpass filters, microstrip circuits, quasistatic analysis, signal tapping pads.**

I. Introduction

MICROSTRIP circuits invariably incorporate transmission line discontinuities of one type or another. The effect of these discontinuities is predominant at microwave frequencies. In high-density RF circuits, it is important to estimate the influence of the discontinuities so that RF noise can be controlled. Some of the common forms of microstrip discontinuities are open ends, gaps [1], steps in width, right angled bends [2], T-junctions and cross-junctions [3]. Since discontinuity dimensions are usually much smaller than the guided wavelength, they may be modeled quasistatically as lumped element equivalent circuits, e.g., [4].

Other important discontinuities in the RF circuit are signal tapping pads and dc biasing pads. Generally, these pads are isolated from the ground, as shown in Fig. 1, and will introduce capacitive reactance to an RF circuit. The field in the slot, between the pad and ground, can cause (very small) radiation. In high-speed circuits, the capacitance of the pads will create a time delay for signal propagation and, therefore, the capacitance created by the pads must be known in order to design compensatory circuits to overcome time delays. Since displacement currents dominate the conduction currents, cutting slots into the pads will not reduce their reactance. Therefore, and in combination with lumped inductors, filter sections can be designed using tapping pads.

The quasistatic evaluation of the open-end discontinuity capacitance has been treated in [1]. In this paper, we present the quasistatic analysis for the capacitance of a dc biasing pad.

II. Formulation

If the substrate height h is small (c.f. Fig. 1), the voltage between the pad and the ground plane is uniform with respect to the radial direction r in region I $(0 < r < a)$. It depends on the z direction only. In the slot, region II $(a < r < d)$, the potential function satisfies Laplace's equation

$$\nabla^2 V = 0 \tag{1}$$

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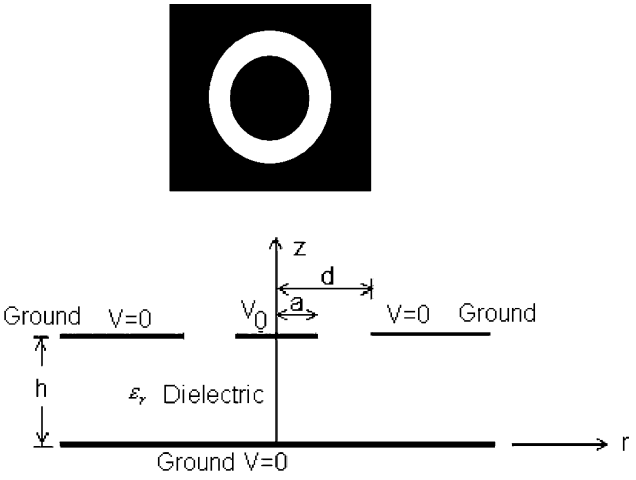

Fig. 1. Top view and cross section of circular signal/dc tapping pad.

with boundary conditions

$$V = V_0, \quad \text{at } r = a \text{ and } z = h \tag{2a}$$

$$V = 0, \quad \text{at } r = d \text{ and } z = h \tag{2b}$$

$$V = 0, \quad \text{for all } r \text{ and } z = 0. \tag{2c}$$

Due to the symmetry, the angular variable ϕ can be neglected, and the general solution to (1) is

$$V(r,z) = [b_1 I_0(\lambda r) + b_2 K_0(\lambda r)]\,[c_1 \cos(\lambda z) + c_2 \sin(\lambda z)] \tag{3}$$

where b_1, b_2, c_1, and c_2 are amplitude constants, which can be eliminated by using the boundary conditions (2a) to (2c); K and I are modified Bessel functions.

Since the solution for the potential in the region II is

$$V_2(r,z) = V_0 \left[\frac{I_0(\lambda d)K_0(\lambda r) - K_0(\lambda d)I_0(\lambda r)}{I_0(\lambda d)K_0(\lambda a) - K_0(\lambda d)I_0(\lambda a)}\right] \frac{\sin(\lambda z)}{\sin(\lambda h)} \tag{4}$$

where $\lambda = \pi/(2h)$, the electric field in region II can be written as

$$E_2(r,z) = \frac{V_0 \lambda}{\sin(\lambda h)} \times \left\{ \frac{I_0(\lambda d)[K_1(\lambda r)\sin(\lambda z) - K_0(\lambda r)\cos(\lambda z)]}{I_0(\lambda d)K_0(\lambda a) - K_0(\lambda d)I_0(\lambda a)} \right. \left. \frac{K_0(\lambda d)[I_1(\lambda r)\sin(\lambda z) - I_0(\lambda r)\cos(\lambda z)]}{I_0(\lambda d)K_0(\lambda a) - K_0(\lambda d)I_0(\lambda a)} \right\}. \tag{5}$$

Similarly, the voltage and electric field in region I are $V_1 = V_0 z/h$ and $E_1 = -V_0/h$.

From the energy stored in the structure

$$W = \frac{1}{2} C V_0^2 = \frac{1}{2} \varepsilon \int_v |E|^2 dv \tag{6}$$

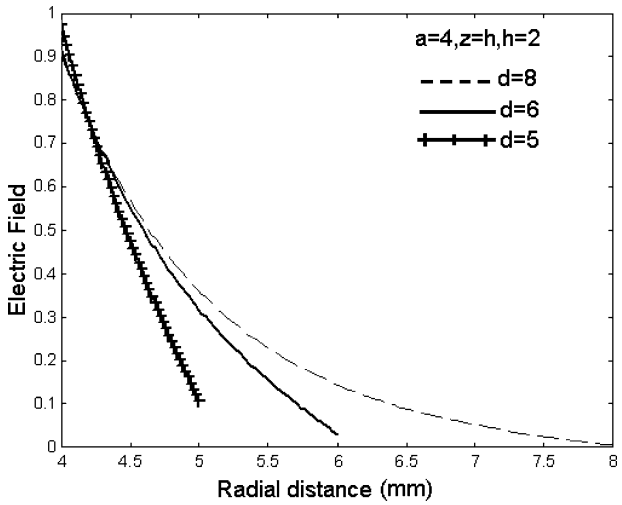

Fig. 2. Variation of the electric field in region II at $z = h$ for $d = 8$, 6, and 5 mm.

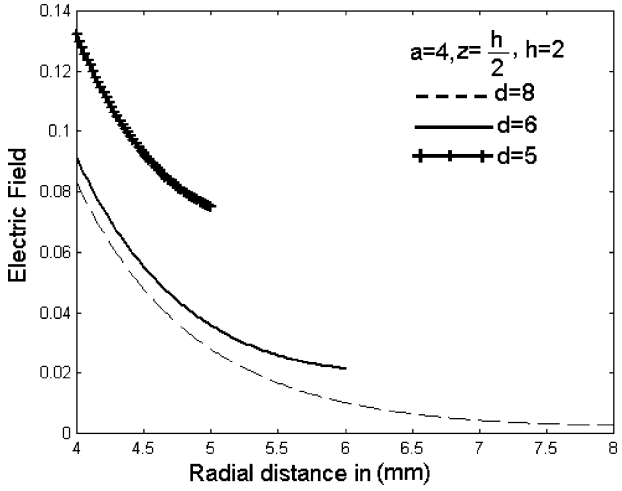

Fig. 3. Variation of the electric field in region II at $z = h/2$ for $d = 8$, 6, and 5 mm.

the capacitance of the pad can be derived as

$$C = \varepsilon \frac{\pi a^2}{h} + \frac{2\pi\varepsilon}{V_0^2} \int_{r=a}^{d} \int_{0}^{h} r|E_2|^2 ds. \tag{7}$$

III. Results

For an example of $a = 4$ mm, $h = 2$ mm, $\varepsilon_r = 10$ and three parameters of the outer pad radius, d, Fig. 2 shows the electric-field variation in radial direction (region II) at height $z = h$. While it is obvious from (4) that the potential between the two ground planes at $r = d$ vanishes, Fig. 3 demonstrates that this is not the case for the electric field in (5) due to the nonzero voltage gradient. Only if the slot width increases in radial direction (e.g., $d = 8$ mm in Fig. 2), then the field at $r = d$ decreases as expected.

Fig. 3 displays the electric field at half the distance between the lower and upper ground plane $(z = h/2)$ for the three different slot gaps d. This confirms the presence of an electric field between the two ground planes.

TABLE I
Comparison of Capacitance (in pF) Obtained With This Theory and IE3D. $a = 1$ mm, $h = 0.8$ mm, $\varepsilon_r = 10$

a=1mm, h=0.8mm, ε_r=10.

Gap (mm)	This Theory	IE3D 0.5GHz	IE3D 1 GHz	IE3D 2 GHz	IE3D 3 GHz
0.2	0.76	0.74	0.73	0.75	0.78
0.4	0.67	0.67	0.67	0.69	0.70
0.6	0.63	0.61	0.63	0.65	0.68
1.0	0.62	0.60	0.63	0.64	0.68
3.0	0.60	0.63	0.63	0.65	0.67
5.0	0.59	0.63	0.63	0.65	0.67

TABLE II
Comparison of Capacitance (in pF) Obtained With This Theory and IE3D. $a = 1$ mm, $d = 1.2$ mm, $h = 1.0$ mm

a=1mm, d=1.2mm, h=1.0mm.

Material	ε_r	This Theory	IE3D 1 GHz	IE3D 2 GHz
PTFE	2.35	0.16	0.19	0.19
Quartz	3.8	0.27	0.28	0.29
GaAs	13.13	0.91	0.87	0.90
InP	12.61	0.88	0.85	0.86
High-Res. Silicon	11.8	0.81	0.81	0.82
Alumina	9.9	0.69	0.66	0.68

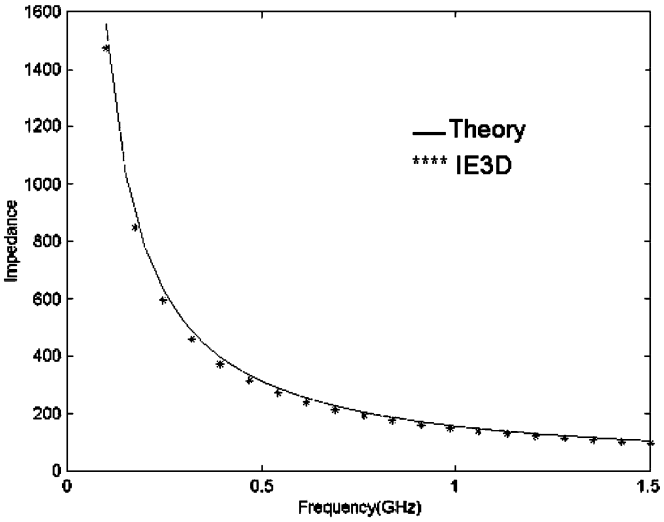

Fig. 4. Impedance of the pad; comparison between this theory and IE3D.

In Table I, the analytical quasistatic formula (7) is compared with numerical results obtained with the commercial EM simulator IE3D, version 9. The capacitance is derived from the impedance parameters calculated from IE3D by defining the port against the pad. Good agreement between the quasistatic approach and IE3D is demonstrated up to 3 GHz. A similar comparison (not shown here) was carried out for the range of dimensions: it is concluded that the capacitance is accurately predicted as long as $h/a < 1.5$, even if h/d is as high as 10. If $h/d < 0.5$, then the model works very well up to $h/a = 2$. The variation with respect to the substrate material is shown in Table II and demonstrates very good agreement for permittivities up to 13.

Impedance values obtained with IE3D and with the quasistatic theory are compared in Fig. 4. The dimensions are: $a = 1.4$ mm, $h = 0.8$ mm, gap width $d - a = 0.6$ mm,

Fig. 5. Lowpass filter designed with quasistatic approach of tapping pads.

and $\varepsilon_{\rm r} = 10$. Very good agreement is demonstrated. As for comparison of CPU times with IE3D, it depends on how large a ground plane is chosen surrounding the pad and how many via holes are selected to actually connect that plane to the lower (infinite) ground plane (c.f. next example). On the average, the quasistatic formulation (7) has been at least three times faster than IE3D.

Finally, the capacitance calculation according to (7) is used in a circuit design problem. We focus our attention on obtaining an initial design for a fifth-order lowpass filter at 3 GHz. Lumped-element capacitances and inductances are readily calculated from standard filter theory. We then use (7) to determine parameters a and d in order to match the theoretical capacitance values with those of the practical pads. The circuit is shown in Fig. 5. The area around the pads is grounded through via holes, and the inductors are mounted within the elevated strip line. The vertical bends of the strip line were included in the EM simulation (using the commercial package MEFiSTo-3D) but not in the filter design process.

The performance of this filter is depicted in Fig. 6. The dashed lines show the results of a circuit-based simulation (ADS) using the capacitances extracted from (7). The solid lines are obtained from a full-wave electromagnetic field solver (MEFiSTo-3D) and show a minimum return loss of 13 dB and 20 dB rejection between 5.2 GHz and 12 GHz. Note that the cutoff frequencies calculated with both methods are in good agreement which verifies the capacitance calculations via (7). Although this is not (and was not meant to be) a final design, it clearly demonstrates the value of the quasistatic theory in dealing with the capacitances of circular signal tapping pads.

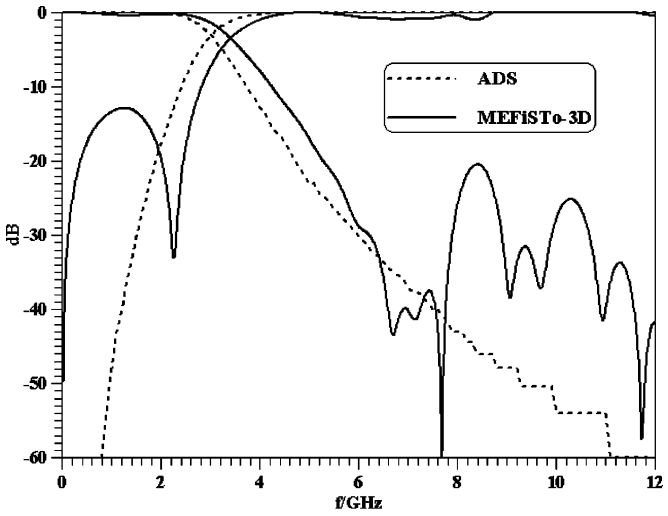

Fig. 6. Performance of initial lowpass filter design using tapping pads. Circuit-based (dashed lines) versus EM-based (solid lines) simulation.

IV. Conclusion

A simple analytical expression for the capacitance of circular signal tapping pads is derived using a quasistatic analysis. The theory is validated by analysis of the pads with the commercial software package IE3D. Very good agreement is demonstrated. The quasistatic analysis is applied to the design of a new lowpass filter, which combines the signal tapping pads with lumped inductors. Its performance simulation demonstrates the value of the quasistatic theory in dealing with initial design problems involving the capacitances of circular signal tapping pads.

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