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Broadband coplanar-waveguide and microstrip low-noise amplifier hybrid integrations for K-band substrate integrated waveguide applications on low-permittivity substrate

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Abstract: K-band low-noise amplifier (LNA) chips are integrated in low-permittivity coplanar waveguide (CPW) and microstrip (MS) structures and are interconnected with substrate integrated waveguide (SIW) ports for direct applications in hybrid SIW technology. A commercial Hittite LNA chip is employed, and special transitions provide the interface between CPW or MS and SIW. The LNA with SIW-to-CPW transitions achieves more than 20 dB gain between 18 and 26.5 GHz, and input/output return losses remain below 10 dB between 21.5 and 26.5 GHz. Related design values for the LNA integration within SIW-to-MS transitions are: the gain is greater than 21 dB; the input/output return loss is better than 12 dB over the entire frequency range. Measurements of a back-to-back SIW-to-CPW transition are provided to put these values in perspective. The maximum noise figures are measured to be better than 4.6 and 4.2 dB, respectively, between 18 and 26.5 GHz. A comparison with measurements performed with an evaluation board supplied by the LNA manufacturer demonstrates successful K-band LNA chip integrations within CPW/MS and SIW.

1 Introduction

Owing to significant research efforts over the last decade [1, 2], substrate integrated waveguide (SIW) technology has reached a certain degree of maturity that permits many traditional waveguide components to be replaced by planar SIW circuits [1]. Especially in the millimetre-wave frequency range and for relatively wide bandwidth applications, SIW has a distinctive advantage over microstrip (MS) technology because of its considerably lower loss factor and self-shielding feature [2, 3]. Excellent progress has been made in the design of SIW circuits, especially in passive SIW structures and subsystems, including antennas, for example, [2–4].

Integration of SIW technology with non-linear and/or active devices, however, has caught on slowly. Only recently varactor and PIN diodes have been used to switch and tune SIW filters [5, 6] or Schottky diodes to develop SIW mixers [7, 8]. Amplifiers have mostly been used in circuits that are separated from the SIW antenna and/or filter components [9, 10].

Only a few attempts have been made to integrate amplifiers within SIW technology. In [11], an X-band amplifier is integrated in MS technology between two SIW sections. It achieves 10 gain and 10 dB return losses at the SIW input and output ports over most of the X-band frequency range. Additional via holes within the SIW sections are used as matching elements. The transmission line connected to the amplifier is an MS line that is DC-separated from the SIW circuit. Since the MS-to-SIW transitions affect the amplifier performance, the entire circuit, including amplifier and transitions, requires proper modelling capability in order to obtain a good match. Thus matching procedures will have to be repeated if a different amplifier chip is used.

A power amplifier is integrated using transitions from SIW to conductor-backed coplanar waveguide (CPW) with side-wall via holes, also called grounded CPW (GCPW) [12]. The design achieves a maximum gain of 13.3 dB at 3.62 GHz and also uses additional via holes within the SIW to match the amplifier. While the transition between SIW and GCPW is broadband (2.4–4.0 GHz), results for the SIW power amplifier are only presented for a single frequency. Therefore, the design is believed to be limited in achievable bandwidth, judging from the fact that GCPW is likely to excite and propagate a higher-order waveguide mode at higher frequencies.

More recently, a different integration is presented in [13], where instead of SIW-to-MS or SIW-to-GCPW interconnects, transitions from SIW to half-mode corrugated SIW (HMCSIW) are used. This approach yields a

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fluctuating gain performance and return loss values up to 5 dB over a bandwidth from 3.8 to 6.5 GHz.

As in conventional waveguide technology, amplifier integration in SIW requires interconnects to a coaxial-like or quasi-TEM transmission-line medium to connect to the amplifier's input/output pins. If such integration is to be established within an SIW receiver system close to or at millimetre-wave frequencies, where low-permittivity substrates are preferred, then the type of transmission-line environment is important for a possible future addition of circuit elements. In this respect, CPW technology has several advantages over its MS line counterpart in the design of millimetre-wave integrated circuits. They include surface-mount integration, lower phase velocity variation, lower crosstalk and lower radiation loss [14, 15]. Within SIW technology, however, SIW-to-MS transitions are straightforwardly designed [16] and are commonly used for the measurement purpose of SIW components.

Therefore this paper presents two K-band low-noise amplifier (LNA) chip integrations: first, and for the first time, an LNA integration is achieved that uses broadband interconnects from SIW to CPW [17]. Second, and for comparison, the same LNA chip is integrated with SIW-to-MS transitions. Compared with the designs presented in [11–13], these circuits operate at higher frequencies (18–26.5 GHz), have a potentially larger bandwidth through avoiding the DC-decoupling in the MS integration of [11] and the use of wideband SIW-to-CPW or SIW-to-MS transitions that do not have to be redesigned if a different amplifier chip is used.

2 Circuit layout and design

The low-permittivity substrate for integrating the LNA is selected as RT/Duroid 6002 with $\varepsilon_r = 2.94$, $\tan\delta = 0.0012$, substrate thickness $h = 0.508$ mm, metallisation thickness $t = 17.5$ µm, and conductivity $\sigma = 5.8 \times 10^7$ S/m. The active device used for this application is a Hittite HMC751LC4 SMT GaAs pHEMT MMIC LNA for 17 GHz to 27 GHz operation [18]. It is 50 Ω input/output matched and is manufactured in a RoHS compliant 4 mm × 4 mm packaged housing. The chip is amenable for surface mount manufacturing applications.

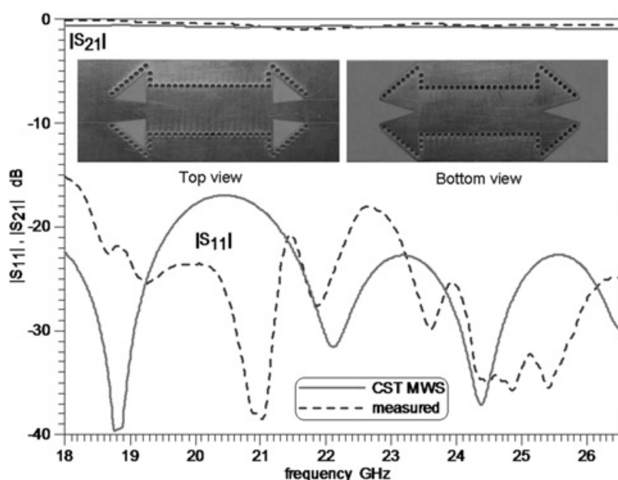

Fig. 1 *Photographs and performance of the back-to-back CPW-to-SIW transition used for amplifier integration*

2.1 Integration with SIW-to-CPW interconnects

Since the LNA is to be integrated in CPW involving SIW-to-CPW interconnects, the transition in [17] is redesigned for the current substrate. Its photograph is shown in the inset of Fig. 1 and its dimensional parameters are listed as follows. The CPW line is designed for a characteristic impedance of 50 Ω; thus its centre conductor is 3.1 mm wide and its slot widths are 0.15 mm. The bandwidth for the LNA integration is chosen as 18 to 26.5 GHz. Therefore the cut-off frequency of the SIW is selected as 14.1 GHz with lateral centre-to-centre via spacing of 6.7 mm. The via diameters and centre-to-centre spacing in longitudinal direction are determined as 0.62 and 0.866 mm, respectively, according to [19].

It is well known that closed-form expressions for the characterisation of CPW circuits are valid only for high-permittivity substrates. Therefore the design of this interconnect on low-permittivity substrate is based on a parametric study involving commercially available field solvers such as CST Microwave Studio. The SIW is first connected to a quasi-MS line whose initial width is selected according to an SIW-to-MS transition [16] while its bottom metallisation is gradually removed (cf. inset of Fig. 1). A gradual transition on the top metallisation involving via holes brings the top ground planes closer to the MS line to form a regular CPW with the bottom ground plane removed. The parametric study involves the transition length and width as well as the line width at the SIW-to-quasi- MS interface. After fine optimisation, the overall transition length from the SIW to the CPW is 4.56 mm. At the SIW interface, the MS line width is 2.2 mm, and the overall width of the removed metallisation is 10.32 mm.

A back-to-back configuration of the SIW-to-CPW interconnect is prototyped and measured. Fig. 1 shows the top and bottom views of the circuit and compares the numerical data, which are obtained with the time-domain solver of CST, with experimental results. The measurements are performed using a universal test fixture and standard TRL calibration circuits. The agreement between simulations and experiments is generally good. The measured return loss is better than 15 dB between 18 and 26.5 GHz. Measured insertion loss values are better than 1.2 dB with the worst case at the upper band end.

An important aspect to be considered in the LNA integration with CPW is the fact that the top ground planes do not provide enough heat dissipation for the LNA to operate properly. This was tested and confirmed with a separate layout which is not shown here. Therefore, a backside heat sink, including via-hole connections to the top metallisation directly under the LNA, was designed, and the grounding scheme of the LNA is devised such that all NC (not connected) lead paddles are unified with the ground labelled paddle. This provides a wider opening at the lower side of the LNA where the generated heat can spread out. Note that the additional via holes for connection to the heat sink do not complicate the fabrication process as via holes are required for the SIW circuitry surrounding the amplifier. Figs. 2*a* and *b* depict the top and bottom metallisation of the layout for LNA integration with SIW-to-CPW transitions.

The geometry of the heat sink must be carefully devised. If it is extended below the slots of the CPW, then it could potentially deteriorate the field pattern of the CPW by creating an abrupt transition from CPW to GCPW. Having

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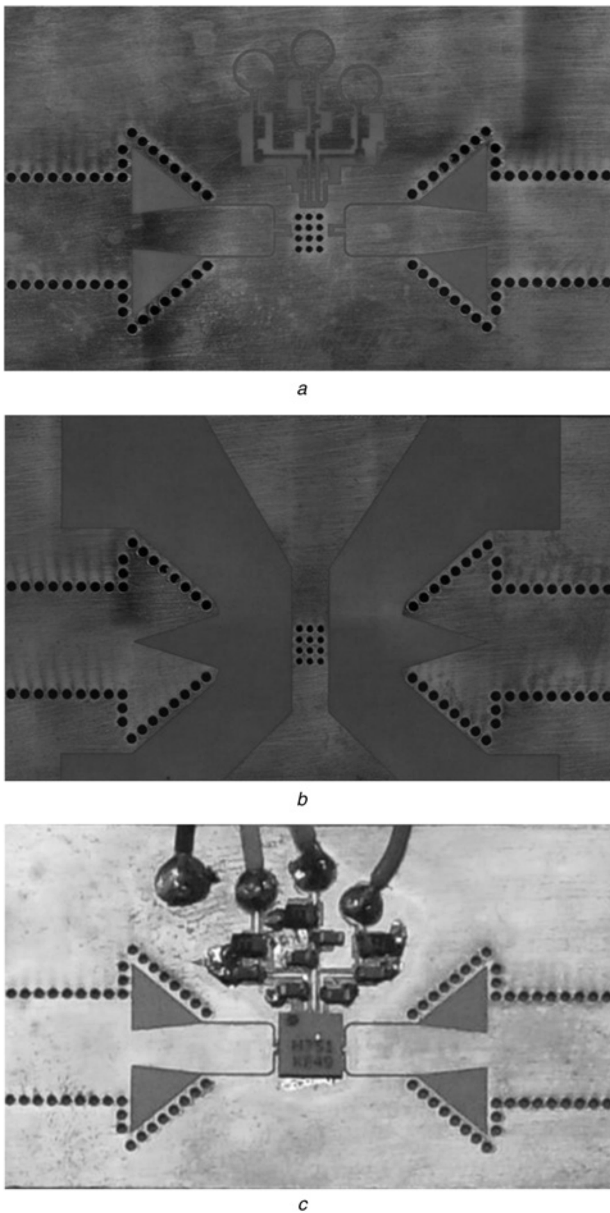

Fig. 2 *Photographs showing LNA integration with SIW-to-CPW transitions*

(a) Top view and (b) bottom view, (c) complete circuit including biasing

this in mind, the heat sink is extended vertically (in Fig. 2*b*) below the LNA and is horizontally limited to the LNA's backside ground width. Once it is stretched far away from the CPW slots, where GCPW mode propagation is no longer an option, the heat sink widens in both directions and allows for proper heat dissipation.

Fig. 2*c* shows the top view of the circuit with the integrated LNA and a biasing circuit that is adapted from the Hittite data sheet [18]. During measurements, as presented in the next section, no overheating of the LNA chip or the surrounding circuitry was observed which confirms proper operation of the heat sink.

2.2 Integration with SIW-to-MS interconnects

Integrating an LNA in SIW within SIW-to-MS interconnects is the most straightforward approach in terms of ease of connection, fabrication and adaptation between the two transmission lines. Two main advantages over the

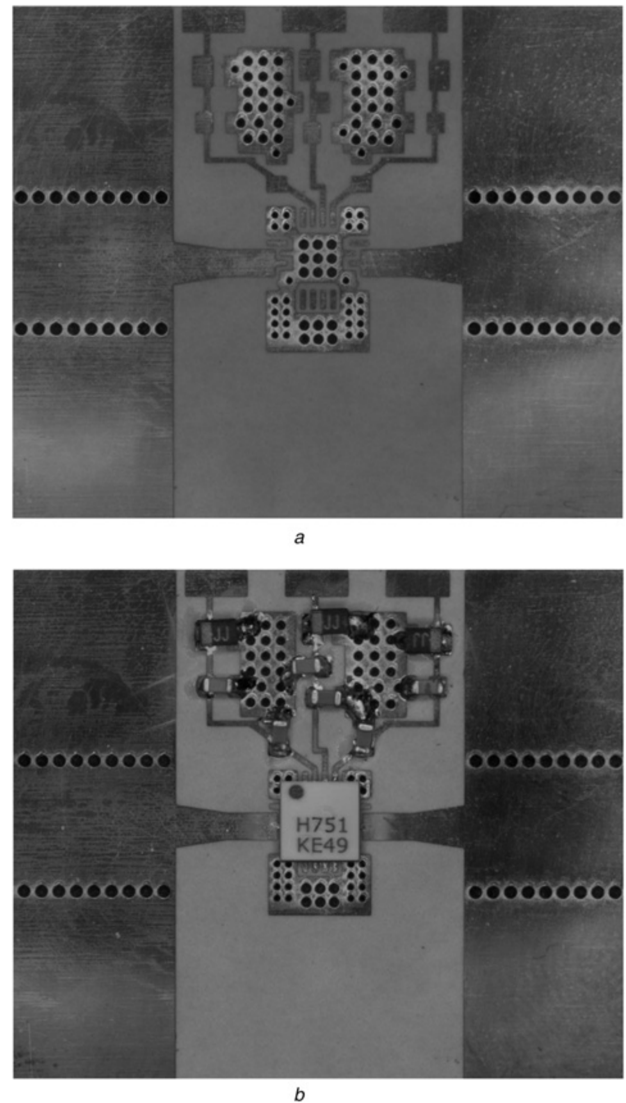

Fig. 3 *Photographs showing LNA integration with SIW-to-CPW transitions*

(a) Layout, (b) complete circuit including biasing

SIW–CPW integration in Section 2.1 facilitate the design and circuit layout. First, SIW-to-MS transitions are well known and can be designed according to Deslandes [16]. This transition (shown in Fig. 2) is 2.28 mm long, and the MS line width extends from 1.31 mm (50 Ω at the LNA port) to 2.06 mm at the SIW interface. Second, the bottom ground of the MS circuit can be accessed through via-hole perforation to provide an adequate heat dissipation medium for the LNA, which otherwise fails to operate efficiently and correctly.

This is demonstrated in Fig. 3*a* where the layout of the integrated LNA circuit within SIW-to-MS transitions is shown. Fig. 3*b* shows the same layout with the LNA chip and biasing circuit integrated.

3 Results

Gain and reflection measurements of the two LNA circuits introduced in the previous section are performed over the K-band frequency range of 18–26.5 GHz using an Anritsu SC5226 Universal Test Fixture (3680 K with 3680-20 base) and an Anritsu 37397 series Vector Network Analyser

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(VNA). An Agilent N8975A Noise Figure Analyser (NFA) and an Agilent N4002A series Noise Source (NS) are used to measure the noise figure.

Fig. 4 shows the experimental results for the LNA with SIW-to-CPW interconnects according to Fig. 2*c*. The measured input and output reflection coefficients remain below −10 dB over a frequency range between 21.5 and 26.5 GHz. However, $|S_{11}|$ reaches maxima of −7 dB at 18 GHz and −9 dB at 19.8 GHz in the lower regions of the band. The corresponding values for $|S_{22}|$ are −7.5 dB at 18 GHz and −7.3 dB at 20.9 GHz. Note that the measured reflection coefficients of the back-to-back SIW-to-CPW interconnects are better than −15 dB over the entire frequency range (cf. Fig. 1). Therefore the increase in measured reflection of the integrated chip is mainly attributed to the discontinuity between the CPW lines and the LNA chip. As a result of the low-permittivity substrate used, the centre conductors of the CPW on either side of the LNA have to be significantly narrowed to be able to connect to the LNA chip's lead paddles. This is seen in Figs. 2*a* and *c*. Thus, an abrupt discontinuity is created which contributes to an increased reflection coefficient. A possible remedy, namely a longer taper section in these regions was not investigated since the entire circuit had to fit into the test fixture for measurements.

The measured gain is reasonably flat and better than 20 dB over the entire K-band. This is a major improvement compared with the SIW-MS single-transistor integration in X-band [11]. The gain variation in Fig. 4 spans from 20.6 dB at 18 GHz to 23 dB at 21 GHz.

Noise figure measurements were performed in order to assess the additive noise of the DC biasing circuit, consisting of three voltage sources and noise blocking capacitive elements. The configuration of the bias circuit, the positioning of the lumped elements and the quality of the soldering to minimise parasitic effects, have significant impact on the additive noise. The measured noise figure is 4.35 dB on average with a minimum of 4 dB at 18 GHz and the maximum of 4.7 dB at 26.5 GHz.

Fig. 5 shows the measured results for the LNA with SIW-to-MS interconnects according to Fig. 3*b*. Both input and output reflection coefficients remain below −12 dB over the entire K-band.

The measured gain is greater than 21 dB with a maximum of 22.4 dB at 22.7 GHz and a minimum of 21.3 dB at 25.2 GHz. The average noise figure is measured as 3.95 dB with a minimum of 3.7 dB at 18 GHz and a maximum of 4.2 dB at 26.5 GHz.

In comparing the measured performances in Fig. 4 with those in Fig. 5, it is observed that the LNA integration within SIW-to-MS interconnects (Fig. 5) performs slightly better than the one with SIW-to-CPW transitions. This performance advantage is mainly seen in gain linearity (21.85 ± 0.55 dB against 21.8 ± 1.2 dB) and noise figure (3.95 ± 0.25 dB against 4.35 ± 0.35 dB). (Fig. 6 shows a direct comparison for gain and noise figure). Moreover, the input/output return loss values are slightly better than in Fig. 4. This is attributed to the fact that the discontinuity between the MS lines and the LNA lead paddles (Fig. 3*a*) is less severe than that between the CPW and the LNA lead paddles.

Note that the measured noise figures of both circuits presented here are higher than the nominal noise figure of 2.2 dB of the LNA chip as reported in [18]. Therefore experiments with an evaluation board supplied by Hittite, where the chip is integrated on substrate with $\varepsilon_r = 3.58$ in GCPW technology without any transitions to SIW, were performed for comparison, using the same noise source and noise figure meter as for the previous measurements. The measured results are compared in Fig. 6 with respect to gain and noise figure. Under the same conditions, the evaluation board's gain was measured as 20.7–22.4 dB (Fig. 6*a*) and its noise figure as 3.8–4.2 dB (Fig. 6*b*).

It is noted that beyond 20 GHz, the average gain (Fig. 6*a*) of the evaluation board is higher than that of the SIW–MS integration. However, the SIW–MS integration shows less variation over the entire K-band. The SIW–CPW integration has the highest peak gain but also the most variation. The noise figures in Fig. 6*b* are comparable between the evaluation board and the SIW–MS integration; those of the SIW–CPW integration are about 0.5 dB higher.

Since the measured data between the new circuits in Figs. 2*c* and 3*b* and the evaluation board are roughly comparable in value and variation, it is concluded that the LNA chip is successfully integrated in CPW and MS and

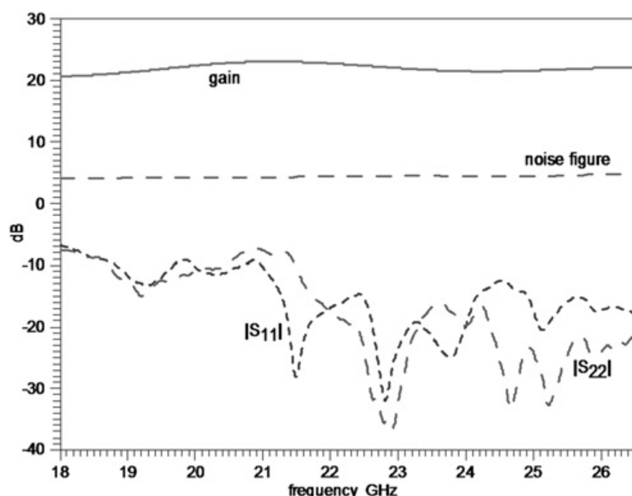

Fig. 4 *Measured gain, input/output reflection coefficients and noise figure of the LNA with SIW–CPW interconnects in Fig. 2c*
(For gain and noise figure variation, see Fig. 6.)

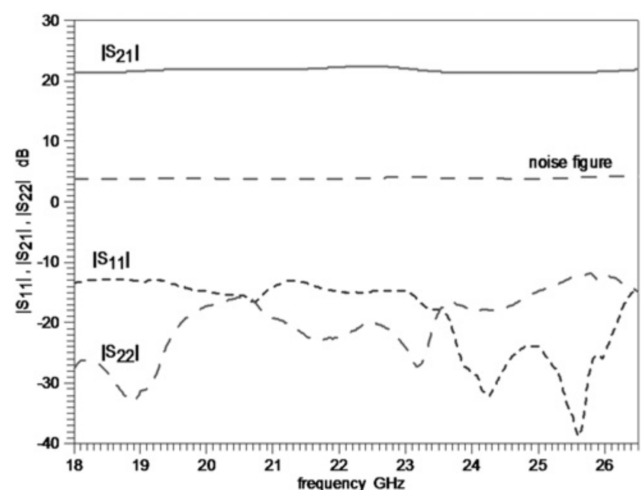

Fig. 5 *Measured gain, input/output reflection coefficients and noise figure of the LNA with SIW–MS interconnects in Fig. 3b*
(For gain and noise figure variation, see Fig. 6.)

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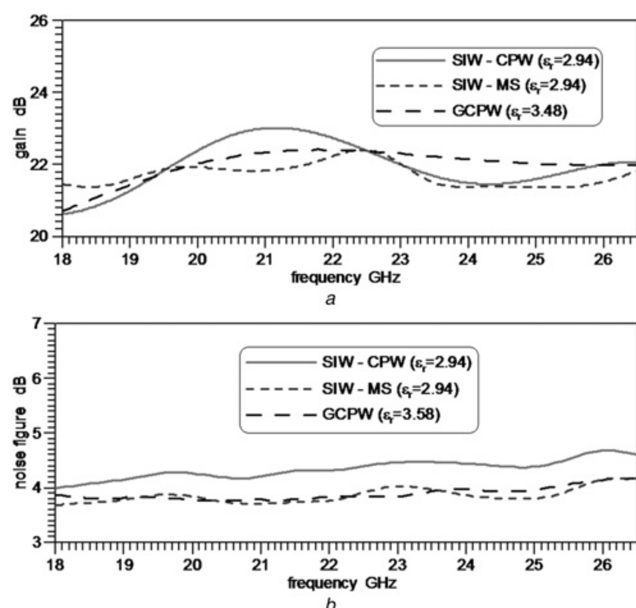

Fig. 6 *Measurements for LNA integrations within SIW-to-CPW-interconnects (solid line), SIW-to-MS interconnects (dotted line) and GCPW technology (evaluation board – dashed line)*

(a) Gain (b) noise figure

that the CPW-to-SIW and MS-to-SIW interconnects can provide for wideband integration within SIW ports.

4 Conclusions

For the first time and for the purpose of integrating an LNA chip within an SIW environment, CPW technology is used to provide an adequate interconnect between CPW and SIW. The chip integration in CPW requires a heat sink that needs to be carefully designed to eliminate interference with the interconnects. The LNA chip integration in CPW – including biasing circuits and CPW-to-SIW transitions – results in minimum gain and maximum noise figure of 20 and 4.6 dB, respectively. For comparison, the integration of the same LNA within SIW-to-MS interconnects provides slightly better results which are mainly attributed to the discontinuities between CPW or MS and the lead paddles of the LNA chip.

Nevertheless, the measured values are very comparable with those of a manufacturer-supplied evaluation board that does not involve transitions to SIW. The measured input and output return loss values are better than 10 dB over almost the entire K-band. Thus, the proposed circuits present viable options for successful integrations of amplifier technology within SIW systems and present major improvements over a similar SIW-to-MS X-band amplifier.

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