

K-band backward diplexer in substrate integrated waveguide technology

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The first backward diplexer for K-band substrate integrated waveguide (SIW) operation is presented. The advantage of this compact diplexer is having input and two output port interfaces at the same side of the substrate, which advances the applications of SIWs to more complex feed system assemblies. The diplexer has two bands at 20 and 21 GHz. The bandwidth of each band is 0.4 GHz, which gives 2 and 1.9% bandwidth at lower and higher bands, respectively. The diplexer is designed and analysed with the mode-matching technique, and its performance is verified by comparison with simulated and measured data. The in-band measured return and insertion losses are 14.65 dB/2.75 dB in the lower band and 13 dB/3.05 dB in the upper band.

Introduction: The introduction of substrate integrated waveguide (SIW) technology in the early 2000s has created new perspectives for microwave engineers to design integrable, compact, low-loss and high Q -factor circuits at low cost. Among various types of passive components designed based on this technology are SIW diplexers for different microwave frequency bands from the C-band up to 60 GHz as reported in the literature [1–8].

Available diplexers have different structural topologies. In [1, 2], SIW diplexers with branching port configurations are presented where the angle between the two output ports is 90° . T-junction diplexers are presented in [3–5] with output port angles of 180° . Instead of using a T-junction to separate the three ports of the diplexer, a circulator is utilised in [6] and results in an output ports angle of about 120° . However, using curved microstrip ports results in a Y-type diplexer. A dual-mode square cavity is employed in [7] as the common resonator to replace the T-junction. However, the positioning of the ports in this configuration is the same as that in T-junction diplexers. A Y-type diplexer is also presented in [8].

In this Letter, we present a new design for SIW diplexers in which all three ports are located at the same edge of the substrate. Owing to the orientation of the ports, this component is named the backward diplexer. This new design, besides being compact compared with other diplexer topologies, as it fits all port interfaces on the same dielectric area, has two main engineering applications. Owing to the common-port interface, first, this diplexer can be placed almost anywhere within a box of a feed network, and especially, close to heat-absorbing features if required. Hence, the new topology enhances the final integration of the diplexer in a feed system [9]. Secondly, the diplexer can be easily replaced/redesigned or just plugged in, if more stringent specifications or a different frequency range is required. The backward diplexer is geared for operation at the K-band with 15 dB return-loss (RL) bandwidths of 0.4 GHz located at 20 and 21 GHz, and is initially designed in dielectric-filled waveguide technology based on principles presented in [8]. Since a conversion from square to circular via holes is envisaged, the dimensions of the square via holes, as derived for a given via diameter [10], can be incorporated from the onset in the all-dielectric waveguide design, for example, as aperture thickness or separation wall thickness. The diplexer is then translated to SIW technology using the relation between the SIW width and its effective waveguide width [11]. Optimisation using a mode-matching technique (MMT) [12] and verification by CST Microwave Studio complete the design. Comparisons with measurements validate the design procedure.

Diplexer design: The design of the diplexer begins with synthesising the two channel filters in waveguide technology. The substrate is chosen as RT/Duroid 6002 with $\epsilon_r = 2.94$ and height $h = 0.254$ mm with loss factors $\tan\delta = 0.0012$ for the dielectric and $\sigma = 5.8 \times 10^7$ S/m for the copper layers and vias. The equivalent waveguide width is set to be $W_{\text{equi}} = 5$ mm. Two five-pole Chebyshev iris filters with bandwidths of 0.4 GHz at 20 and 21 GHz are designed with the MMT approach. The thicknesses of the apertures are chosen as $l_{\text{iris}} = 0.55$ mm, which is the same as the side length of the square via in the SIW structure. This results in via diameters of $d = 0.6444$ mm in the SIW diplexer [10]. Fig. 1 shows the performance of the two channel filters with MMT data verified by simulations in CST.

The backward waveguide diplexer is then constructed from the channel filters. Optimisation using the MMT results in an in-band return loss better than 25 dB and channel isolation better than 50 dB.

The layout and performance of the waveguide diplexer are presented in Fig. 2. All the structural parameters of the all-dielectric waveguide diplexer are shown. The MMT data is verified by simulations with CST. Note that a via is added at the centre of the structure, close to the short circuit at the far end (layout in Fig. 2), to provide a better return loss.

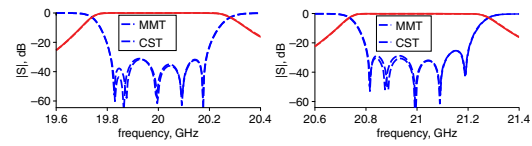


Fig. 1 Lower (left) and higher (right) channel filters of backward waveguide diplexer. Filters are designed with MMT (solid line) and verified in CST (dashed line)

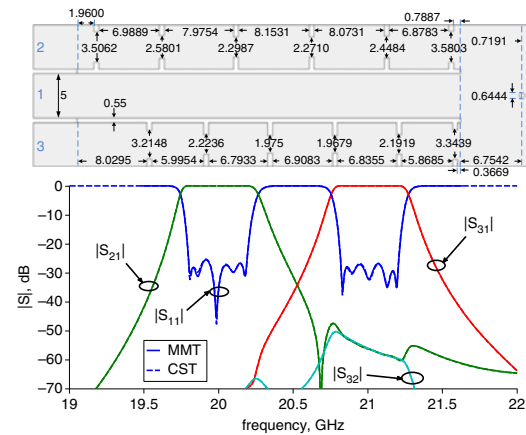


Fig. 2 Layout (dimensions in mm) and performance of backward all-dielectric waveguide diplexer. MMT data (solid line) is identical with CST data (dashed line) to within plotting accuracy

The diplexer is then translated to SIW technology using the relation presented in [11]. The side length of the square vias and via pitch are $l_{\text{square}} = 0.55$ mm and $p = 1$ mm, respectively. Deploying the MMT approach [12], the SIW diplexer with square vias is optimised for best performance in each band. The square-to-circular conversion relation adopted in [10] is deployed to replace square with circular vias with a diameter of $d = 0.6444$ mm. 15 dB return loss in each band and isolation better than 53 dB between the two channels are achieved. The layout and performance of the optimised SIW backward diplexer with circular vias and with waveguide ports are presented in Fig. 3, where the MMT data for square vias is also verified by CST data for circular vias.

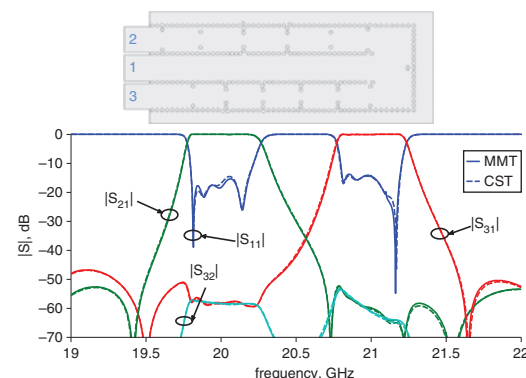


Fig. 3 Backward SIW diplexer (top) and its performance (bottom). MMT data for square vias (solid line) is compared with CST data for circular vias (dashed line)

It should be noted that for the SIW diplexer, the return loss at each band is better than 15 dB (for the same bandwidths as those in the waveguide design), which is inferior to the 25 dB return loss achieved in the all-dielectric waveguide component of Fig. 2. One of the main reasons is that in SIW technology the spacing between vias is restricted by

manufacturing limitations. In this case, according to our manufacturer, the separation between vias should be at least 0.2 mm for a via diameter of $d=0.65$ mm, to properly drill the vias. This restriction prevents us from realising some of the iris widths obtained in the waveguide design, and thus the vias around those irises should be displaced as well (c.f. the adjusted vias around irises in Fig. 3). This backward diplexer, because of the presence of a short at the far end, is very susceptible to these structural changes compared with regular types of diplexers, for example [4, 5, 8]. As a result, optimising such a structure is a more cumbersome task. Nevertheless, the designed SIW backward diplexer still outperforms most of the previously designed diplexers in terms of RL, for example 12 dB RL in [1], 11 dB RL in [2].

Measurement: The fabricated prototype of the SIW backward diplexer, along with its simulated and measured performances, is presented in Fig. 4. Note that the structure with microstrip ports has a slightly better in-band RL (RL better than 16.5 dB) in a slightly narrower bandwidth (395 MHz) of the first band. The width of the 50 Ω microstrip port is $w_m = 0.6442$ mm, and the widths and lengths of the tapers after optimisation are 1.0019 mm and 2.3058 mm, respectively.

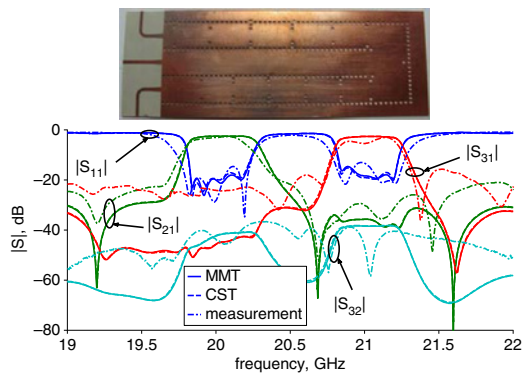


Fig. 4 Photograph (top) and performance (bottom) of fabricated prototype. MMT data for square vias (solid line) is compared with CST data for circular vias (dashed line) and measurements (dash-dotted line)

To be able to use a test fixture in our measurement for at least one of the ports, the two output ports are curved. The parameters of the bent microstrip ports, $R_c = 2w_m$, $\alpha = \pi/2$, are based on the data presented in [13], where R_c is the radius of the bend and α is the curve angle. The via diameter has changed to $d = 0.65$ mm because of fabrication restrictions. The overall agreement between measured data and MMT and CST data is good. The in-band measured RLs are 14.65 and 13 dB, compared with the simulated RLs of 16.5 dB and 15 dB. The in-band measured insertion losses are 2.75 and 3.05 dB compared with the simulated 2.53 and 2.76 dB. The measured isolation between the two channels is better than 36.7 dB, compared with 38.4 dB in the CST simulation.

Conclusion: A K-band backward SIW diplexer of more compact design compared with other common diplexer designs and high isolation between channels is presented. The common-port interface in this topology is advantageous in enhancing the integration of the diplexer in more complex feed systems. Approximately 0.4 GHz bandwidth as well as 14 and 15 dB return loss are achieved at lower (20 GHz) and higher (21 GHz) bands of the diplexer, respectively. The diplexer is

designed and analysed with an MMT approach, and comparison with the simulations in CST and measurements validates the design.

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One or more of the Figures in this Letter are available in colour online.

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