Accurate Simulation of High-Gain MMIC Amplifiers With Microstrip-Type Transistors

Mingye Fu, Nianhua Jiang, *Member, IEEE*, Jens Bornemann, *Life Fellow, IEEE*, and Quanyuan Feng, *Senior Member, IEEE*

***Abstract*—A discrepancy of monolithic microwave-integrated circuit (MMIC) amplifier simulations is discussed for conventional electromagnetic (EM) circuit co-simulation in advanced design system (ADS). An obvious discrepancy occurs when microstrip (MS) type transistor schematic models are used in a high gain MMIC amplifier. The coupling effect of a backside via hole in the MS-type model, which is excluded from EM layout simulation, is demonstrated to be the root of this error that will become significant in high-gain MMIC amplifier design. A new method is proposed to include a source via hole of the MS-type transistor in MMIC layout EM simulations. Simulation experiments confirm that this new method can significantly improve the EM simulation accuracy when including a transistor source via hole in the circuit layout EM simulation. The intercoupling effect of the transistor source via is investigated on the correlation with frequency, current gain, via separation distance, and substrate thickness.**

***Index Terms*—Amplifier design, backside via hole, electromagnetic (EM)-circuit co-simulation, monolithic microwave-integrated circuit (MMIC), transistor.**

I. Introduction

MONOLITHIC microwave-integrated circuits (MMICs) have seen increased development in the past several decades. Besides the continuously improving process of fabrication, which is the basis of high performance circuits, advanced computer-aided design (CAD) techniques also play an important role. The CAD tools for MMICs highly improve the efficiency of a design flow and thus, become indispensable. For a passive MMIC, which may be fabricated based on the integrated passive device process (IPD) [1], the entire structure is electromagnetic (EM) simulated with CAD tools. The EM simulation algorithm can be the finite element method (FEM), finite difference time domain (FDTD), method of moments (MoM), etc. A more common case is an MMIC that contains some active devices, such as an HBT [2], pHEMT [3], or mHEMT [4]. Then, the EM simulation should be combined with a circuit simulation to obtain the circuit's performance, which leads to the widely used EM-circuit co-simulation method that includes two parts: 1) layout EM simulation and 2) circuit simulation.

In the EM simulation, the active devices should first be removed from the layout. Each deleted active device layout is the layout view of the schematic model of the active device. Then, in the remaining layout, some ports are added where the active device terminals are originally located. These ports are required in the circuit simulation. They are connected to the terminals of the schematic models of the active devices, as observed in the second figure in [5]. In this way, the performance of the MMIC can be obtained in a circuit simulation. This EM-circuit co-simulation method is widely used. Detailed descriptions can be found in [6]–[8] and examples provided by the advanced design system (ADS). With some recent tools, such as automated EM-circuit partitioning used in [7] and RFpro in ADS, users do not need to manually remove the active devices in the layout and connect the models in the schematic. Yet the essential procedure is the same.

As mentioned, there are two parts of EM-circuit co-simulation: 1) EM simulation and 2) circuit simulation. Both are important to the simulation accuracy. In the circuit simulation, the models of active devices should be accurate. Thus, many researchers are working on transistor models and modeling methods [9]–[13]. For the EM simulation, although modern software tools are very powerful, the accuracy highly depends on the simulation settings (mesh, port, boundary, layout, etc.). Since an accurate EM-circuit co-simulation is desired, improvements of the EM simulation and circuit simulation (model accuracy) are required. But they are usually discussed separately. In some cases, the EM-circuit co-simulation is inaccurate because the combination of the circuit layout ("circuit layout" is the layout simulated in EM simulation, which removes the transistors) and the schematic model fails to capture the reality. For instance, the pad capacitance may be lost or duplicated in the EM-circuit co-simulation. Reference [14] presents the port layout and port settings for different types of device models. Another category is related to transistor model types and will be demonstrated in this article.

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In the MMIC amplifier design, foundries usually provide two types of transistor models: 1) the coplanar waveguide (CPW) type and 2) the microstrip (MS) type. MMIC design engineers usually use these models as a black box in schematic design. The MS-type transistor model itself includes the backside via in the model while the CPW-type transistor model has no via. In the current CAD tools of MMICs, the transistor layouts cannot be included in the circuit layout for EM-simulation. Therefore, the backside via effect of the MS-type transistor model is missed in the MMIC layout EM-simulation in the conventional EM simulation setup. However, all of the backside vias on the MMIC chip would have EM interference with each other. So the backside via missing of an MS-type transistor on the circuit layout would result in the mutual inductance or coupling effect lost in the EM simulation. This omission will cause the design error in the final circuit layout EM simulation. To the best of our knowledge, there are no published papers in the literature that reported this issue. References [5]–[8] and examples/tutorials of ADS explicitly show their simulation methods but none of them mention this problem. Some LNAs used MS type transistors such as the ones in [15] and [16], etc., but these papers did not discuss the backside via in the circuit layout and simulation setup. Even the MMIC foundries do not provide any suggestion about this issue in their documents.

In this article, a new approach is proposed as an engineering solution to solve the problem. For the MMIC amplifier design, this proposed method can help MMIC design engineers to avoid the flaw in design and simulation. The GaAs pHEMT MMIC process is used as a demonstrator. The layout and port settings for different types of transistor models are investigated with ADS. Two special cases of EM-circuit co-simulation, whose EM simulation is based on the FEM, are presented. The intercoupling effect of the transistor source via is investigated on the correlation with frequency, current gain, via separation distance, and substrate thickness.

II. Accuracy Issue in High-Gain Amplifier Simulation

A. CPW-Type and MS-Type Transistors

There are two types of transistor models in the GaAs pHEMT process: 1) CPW type and 2) MS type. A CPW-type transistor model has three ports for users: 1) gate; 2) drain; and 3) source. For MS-type transistors, only two ports are available: 1) gate and 2) drain. The source of an MS-type transistor is connected to the backside via, which is not accessible for the circuit layout design. In other words, the source via is a part of the MS-type model but it is not included in the CPW-type model. A comparison between CPW-type and MS-type transistors is shown in Fig. 1.

The CPW-type transistor provides the source port for the designer to add in source inductance. However, the source inductance can cause the gain to decrease with increasing frequency. The MS-type transistor layout is designed to minimize the source inductance at the source port by including the via hole in the model. These two types of transistors have different usage in MMIC design. The CPW-type transistor is mostly used in the first stage to optimize noise and S_{11}. The MS-type transistor is often used in the last stage and mid stages to improve the gain, gain flatness, power capability, and extend the frequency band. Both CPW-type and MS-type transistors are needed in multistage MMIC amplifier design.

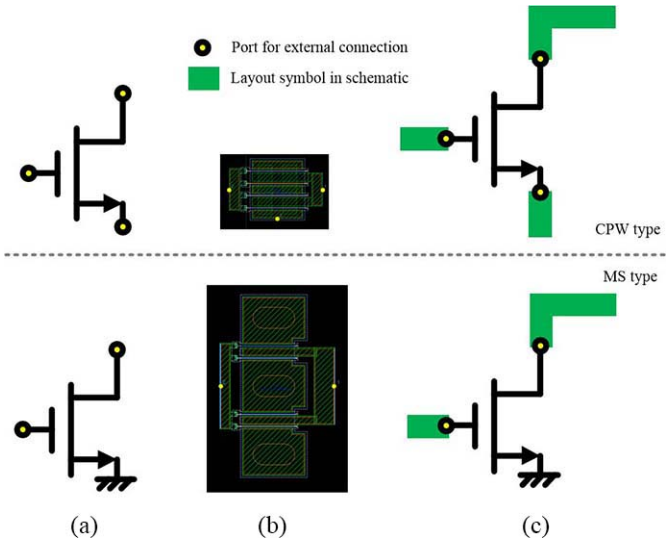

Fig. 1. CPW-type and MS-type transistors. (a) Schematic view. (b) Layout view. (c) In EM-circuit co-simulation. The top ones show a CPW-type transistor while the bottom ones show an MS-type transistor.

The two models are treated differently in EM-circuit co-simulation where the transistor model should be removed from the layout for the layout EM simulation. The ports that are added to the layout correspondingly are direct-feed ports in ADS. Their self-inductances and mutual inductances are removed from the result by default. When a CPW-type transistor is removed, the source network, whether it is only a backside via or a complex network, remains in the layout. So the effect of the source and ground via network is accounted for in the EM simulation. On the contrary, since the MS-type transistor model includes the active part and source ground via, both active structure and ground via are removed in the circuit layout EM simulation, as shown in Fig. 1(c). The EM coupling effect of the source ground via is ignored in the layout EM simulation. This omission will degrade the simulation accuracy significantly when an amplifier has high gain, involving large currents in transistors.

B. Backside Via in GaAs pHEMT MMIC Process

A backside via in the GaAs process crosses through the GaAs substrate. It connects the bottom ground metal and the top circuit metal layers. Fig. 2 illustrates a simplified cross-section view of the substrate with a backside via. In practice, both DC and RF currents flow through this backside via (current I in Fig. 2). Correspondingly, a magnetic field is generated, which couples it with other components within the MMIC layout. This intercoupling effect affects the circuit performance.

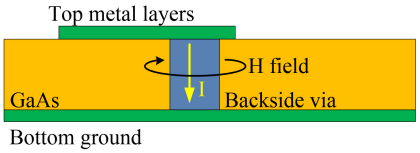

Fig. 2. Simplified cross-section view of the substrate with a backside via.

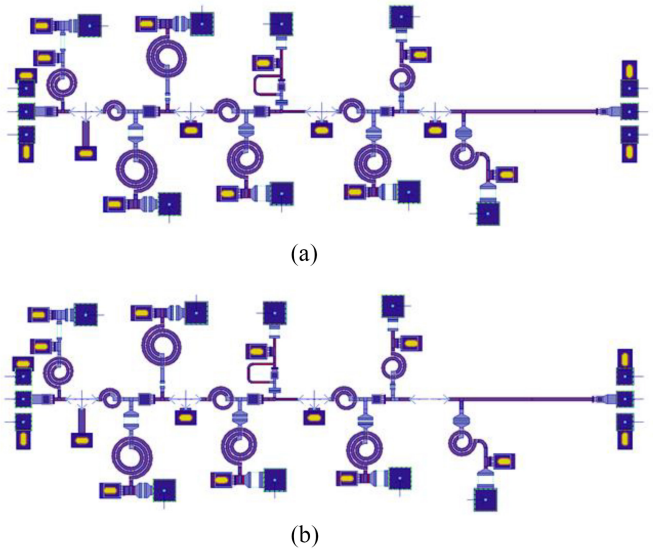

Fig. 3. Layout of an amplifier (a) with four CPW-type transistors that are removed for EM-circuit co-simulation and (b) with MS-type transistor in the last stage and the ground via is removed.

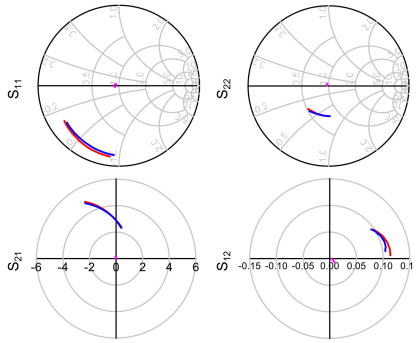

Fig. 4. S-parameter comparison of CPW-type model and MS model of GaAs pHEMT, from 8 to 20 GHz. Blue line: CPW-type transistor; red line: MS-type transistor; and pink line: the difference between blue line and red line.

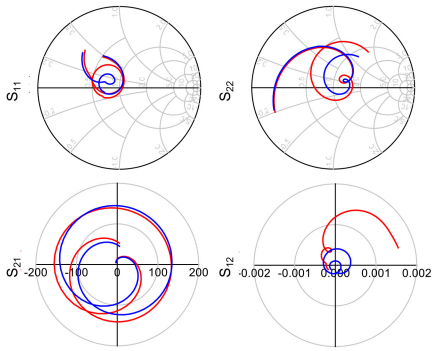

Fig. 5. Simulated results of the amplifiers in Fig. 3(a) and (b). Blue line: all transistors are CPW type; and red line: the last stage uses MS type.

C. Issues in High-Gain Amplifiers

The first layout is a Ku-band high-gain MMIC amplifier. As shown in Fig. 3(a), four CPW-type transistors are utilized in this design and are already removed from the circuit layout for EM-circuit co-simulation. All of the four transistors have the same size: 4 fingers and 75 μm gate width per finger. In this simulation experiment, the transistor in the last stage will be changed to an MS type for comparison. As shown in Fig. 3(b), the ground via is removed for the MS-type transistor in the last stage. The layout views of transistors that are removed from the layout in Fig. 3 are shown in Fig. 1(b).

The *S*-parameters of the CPW-type transistor (plus an EM simulated backside via) and MS-type transistor (both have a size of 4 $\times$ 75 μm), from 8 to 20 GHz, are shown in Fig. 4. In this frequency band, the performances of these two types of transistors have small differences. Therefore, it is assumed that the EM-circuit co-simulated performance of the layout in Fig. 3(a) will hardly change if the CPW transistor in stage 4 is replaced by an MS-type transistor.

Fig. 5 shows the EM-circuit co-simulated results of the layout with CPW-type and MS-type transistors. It can be observed that the *S*-parameters deviate significantly when the type of transistor is changed. The only difference between these two layouts is the transistor type of the last stage. These significant discrepancies between EM-circuit co-simulation results cannot be explained by the little difference of two transistor models' performances, which is shown in Fig. 4. By further simulation experiments, the cause is attributed to the intercoupling effects of the source ground via of transistors. In the following sections, we will explain this in detail and propose a method to deal with the intercoupling effect.

In order to verify the problem that the backside via is excluded in the MMIC layout EM simulation with the MS-type transistor model, a new MS-type transistor, which is based on the original CPW-type model, is created as depicted in Fig. 6. The original CPW-type transistor is connected to an EM simulated source inductor, which is mainly a backside via. The simulated results are exported to a 2-port data file as in Fig. 6(b), which can be used as an MS-type transistor in EM-circuit co-simulation. In this way, a single CPW-type transistor (plus a backside via) and a single MS-type transistor have the same performance. Thus, the unwanted small deviation of models observed in Fig. 4 can be eliminated. Either of these two transistors can be used in MMIC circuits, and the performances are supposed to be the same. It should be noted that only the self-inductance of the backside via layout is included in the new model while the mutual inductance with other components is not accounted for. The new model is just used in this experiment to verify the problem.

The second amplifier layout as shown in Fig. 7 is also simulated. The last stage originally utilizes the CPW-type transistor that can be replaced by the new MS-type transistor model in Fig. 6(b).

Fig. 8 shows the EM simulated layout of Fig. 7 in which the transistor in stage 4 is a CPW type. When the last stage

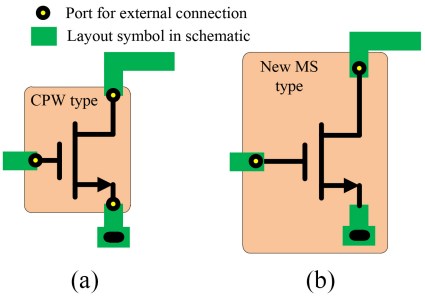

Fig. 6. New MS-type transistor based on original CPW-type transistor. (a) EM–circuit co-simulation with original 3-port CPW-type transistor. (b) Conventional EM-circuit co-simulation configuration of the new 2-port MS-type model. The two simulations have the same results.

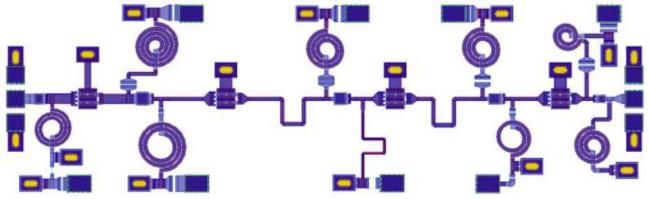

Fig. 7. New amplifier layout with four stage transistors. The last stage can be the new MS-type model or CPW-type model.

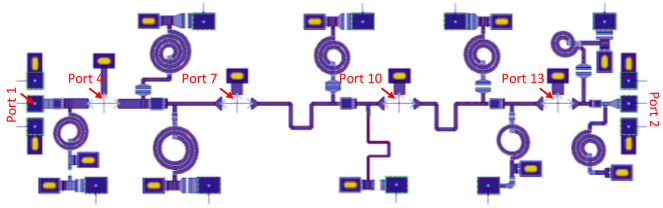

Fig. 8. EM simulation layout with all CPW-type transistors removed in Fig. 7.

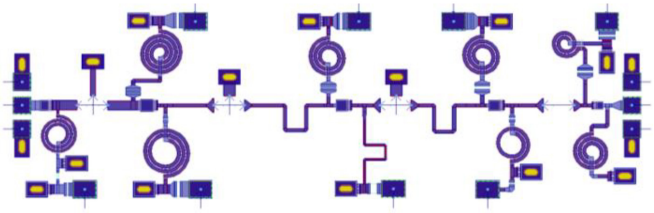

Fig. 9. EM simulation layout with the last stage transistor replaced by a new MS-type transistors in Fig. 7. The last stage source via included in the MS-type model is removed from layout.

is replaced by the new MS-type transistor, the EM simulated layout in the co-simulation is as in Fig. 9. The only difference is the source layout of stage 4.

The corresponding EM-circuit co-simulation results are shown in Fig. 10. The simulated performances have significant differences. Especially, changing the model type of the last stage significantly influences the reflection coefficient S_{11}. The single transistors' performances of the CPW type and MS type are identical, and all other parts in layout remain the same. The only difference between the simulated layouts (Figs. 8 and 9) is the backside via in the 4th stage.

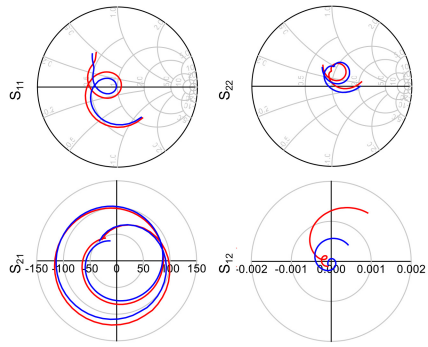

Fig. 10. EM-circuit co-simulation results of circuits in Figs. 8 and 9. Blue line: all transistors are CPW type; and red line: the last stage uses MS type.

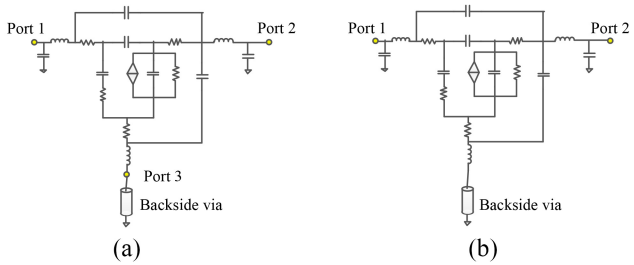

Fig. 11. Typical schematic model of (a) CPW-type transistor and (b) MS-type transistor.

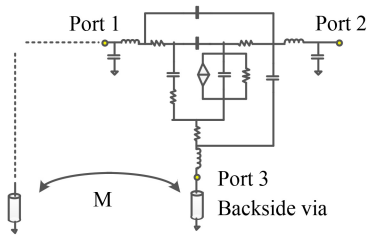

Fig. 12. Very common backside via coupling in MMIC layout design.

The backside via removed in the circuit layout of Fig. 9 can be seen as an inductor, which has self-inductance and mutual inductance (coupling). A typical schematic model of a transistor is shown as Fig. 11.

The self-inductance is included in the MS-type transistor schematic model. However, the mutual inductance is not included in either the schematic model or the circuit layout in the conventional EM simulation processing. A very common situation is shown in Fig. 12 where M is the mutual inductance.

This mutual inductance is never included in the model of a single transistor. Only when the two backside vias are both in the EM simulated layout, their mutual inductance M can be calculated, which is impossible for an MS-type transistor in a conventional simulation. In contrast, a CPW-type transistor has no backside via in its model so its layout provides the third port—a source port to add a backside via on the substrate chip, as in Fig. 11(a). The self- and mutual inductances of a CPW-type transistor will be both accounted for in the EM simulation. Hence, the only difference between the two transistor models in a conventional simulation method is the mutual

inductance—coupling, which is the root of the differences in Fig. 10.

III. Intercoupling Effect From Transistor Sources

A. Quantify the Intercoupling Effect

In principle, the intercoupling effect due to the backside via of any transistor is unavoidable because there are currents flowing through this backside via. Thus, some EM field is excited by this structure. This field will interact with other components in the layout and influence the performance.

To determine the strength of this coupling effect, the Z-parameters of the layout are calculated. The layout in Fig. 7 is simulated after the CPW-type transistors are removed and ports are assigned to the transistors' locations, as shown in Fig. 8. Including the ground-signal-ground (GSG) pads, dc feed pads and transistor terminals, there are 26 ports in the layout.

The voltage at port j, v_j, is written as

$$v_j = \sum_{k=1}^{26} Z_{j,k} i_k \tag{1}$$

where $Z_{j,k}$ is the element of the simulated Z-matrix at the jth row and kth column, and i_k is the current into port k. Not only can we calculate the total voltage at port j but we can also find the contribution of each port current. For the voltage at port j, the contribution of current in port k is defined as

$$C_{j,k} = \left| \frac{Z_{j,k} i_k}{v_j} \right| = \left| \frac{Z_{j,k} i_k}{\sum_{k=1}^{26} Z_{j,k} i_k} \right|. \tag{2}$$

It should be noted that $C_{j,k}$ is a unitless value. The source of the first stage (port 4) v_4 is taken as an example

$$v_4 = \sum_{k=1}^{26} Z_{4,k} i_k \tag{3}$$

$$C_{4,k} = \left| \frac{Z_{4,k} i_k}{v_4} \right| = \left| \frac{Z_{4,k} i_k}{\sum_{k=1}^{26} Z_{4,k} i_k} \right|. \tag{4}$$

For simplicity, only the contributions of port 4 (source port of stage 1), port 7 (source port of stage 2), port 10 (source port of stage 3), and port 13 (source port of stage 4) are discussed. First, the imaginary parts of $Z_{4,4}$, $Z_{4,7}$, $Z_{4,10}$, and $Z_{4,13}$ from 8 to 20 GHz are plotted in Fig. 13 (their real parts are relatively small). Imag($Z_{4,4}$) is related to the self-inductance looking into port 4 and has the largest value. Then, |imag($Z_{4,7}$)| > |imag($Z_{4,10}$)| > |imag($Z_{4,13}$)|, which is consistent with common sense because port 13 is the farthest away from port 4. But this does not mean that the last stage transistor has least influence on the first stage transistor because the last stage has the largest current in amplifier design.

As shown in (4), the numerator of $C_{j,k}$ is the Z parameter multiplying the current flowing into port k. The last stage transistor may have nearly hundred time larger current than the first stage transistor, which results in the largest $C_{4,k}$ even though the value of |imag($Z_{4,13}$)| is smallest. To prove this, the layout in Fig. 8 is used in the EM-circuit co-simulation

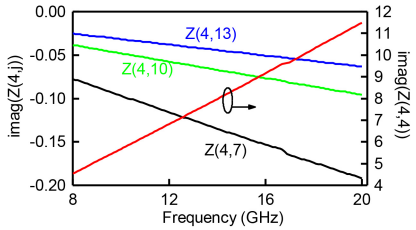

Fig. 13. Imaginary parts of $Z_{4,4}$, $Z_{4,7}$, $Z_{4,10}$, and $Z_{4,13}$ of Fig. 8.

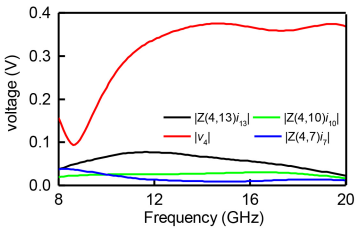

Fig. 14. Simulated voltage at source of stage 1: total voltage and its portions.

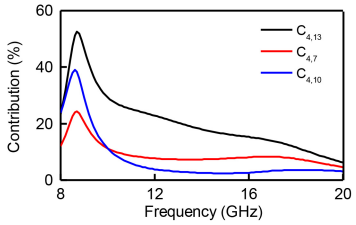

Fig. 15. Contributions of source current in other stages.

of the amplifier with CPW-type transistors, followed by an AC simulation. Since the EM simulated layout and the utilized models of the transistors are all linear, the magnitude of excitation voltage never causes nonlinearity. Here, we set this voltage to 1 V.

The simulated voltage at port 4 is shown in Fig. 14. The red line is the total voltage at port 4 according to (3). The black line is the magnitude of voltage induced by stage 4 ($Z_{4,13} i_{13}$), which has the largest value. The smallest value $Z_{4,13}$ multiplied by a factor of i_{13} becomes the largest contribution. Fig. 15 shows the calculated contributions of source current of stage 2, 3, and 4, among which stage 4 has the largest contribution. If the MS-type transistor is used in stage 4, the source ground via is removed from the layout, so there is no port 13 in the EM simulation. Equivalently, $Z_{4,13} = 0$. So a large portion of v_4 is lost. This also explains why the transistor type of the last stage can significantly change S_{11}. Usually, the last stage hardly affects S_{11} in the schematic.

The amplifier performance is sensitive to the source impedance of each transistor. Now, the contribution due to the coupling effect of stage 4 can be very high, so this effect must be accounted for in the EM simulation. For a CPW-type transistor, the EM-circuit co-simulation calculates the effect of their source ground via. However, this effect is ignored in the MS-type transistor. Then, the simulation accuracy cannot be guaranteed if the amplifier has a high gain and large current. The source vias' intercoupling effects of stage 2, 3, and 4 upon stage 1 are not the only intercoupling paths within this

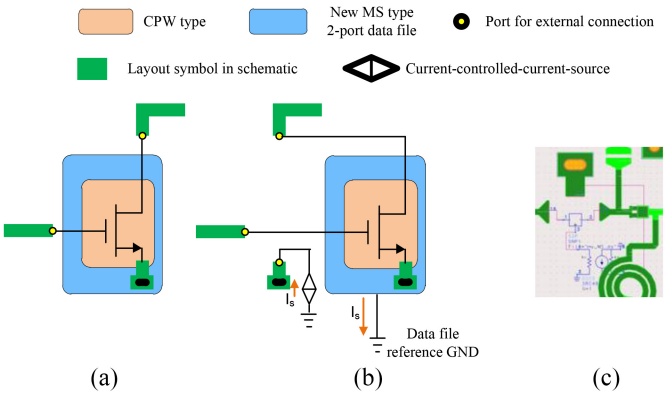

Fig. 16. Configuration of MS-type transistor in schematic part of EM-circuit co-simulation. (a) Conventional, (b) proposed, and (c) implementation of proposed configuration in ADS.

layout. For instance, the source of stage 2 is also affected by the backside vias of stage 1, 3, and 4, which can influence the performance and be analyzed in a similar way. Anyway, the standard method to treat the MS-type transistor model in layout EM simulation can cause significant error due to ignoring the source via on the substrate.

B. Proposed Method

In order to account for the source via of the MS-type transistor in layout EM simulations when the MS type is used, adding a backside via in the stage-4 layout of Fig. 9, which results in the same layout as in Fig. 8, can be adopted. The conventional and modified configurations in the schematic are shown in Fig. 16(a) and (b), respectively. Fig. 16(c) shows an implementation of the proposed configuration in ADS, where the entire amplifier layout is simulated. This configuration is different from the CPW-type and conventional MS-type configuration. A current-controlled-current-source is used to inject the source current of the transistor into the source via layout. In this way, the effect of the source structure can be accounted for in EM-circuit co-simulations.

Now, if the MS-type transistor is used, the simulated performance with this proposed method is shown as red curves in Fig. 17. The simulated S_{11}, S_{21}, and S_{12} almost overlap with the results of the layout in Fig. 8 (all CPW-type transistors). The discrepancy between S_{22} also becomes smaller than in Fig. 10. Therefore, the simulation accuracy is significantly improved. These are the simulation results with the layout shown in Figs. 7–9 whose MS-type model is defined in this article. In practice, MMIC designers always use the MS-type model provided by foundries. The proposed method can also be applied for the circuit layout in Fig. 3. Then, multiple backside vias should be considered in the layout EM simulation.

As shown in Fig. 1(b), there are three backside vias in the MS-type transistor model and all of them are removed from the layout for EM-circuit co-simulation. These three backside vias are now added to their original locations in the layout. Additional ports are assigned to the backside vias for current injection, as shown in Fig. 18. It is assumed that A % of the

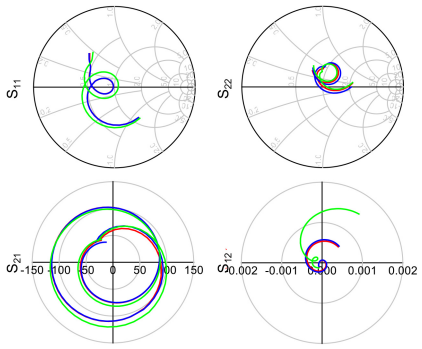

Fig. 17. Simulated performance with proposed method. Blue line: all transistors are CPW type; green line: the last stage uses MS type; and red line: the last stage uses MS type with the proposed backside via layout on the substrate.

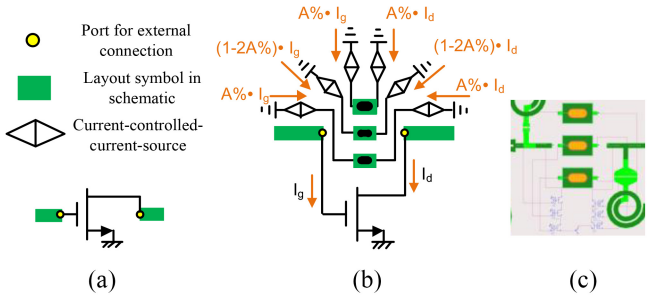

Fig. 18. Configuration of MS-type model in schematic part for EM-circuit co-simulation. (a) Conventional, (b) proposed, and (c) implementation of proposed configuration in ADS.

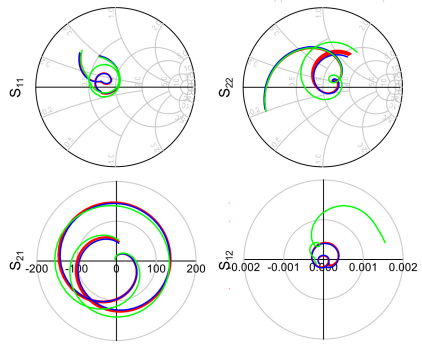

Fig. 19. Simulated performance with proposed configuration of Fig. 3(b). Blue line: all transistors are CPW type; green line: the last stage uses MS type; and red line: the last stage uses MS type with the proposed via hole and the value of A is swept.

source current of the transistor goes through the upmost and bottom vias, so (100-2A) % of the source current goes through the middle via, as depicted in Fig. 18(b). The value of A is swept from 0 to 50 with a step of 10. The simulated results are shown in Fig. 19.

As shown in Fig. 19, varying A does not significantly change the simulated performance. Designers can set the current evenly distributed in the three vias. Compared with Fig. 5, the simulated results are much closer to that of the amplifier with all CPW-type transistors. The simulation accuracy is highly improved. This method can also be used when the

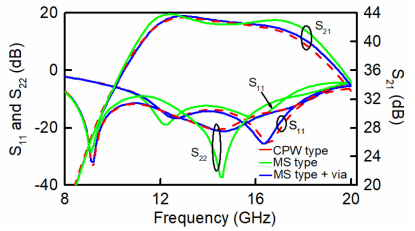

Fig. 20. *S*-parameters in dB of the amplifier in Fig. 3.

MS-type transistors have different numbers of backside vias. The *S* parameters of Fig. 19 are shown in dB in Fig. 20.

The magnitude differences of simulated *S*-parameters can be seen in Fig. 20. Two expressions can be used to quantify both the magnitude and phase differences of the *S*-parameters

$$D = \frac{1}{N}\sum_{k=1}^{N}\left|S_{i,j} - S_{i,j}^{\text{ref}}\right| \tag{5}$$

$$D_{\max} = \max\left(\left|S_{i,j} - S_{i,j}^{\text{ref}}\right|\right) \tag{6}$$

where N is the number of frequency points in the results, and $S_{i,j}$ $(i, j = 1, 2)$ are the *S*-parameter of the amplifier, whose last stage utilizes an MS-type transistor. $S^{\text{ref}}{}_{i,j}$ are the reference *S*-parameters, which are *S*-parameters of the amplifier with all CPW-type transistors. Both $S_{i,j}$ and $S^{\text{ref}}{}_{i,j}$ are functions of frequency. D is an average over the selected frequency band (8–20 GHz) and it depends on the band. The max deviation, $D_{\max}$, is defined and it is independent on the band.

In the simulation experiment, in which the new MS-type model shown in Fig. 6(b) has exactly the same S-parameters as a CPW-type transistor plus backside via, this kind of discrepancy is effectively reduced by the proposed method, as shown in Table I where the reference *S*-parameters reflect the performance of the amplifier in Fig. 8.

In practical MMIC amplifier design, CPW-type and MS-type models are provided by the foundry. The transistor type can be chosen according to the performance and circuit configuration requirements. However, the source via of the MS-type transistor model has been ignored in the MMIC circuit layout and EM simulation for a long time because the source via is included in the MS-type transistor model. Hence, the conventional method of EM-circuit co-simulation also shows significant discrepancy (Fig. 5). Usually this deviation is not acceptable: the magnitude of S_{11} is less than 1 for a stable amplifier, while $D_{\max}$ of S_{11} can be around 0.1. Furthermore, amplifiers often require $|S_{11}| \leq 0.3$ $(-10$ dB), which means the magnitude of S_{11} should be smaller than 0.3. The proposed method can reduce the deviation from 0.13 to 0.02, as shown in Table II.

IV. Applicability Analysis

The ignorance of the backside via of the MS-type transistor can cause simulation error for most MMIC processes. The typical substrate thickness of GaAs processes is from 50 to 100 μm (100-μm substrate is used in this article). A simulation is carried out on three different substrate thicknesses to investigate the intercoupling effect among the via holes. The circuit layout in Fig. 8 is resimulated, in which the substrate thickness changes from 5 to 50 μm and to 150 μm. Intuitively, the thicker the substrate, the longer the backside via will be. Therefore, the coupling effect is stronger. Table III lists the D and $D_{\max}$ of the simulation with different substrate thicknesses. Although the error tends to be smaller for thinner substrates, it always exists. The problem is common to all these GaAs MMIC processes and other MMIC processes such as the InP MMIC process when an MS-type transistor is used.

The coupling effects always exist, regardless of frequency, separation distance, etc. Two backside vias are placed in a layout, and separated from 500 to 3000 μm as shown in Fig. 21. Simulated from 1 to 30 GHz, Z_{21} linearly increases as the frequency increases, and increases faster when the two structures get closer (separation distance decreasing).

This kind of structure in Fig. 21 can be easily found in MMIC layouts such as amplifiers. For example, the two backside vias can be at the source of two transistors in different stages. In this case, assume the right backside via in the structure corresponds to the latter stage transistor. Therefore, the

TABLE I
Calculated *D* and *Dmax* Between Circuit Layouts of Figs. 8 and 9

	Conventional method	Proposed method	Discrepancy reduction
D of S_{11}	0.065	0.002	96.9%
$D_{\max}$of S_{11}	0.081	0.009	88.9%
D of S_{22}	0.055	0.029	47.3%
$D_{\max}$of S_{22}	0.094	0.058	38.3%
D of S_{21}	7.232	3.882	46.3%
$D_{\max}$of S_{21}	12.0	9.89	17.6%
D of S_{12}	4.353×10^{-4}	2.121×10^{-5}	95.1%
$D_{\max}$of S_{21}	9.34×10^{-4}	3.80×10^{-5}	95.9%

TABLE II
Calculated *D* and *Dmax* Between Circuit Layouts of Fig. 3(a) and (b)

	Conventional method	Proposed method	Discrepancy reduction
D of S_{11}	0.088	0.010	88.6%
$D_{\max}$of S_{11}	0.13	0.02	84.6%
D of S_{22}	0.092	0.025	72.8%
$D_{\max}$of S_{22}	0.22	0.05	77.3%
D of S_{21}	18.465	6.879	79.0%
$D_{\max}$of S_{21}	37.16	11.38	69.4%
D of S_{12}	7.035×10^{-4}	2.724×10^{-5}	96.1%
$D_{\max}$of S_{12}	2×10^{-3}	6.78×10^{-5}	96.6%

TABLE III
Calculated *D* and *Dmax* for Different Substrate Thickness

Substrate thickness	5 micron	50 micron	50 micron (high gain)	100 micron	150 micron
Gain	40 dB	40 dB	50 dB	40 dB	40 dB
D of S_{11}	0.0000144	0.016	0.06	0.065	0.148
$D_{\max}$of S_{11}	0.0000284	0.019	0.076	0.081	0.206
D of S_{22}	0.000265	0.018	0.06	0.055	0.119
$D_{\max}$of S_{22}	0.000395	0.024	0.086	0.094	0.226
D of S_{21}	0.002	1.46	17.6	7.232	16.6
$D_{\max}$of S_{21}	0.004	2.10	27.9	12.0	33.7
D of S_{12}	0.00000052	0.00011	0.0001	0.00044	0.001
$D_{\max}$of S_{21}	0.00000084	0.00022	0.00021	0.00093	0.002

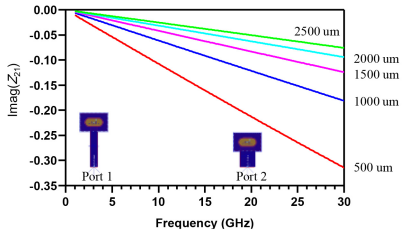

Fig. 21. Simulated layout to study separation distance between two via holes and the simulated Z parameters.

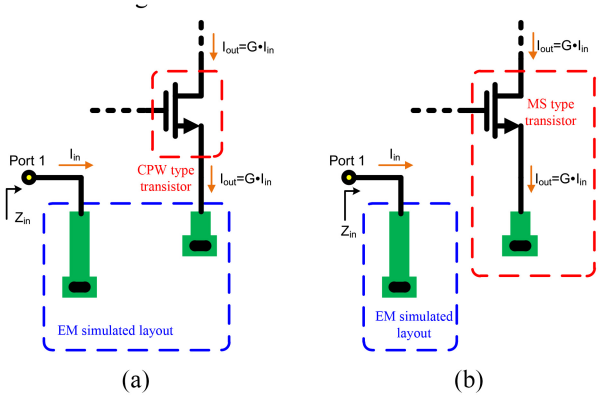

Fig. 22. EM-circuit co-simulation of the layout in Fig. 21 when (a) the latter stage transistor is CPW type and (b) MS type.

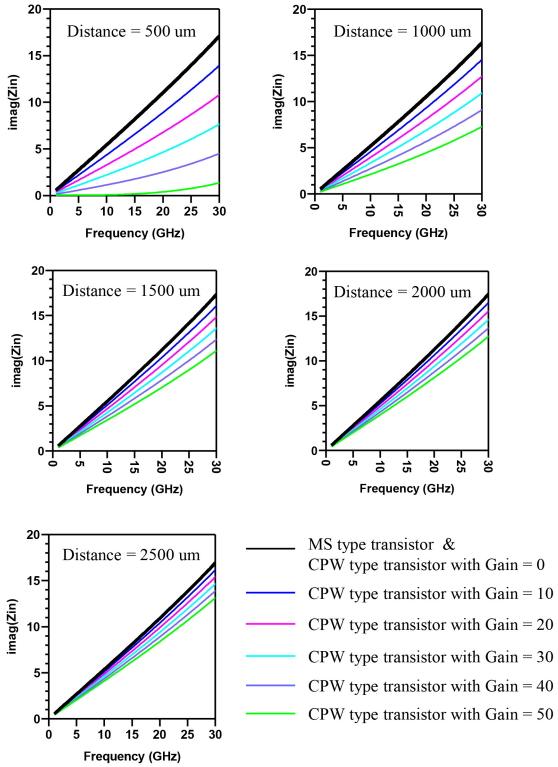

Fig. 23. Input impedance of Fig. 22 with different separation distance. The real part is very small compared with the imaginary part, so it is not displayed.

current flowing into the right backside via is larger, compared with the current flowing into the left backside via. The current gain (the ratio of I_{out} to I_{in} in Fig. 22) is defined as G. If the transistor in the latter stage is a CPW type, then both backside structures are simulated in EM simulation, as in Fig. 22(a). However, if the transistor in the latter stage is an MS type and the conventional simulation setup is used, the right source via structure is NOT simulated in the EM simulation. Fig. 22(b) shows the circuit where the coupling effect is ignored, which leads to different simulation results. It should be noted that the MS-type transistor in Fig. 22(b) is identical to the CPW-type transistor PLUS the right source via in Fig. 21.

The influence of the ignorance of the coupling effect on the input impedance deviation is studied by EM-circuit co-simulation: the input impedance looking into port 1 in Fig. 22 (Z_{in}) is observed. The real part is very small, so only the imaginary part is shown in Fig. 23. There are five-group plots for five different separation distances. At each separate distance (varying from 500 to 2500 μm), the input impedance of the circuit with the CPW-type transistor as in Fig. 22(a) is depicted by the colored lines while the current gain varies from 0 to 50 in steps of 10. As can be seen, the input impedance changes with current gain and the separation distance between the two vias. At the shortest distance of 500 μm, the current (gain) has stronger influence on the impedance than at longer distances, which is enhanced with increasing frequency.

For the MS-type transistor case of Fig. 22(b), the input impedance as shown in black lines in Fig. 23 will not change when the current gain G changes from 0 to 50, which is the same impedance as in the CPW transistor case when $G = 0$. Furthermore, when the separation distance of two via-holes in the MS-type transistor case changes from 500 to 2500 μm, the input impedance shows no change at all. All of the above is because there is no coupling effect included in EM layout simulation.

With the same current gain and the same separation distance, Z_{in} of the MS-type transistor case is supposed to be the same as Z_{in} of the CPW-type transistor case, because their circuit structures are the exact same. However, we can clearly see the difference in Fig. 23. The differences are due to the ignorance of the coupling effect in the MS-type transistor layout. In Fig. 23, when the black line is farther away from the colored lines, the error is greater.

Comparing the five figures in Fig. 23, it is found that when the separate distance increases and the current gain is fixed, the input impedance change becomes smaller. However, if the current gain is large enough, the deviation for large separation distance can definitely increase to a higher level.

On the other hand, it is found that the deviation is smaller at lower frequencies. But it can still be amplified to a higher level by a higher gain. The derivations of the reflection coefficient (7) including the source via coupling and inequality (8) are given in the Appendix. When inequality (7) is satisfied, $|S_{11}|$ of the amplifier changes less than 0.1 due to the via coupling

$$\frac{\left|g_m + j\omega C_{gs}\right|}{\left|g_m\left(\frac{2L_s \cdot \text{dist}}{G \cdot l_m} + 1\right) + j\omega C_{gs}\right|} \leq 0.1. \tag{7}$$

If the current gain is assumed to be a real number for simplicity, (7) can be rewritten as

$$100 < \left(\frac{2L_s \cdot \text{dist}}{G \cdot l_m} + 1\right)^2 \tag{8}$$

where ω is the angular frequency, C_{gs} is the parasitic capacitance between the gate and source of the transistor, g_m is the transconductance, G is the current gain, dist is the backside via separation distance, and L_s is the self-inductance of the source inductor. The mutual inductance L_m is simulated and approximated by l_m/dist and l_m is a fitting coefficient, which is estimated to be $\pm 10^{-15}$ Hm for 100-μm thick GaAs substrate. As a rule of thumb, when the operation frequency is lower than 10 GHz, and the gain is less than 30 dB, the source via of the MS type transistor can be treated like a conventional layout EM simulation. At lower frequencies, the gain threshold can be higher.

V. Conclusion

For a long time, the source via of the MS-type transistor model has been ignored in the MMIC circuit layout and EM simulation because the source via is included in the MS-type transistor model and cannot be implemented in the conventional layout process. The circuit layout EM-simulation cannot account for the intercoupling effect of the source via in the conventional MMIC layout EM simulation process.

By simulation experiment and analysis, the intercoupling effect of the backside via omitted in MS-type transistors is found to be able to cause a significant error in amplifier EM-circuit co-simulation. A new simulation setup of circuit layout is proposed to implement the source via of MS-type transistor models in the MMIC amplifier layout and include the coupling effect in the EM-circuit co-simulation. It is demonstrated that this new layout and simulation processing for MS-type transistors significantly reduces the error and improves the EM-circuit co-simulation accuracy, making the simulated results more reliable. A common MMIC amplifier usually has fewer than five transistors [4], [17], [18]. Therefore, our two examples are 4-stage amplifiers. For simplicity, we use the MS-type transistor in the fourth stage to verify the problem and demonstrate our solution. This method is not limited to any number of MS-type transistors. The intercoupling effect of the transistor source via is investigated on the correlation with frequency, current gain, via separation distance, and substrate thickness.

Appendix

To analyze the data in Fig. 23, the impedance deviation is defined as

$$\Delta Z_{\text{in}} = Z_{in\_\text{CPW}} - Z_{in\_MS} \tag{9}$$

where Z_{in_CPW} is the impedance when a CPW type transistor is used and Z_{in_MS} is the impedance when an MS type transistor is used (conventional simulation setup). In Fig. 24(a), we have

$$Z_{in\_\text{CPW}} I_1 = j\omega L_1 I_1 + j\omega L_m \cdot (G \cdot I_1) \tag{10a}$$

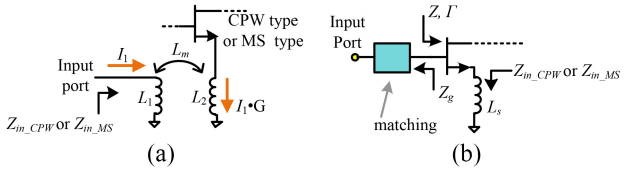

Fig. 24. (a) Illustration of calculating the impedance deviation. (b) Transistor with source inductance in the first stage of a microwave amplifier.

$$Z_{in\_MS} I_1 = j\omega L_1 I_1. \tag{10b}$$

Therefore

$$\Delta Z_{\text{in}} = j2\pi \cdot f \cdot G \cdot L_m = j2\pi \cdot f \cdot G \cdot \frac{l_m}{\text{dist}} \tag{11}$$

where all parameters are defined in Section IV.

For a transistor in an amplifier as shown in Fig. 24(b), the impedance Z looking into the gate can be calculated as [19]

$$Z = \frac{g_m L_s}{C_{gs}} + j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right). \tag{12}$$

On the other hand, the impedance looking into the matching network from the gate is defined as Z_g. If the coupling is ignored, the matching network would be designed properly so that the impedance Z_g is the conjugate of Z in (12). In this case, the reflection coefficient is zero and Z_g should be

$$Z_g = Z^* = \frac{g_m L_s}{C_{gs}} - j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right). \tag{13}$$

But in fact, the mutual coupling effect will add extra impedance (ΔZ_{in}) to the source. Therefore, (12) needs to be rewritten as

$$Z = \frac{g_m(j\omega L_s + \Delta Z_{\text{in}})}{j\omega C_{gs}} + (j\omega L_s + \Delta Z_{\text{in}}) + \frac{1}{j\omega C_{gs}}. \tag{14}$$

Correspondingly, the reflection coefficient Γ (referring to the complex impedance Z_g) is

$$|\Gamma| = \left|\frac{Z - Z_g^*}{Z + Z_g}\right| = \frac{\left|g_m + j\omega C_{gs}\right|}{\left|g_m\left(\frac{2L_s \cdot \text{dist}}{G \cdot l_m} + 1\right) + j\omega C_{gs}\right|}. \tag{15}$$

In conclusion, the magnitude of the reflection coefficient is

$$|\Gamma| = \begin{cases} 0, & \text{ideal matching when the coupling is not considered} \\ \dfrac{\left|g_m + j\omega C_{gs}\right|}{\left|g_m\left(\frac{2L_s \cdot \text{dist}}{G \cdot l_m} + 1\right) + j\omega C_{gs}\right|}, & \text{when the coupling is considered.} \end{cases} \tag{16}$$

If the coupling is ignored and a perfect matching network is designed to make $\Gamma = 0$, the actual reflection coefficient with coupling effect would be different from zero. The magnitude of the change is written as (17). The change is dependent on the current gain, the separation distance of vias, substrate thickness, and frequency; note that the source inductor L_s in the design is also related to frequency

$$|\Delta\Gamma| = |\Gamma| = \frac{\left|g_m + j\omega C_{gs}\right|}{\left|g_m\left(\frac{2L_s \cdot \text{dist}}{G \cdot l_m} + 1\right) + j\omega C_{gs}\right|}. \tag{17}$$

When the magnitude in (17) is supposed to be smaller than 0.1, which means the actual Γ is better than -20 dB,

inequality (7) should be satisfied. For simplicity, if the current gain G is assumed to be real, then (7) is equivalent to

$$\frac{\sqrt{g_m^2+\omega^2 C_{gs}^2}}{\sqrt{g_m^2\left(\frac{2L_s\cdot \mathrm{dist}}{G\cdot l_m}+1\right)^2+\omega^2 C_{gs}^2}} \le 0.1. \tag{18}$$

Inequality (18) can be rewritten as (19) by algebra transformations and inequality scaling

$$\begin{aligned} 100g_m^2 &\le g_m^2\left(\frac{2L_s\cdot \mathrm{dist}}{G\cdot l_m}+1\right)^2 - 99\omega^2 C_{gs}^2 \\ &< g_m^2\left(\frac{2L_s\cdot \mathrm{dist}}{G\cdot l_m}+1\right)^2. \end{aligned} \tag{19}$$

When the leftmost and right most parts of (19) are both divided by ${g_m}^2$, inequality (8) can be obtained. It should be noted that in (19), $99\omega^2{C_{gs}}^2$ is usually much smaller than ${g_m}^2(2L_s\mathrm{dist}/(Gl_m)+1)^2$.

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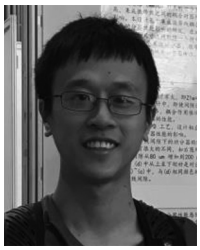

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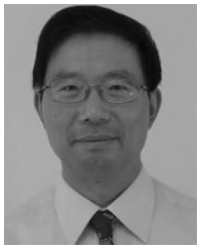

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