# Performance of Frame Synchronization in Packet Transmission Using Bit Erasure Information

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***Abstract*—The probability of successful frame sync in packet transmission using bit erasure information is compared to this probability when erasure information is ignored. For a given bound on false alarms, a significant improvement is found on AWGN channels if an erasure zone is added to the receiver. An improvement is also found for channels where the presence of jamming or other interference is detected and erased by the receiver.**

**An expression for the probability of frame synchronization in packet transmission is derived as a function of the bit error and erasure probability, the amount of overlap and the number of bit errors/erasures which are tolerated in the frame sync word.**

## I. INTRODUCTION

DATA transmission systems operating in burst or packet mode using data link protocols such as HDLC require that reliable frame synchronization be achieved since the meaning of each bit in a frame or packet depends on its position. Thus, each packet begins with a unique work or marker for frame synchronization preceded by a preamble for bit synchronization. On channels corrupted by noise or interference, it is desirable to tolerate some bit errors and erasures in the marker in order to increase the frame sync reliability.

This paper examines the performance of frame synchronization on a burst mode data link in detail. It is assumed that the demodulator makes hard decisions on each bit in the data stream. The objective is to calculate the probability of successful and false frame sync for packet transmission with errors-only and errors-and-erasures decoding. Thus, quantitative data are established which permits a system designer to consider adding erasure detection to the receiver and trade off the additional cost with the performance improvement. Erasures may be declared when the receiver test statistic (detector output) is close to the decision threshold and falls within the erasure zone of the receiver. Alternately, erasures may be declared when large disturbances caused by jamming or interference are detected at the receiver.

Frame synchronization techniques are described in [1], [10]. Errors-and-erasures decoding is considered in [2] in the context of periodic frame sync words embedded in a continuous data stream, but [2] does not consider packet transmission.

In Section II, the data frame format is reviewed for reference, and the method of synchronization is outlined.

In Section III, a general expression is derived for the probability of achieving frame synchronization as a function of three variables: the probabilities of bit error and erasure, the overlap between the incoming data stream and the frame sync word, and the number of bit errors/erasures which are tolerated in the frame sync word. This expression is used to determine the probability of false synchronization in an incorrect position.

In Section IV, the probability $P_{\text{SYNC}}$ of successful frame sync with errors-and-erasures decoding is compared to $P_{\text{SYNC}}$ with errors-only decoding, given a fixed upper bound on the probability of false frame sync $P_{FA}$. The bound on $P_{FA}$ is required because if the decoder falsely declares frame synchronization just prior to the correct epoch then a frame will be lost which otherwise would have been received correctly. The bound on $P_{FA}$ is established as a function of the desired message success rate and determines the maximum number of errors and erasures that may be tolerated in a marker.

In Section V, numerical results are presented for two example data frame formats. The results show that for a given bound on $P_{FA}$, a significant improvement in $P_{\text{SYNC}}$ may be obtained by using erasure information.

## II. DATA FRAME FORMAT AND SYNCHRONIZATION METHODS

The frame format is illustrated in Fig. 1. Each frame includes a $N_p$-bit preamble for bit synchronization (usually an alternating 1010 pattern ending in 0), a $N_s$-bit frame synchronization sequence (unique word, marker), and an information field containing address and control bits, data bits and an error detection or correction code.

For illustrative purposes, we present numerical results for a 16 b marker with minimum sidelobes when preceded by preamble [4], [6] ($B433$ in hexadecimal notation), and compare to a 16 b marker made up of two high-level data link control (HDLC) [13] flags ($7E7E_{hex}$). For these two markers, $N_s = N_p = 16$. Results are also presented for a 40 b marker ($07092A446F_{hex}$) recently adopted as a standard for packet transmission [3] where $N_s = N_p = 40$.

Two different methods to obtaining frame synchronization are considered in the sequel. In the first method, referred to as the "DCD first" method, the receiver searches for bit synchronization first, taking advantage of the frequent data transitions in the preamble, and declares successful bit sync by raising a data carrier detect (DCD) or lock detector [5] flag. When bit sync is achieved, the receiver outputs a binary data symbol $\hat{a}$ or an erasure once per code period. Frame synchronization is declared when the current bit $\hat{a} \in \{0, 1, \text{erasure}\}$ plus the previous $N_s - 1$ b match the marker in Fig. 1 within a specified bit error and erasure tolerance. Since it is not known *a priori* at which point in the preamble bit sync was achieved, the marker search is performed in successive positions of the marker until a match is found or $N_p$ positions have been tested.

In the second method, referred to as the "no DCD" method, the receiver searches for frame synchronization at all times, regardless of the state of the DCD flag. In the absence of signal

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Fig. 1. Data link frame format.

(noise only), the receiver output is a random sequence of bits or erasures.

## III. Marker Tolerance of Bit Errors and Erasures

In this section, the probability of false synchronization in an incorrect position is calculated as a function of the specified error and erasure tolerance, the bit error and erasure probabilities, and the number of disagreements $h_o(n)$ (Hamming distance) between the marker and the received data in the absence of errors.

### A. Errors Only

An expression for the false sync probability $P_A(h, n, h_o(n))$ in terms of the marker length $N_s$, the amount of overlap $n \leq N_s$, the error tolerance $h$ (maximum number of disagreements) and the bit error probability $p_s$ is given in [1], [10] when the marker is preceded by random data or noise. The set of disagreements $\{h_o(n)\}$ is related to the correlation function [1] and will depend on the specific marker in use.

When there is a preamble of length $N_p$, then the number of disagreements $h_o(n)$ in the absence of errors is known for all $n \geq N_s - N_p$. For this case, the expression in [1] is modified to

$$\begin{aligned}&\text{Prob(acquisition at time } t \text{ with overlap } n)\\&\quad= \text{Prob(}h\text{ or fewer disagreements with overlap } n)\\&\quad= P_B(h, N_s, h_o(n))\\&\quad= \sum_{j=0}^{h} \sum_{\ell=\max(0,j-h_o)}^{\min(j,N_s-h_o)} \binom{N_s - h_o}{\ell} (1-p_s)^{N_s-h_o(n)-\ell} p_s^{\ell}\\&\qquad \cdot \binom{h_o}{j-\ell} (1-p_s)^{j-\ell} p_s^{h_o(n)-j+\ell}. \qquad (1)\end{aligned}$$

The first term of (1) represents the probability of obtaining $\ell$ errors in the $N_s - h_o(n)$ bits which agree to add to the disagreements, and the second term represents the probability of obtaining $j - \ell$ correct bits in the $h_o$ bits which disagree to add to the disagreements. If the total number of disagreements is $h$ or less, then acquisition occurs.

### B. Errors and Erasures

In this section we derive new expressions corresponding to (1) when bit erasures are considered. We define the following:

$p$ = bit error probability (signal present),
$s$ = bit erasure probability (signal present),
$q = 1 - p - s$,
$h$ = error tolerance, and
$h_x$ = erasure tolerance.

For this case, $P_B(h, h_x, N_s, h_o(n))$ may be calculated using probability generating functions according to

$$P_B(h, h_x, N_s, h_o(n)) = \sum_{j=0}^{h} \sum_{k=0}^{h_x} g_{jkn}, \qquad (2)$$

where the $g_{jkn}$ are given by

$$\begin{aligned}\sum_{j=0}^{N_s} \sum_{k=0}^{N_s-j} g_{jkn} z_1^j z_2^k &= G_n(z_1, z_2)\\&= G_{h_o(n)}(z_1, z_2) \cdot G_{N_s-h_o(n)}(z_1, z_2), \qquad (3)\end{aligned}$$

with

$$G_{h_o(n)}(z_1, z_2) = (p + qz_1 + sz_2)^{h_o(n)} \qquad (4)$$

for the $h_o(n)$ bit which disagree or are erased, and

$$G_{N_s-h_o(n)}(z_1, z_2) = (q + pz_1 + sz_2)^{N_s-h_o(n)} \qquad (5)$$

for the $N_s - h_o(n)$ bits which agree or are erased.

$P_B(h, h_x, N_s, h_o(n))$ may be written

$$\begin{aligned}&P_B(h,h_x,N_s,h_o(n))\\&\quad= \text{Prob(acquisition at time } t \text{ with overlap } n)\\&\quad\phantom{=}\ \text{Prob(}h\text{ or fewer disagreements and } h_x \text{ or fewer erasures with overlap } n)\\&\quad= \sum_{j=0}^{h} \sum_{k=0}^{h_x} \sum_{m=\max(0,k-h_o)}^{\min(k,N_s-h_o)} \sum_{\ell=\max(0,j-h_o+k-m)}^{\min(j,N_s-h_o-m)}\\&\qquad \cdot \binom{N_s - h_o}{\ell, m} q^{N_s-h_o(n)-\ell-m} p^{\ell} s^{m}\\&\qquad \cdot \binom{h_o}{j-\ell, k-m} q^{j-\ell} p^{h_o(n)-j+\ell-k+m} s^{k-m} \qquad (6)\end{aligned}$$

where

$$\binom{h_o}{\ell, m} = \frac{h_o!}{\ell!\, m!\, (h_o - \ell - m)!}. \qquad (7)$$

The first term represents the probability of obtaining $\ell$ errors and $m$ erasures in the $N_s - h_o$ bits which agree, and the second term represents the probability of obtaining $j - \ell$ correct bits and $k - m$ erasures in the $h_o$ bits which disagree. If the total number of disagreements is $h$ or less and the total number of erasures is $h_x$ or less, then acquisition occurs.

The probability $P_{FS}$ of frame sync when testing in the correct position $n = N_s$ is given by

$$P_{FS} = P_B(h, h_x, N_s, 0) = \sum_{i=0}^{h} \sum_{j=0}^{h_x} \binom{N_s}{i, j} p^i s^j q^{N_s-i-j}. \qquad (8)$$

Computation of $P_B(h, h_x, N_s, h_o(n))$ requires that both the erasure tolerance $h_x$ and the error tolerance $h$ be selected. Following [2], we select $h$ and set $h_x = \min[2(h - j), N_s - j]$, so that $k + 2j \leq 2h$ and thus twice as many erasures as errors are tolerated.

The probability $P_{FA2,n}$ of random data or noise looking like the marker when the signal is absent is given by

$$P_{FA2,n} = \sum_{i_1=0}^{h} \sum_{i_2=0}^{h_x} \binom{N_s}{i_2, i_1} p_n^{i_1} s_n^{i_2} q_n^{N_s-i_1-i_2} \qquad (9)$$

where $s_n$ is the probability of a bit erasure when the signal is absent, and $p_n = q_n = (1 - s_n)/2$ is the probability of a match or mismatch when the signal is absent.

### *C. Probability of Bit Error and Erasure*

Expressions for $p, s, p_n$, and $s_n$ will depend on how erasures are declared. We define System 1 in which bit erasures are declared when the receiver detects a signal close to the decision threshold which would cause the bit decision to be unreliable. Alternately, we define System 2, in which erasures are declared when jamming or other disturbance is detected.

In System 1, the channel is perturbed by AWGN only. For purposes of illustration, we consider binary antipodal signaling with received signal energy $E_b$ per bit where the receiver test statistic $D$ is the output of a matched filter sampled at each bit time. Thus $D$ is a Gaussian random variable with mean $+\sqrt{E_b}$ or $-\sqrt{E_b}$ (depending on whether a 1 or 0 was transmitted), and noise variance $\sigma^2 = N_o/2$ [12]. Erasures are declared if $D$ falls within the erasure zone $|D| < b$. If perfect bit synchronization is available, we may write

$$\begin{aligned} p &= Q\left[\sqrt{2E_b/N_o} + e\right] \\ s &= Q\left[\sqrt{2E_b/N_o} - e\right] - p \\ q &= 1 - Q\left[\sqrt{2E_b/N_o} - e\right] \end{aligned} \tag{10}$$

where $e = b\sqrt{2/N_o}$, and $Q(\alpha) = \frac{1}{\sqrt{2\pi}} \int_\alpha^\infty e^{-t^2/2}\,dt$.

If the signal is absent and there is noise only, then $E_b = 0$ and

$$\begin{aligned} p_n &= Q[e] \\ s_n &= Q[-e] - p_n \\ q_n &= 1 - Q[-e] = p_n. \end{aligned} \tag{11}$$

Expressions for $p, s, p_n$, and $s_n$ may in principle be derived for other receiver designs with an erasure zone, and for receivers with imperfect bit synchronization. For example, a polarity coincidence detector which operates on several independent hard-limited samples per bit is considered in [11].

To determine the performance improvement available by using erasures in System 1, we compare to a system in which the erasure zone $e = 0$, $p = Q\left[\sqrt{2E_b/N_o}\right]$, $p_n = 0.5$, and $s = s_n = 0$.

In System 2, the channel is subject to large disturbances, jamming or interference which can be reliably detected by the receiver, and the bits received during the disturbance are simply erased. For this case the probability of erasure is independent of the presence or absence of the desired signal, and its value depends only on the amount of interference. The largest value of interest is $s = s_n = 0.25$ [2]. Following [2], $p$ is set to $Q\left[\sqrt{2E_b/N_o}\right](1 - s)$. If the signal is absent, then $q_n = p_n = (1 - s_n)/2$.

To determine the performance improvement available by using erasures, in System 2, we compare to an alternative scheme in which the erasure information is ignored [2]. It is assumed that the bit which would have been erased with probability $s$ is equally likely to be correct or incorrect, and thus the bit error probability with signal present is replaced with $p + s/2$, the bit erasure probability is set to 0, and the probability of a match or mismatch with signal absent is set to 0.5.

## IV. PERFORMANCE CALCULATIONS

In this section, the synchronization performance in terms of the probabilities of successful frame sync $P_{\text{SYNC}}$, frame sync false alarm $P_{FA\text{SYNC},n}$ with signal absent (noise only) and $P_{FA\text{SYNC},d}$ with signal present is determined for a fixed length preamble/marker as a function of $p, s, p_n$, and $s_n$. The analysis is identical for both System 1 and System 2.

The probability $P_{\text{success}}$ of successful packet transmission depends also on the probability $P_{\text{BIT}}$ of successful bit sync with the $N_p$ bit preamble. For the "DCD first" sync method the probability $P_{F\text{BIT},n}$ of false bit sync in noise must also be considered, as outlined in Section V. $P_{\text{BIT}}$ as well as $P_{F\text{BIT},n}$ are determined by the modem bit synchronizer design and $E_b/N_o$. In general, $P_{\text{BIT}}$ is designed to be as high as possible with an upper bound on $P_{F\text{BIT},n}$.

Values of the thresholds $e$ and $h$ are optimized to maximize $P_D = P_{\text{BIT}} \cdot P_{\text{SYNC}}$ subject to upper bounds on both $P_{F\text{BIT},n}$ and $P_{FA\text{SYNC},n}$ to be specified in Section V.

The probability $P_{\text{SYNC}}$ of successful frame sync will depend on two factors: at which point in the $N_p$ bit preamble bit sync occurred and correct bits begin to be received (i.e., the value of overlap $n = n_f \in \{N_s - N_p, N_s\}$ at the first frame sync trial), and the values of $P_B(h, N_s, h_o(n))$, $n \geq n_f$ and the specific marker in use. $P_{\text{SYNC}}$ may be bounded as follows:

$$P_{FS} - P_{FA\text{SYNC},d} \leq P_{\text{SYNC}} \leq P_{FS} \tag{12}$$

where

$$P_{FA\text{SYNC},d} = \sum_{n=N_s-N_p}^{N_s-1} P_B[h, N_s, h_o(n)] \tag{13}$$

is an upper bound on the probability of false frame sync at an incorrect position with signal present. For a specific marker, $P_{FA\text{SYNC},d}$ will depend on $N_s, p, s, h$, and $h_o(n)$. For a well chosen marker [6] and reasonable choice of $h$ and $E_b/N_o$, $P_{FA\text{SYNC},d} \ll P_{FS}$ and $P_{\text{SYNC}}$ is approximately the probability of successful frame sync when testing in the correct position. Thus, $P_{\text{SYNC}}$ is given by the probability of obtaining $h$ or fewer bit errors and $h_x$ or fewer erasures in a sequence of $N_s$ bits:

$$P_{\text{SYNC}} \cong P_{FS}$$

where $P_{FS}$ is given by (8).

For the "DCD first" sync method, the probability of a false alarm $P_{FA,n}$ when the signal is absent is the combined probability that a false DCD occurs and also a sequence of marker bits are imitated by a random sample pattern within the error tolerances. A false frame sync alarm will occur with probability $P_{FA\text{SYNC},n}$ if the marker is imitated by noise in one of the $N_p$ positions tested following false bit sync in noise. Thus

$$\begin{aligned} P_{FA,n} &= \text{Prob}\{\text{false bit sync in noise}\} \\ &\quad \cdot \text{Prob}\{\text{at least one successful (false) frame sync in} \\ &\quad \text{noise out of the } N_p \text{ positions tested}\} \\ &= P_{F\text{BIT},n} \cdot P_{FA\text{SYNC},n}. \end{aligned} \tag{14}$$

For $h = 0$, $P_{FA\text{SYNC},n}$ is given by the probability of a success run of length $N_s$ in a sequence of $N_s + N_p$ independent Bernouilli trials with success probability $q_n$ for each bit, and can be determined from recurrent event theory [7].

For any value of $h$, an upper bound on the probability of obtaining frame sync in one or more positions after $N_p$ positions have been tested is given by

$$P_{FA\text{SYNC},n} \leq 1 - (1 - P_{FA2,n})^{N_p} \simeq N_p P_{FA2,n}, \tag{15}$$

where $P_{FA2,n}$ is given by (9).

For the "no DCD" sync method, it is assumed that the bit synchronizer has no effect and the probability of false alarm in a particular position when the signal is absent is given by $P_{FA2,n}$.

## V. Upper Bound on False Alarms

In this section, upper bounds on $P_{F\mathrm{BIT},n}$ and $P_{FA\mathrm{SYNC},n}$ are determined in terms of the maximum acceptable probability $P_L$ of missing a message or packet where $P_L > 0$ is caused by a false sync event immediately prior to the beginning of a legitimate message. This probability $P_L$ may be chosen to be approximately equal to the expected probability $1 - P_D$ of missing a message due to bit errors or erasures.

For the "DCD first" sync method, the choice of the upper bound on $P_{F\mathrm{BIT},n}$ will depend on the detailed characteristics of the bit synchronizer. For purposes of illustration, a two-state PLL bit synchronizer is assumed with a wide bandwidth for rapid acquisition, and a narrow bandwidth for tracking when bit sync is found and DCD is raised. Once DCD is raised, it is assumed that the PLL remains in the tracking state for at least $N_p + N_s$ bits before resetting to the acquisition state. This last assumption is to ensure that the bit synchronizer will not lose lock during a noise burst.

An upper bound is imposed on $P_{F\mathrm{BIT},n}$ for the "DCD first" sync method, because after a false bit sync in noise, DCD is raised, the bit synchronizer PLL is locked in tracking mode, and the frame sync correlator is kept busy searching for frame sync for a time interval $(N_p + N_s)$ bits. Since the bit synchronizer does not adjust rapidly to a new bit phase when in tracking mode, a legitimate message which arrives during this time interval will not be received [8], [9], unless the bit timing of the message is approximately the same as the phase of the falsely locked bit synchronizer. Similarly, an upper bound is imposed on $P_{FA\mathrm{SYNC},n}$ because after false frame sync the receiver is kept busy receiving a false message and legitimate messages which arrive during this time will be lost. We make the conservative assumption that the PLL remains in the tracking state for the expected message duration after a false frame sync event.

For the "DCD first" sync method, by modeling the arrival of false sync events in noise as a Poisson process [9] with normalized traffic load $a$, the probability $P_{\mathrm{miss}}$ that a legitimate message will be missed is given by

$$\begin{aligned} P_{\mathrm{miss}} &= b + (1-b)(1-P_{\mathrm{BIT}}) + (1-b)P_{\mathrm{BIT}}(1-P_{\mathrm{SYNC}}) \\ &= (1 - P_{\mathrm{BIT}}P_{\mathrm{SYNC}}) + bP_{\mathrm{BIT}}P_{\mathrm{SYNC}} \\ &= (1-P_D) + P_L \\ &= 1 - P_{\mathrm{success}} \end{aligned} \tag{16}$$

in the absence of other messages. Thus, $P_{\mathrm{success}} = P_D - P_L \leq 1 - P_L$ and thus $P_{\mathrm{success}} < 1$ even if $P_D = 1$. In (16),

$$b = a/(1+a) \tag{17}$$

is the blocking probability for an $M/D/1/1$ queue with offered traffic load

$$\begin{aligned} a = P_{F\mathrm{BIT},n}[&(1 - P_{FA\mathrm{SYNC},n})(N_p + N_s) \\ &+ P_{FA\mathrm{SYNC},n}(N_p + N_s + M_L)] \end{aligned} \tag{18}$$

where $M_L$ is the message length in bits.

The three terms in the first line of (16) which contribute to $P_{\mathrm{miss}}$ may be interpreted from [9] as follows. The first term is the probability that DCD is raised by a false bit sync event, thus blocking the receiver. The second term is the probability that the receiver does not achieve bit sync during the preamble. The third term is the probability that the frame synchronizer fails to recognize the marker after testing $N_p$ positions. These events are mutually exclusive.

The first term in (16) is a conservative estimate because a legitimate message may be received even when DCD is raised, if the phase of the falsely locked bit synchronizer is acceptably close to the phase of the incoming message. Alternately, the bit synchronizer may be able to detect the phase error and correct the phase within the $N_p$-bit preamble time. A more precise determination of (16) which takes into account the details of the bit synchronizer design is beyond the scope of this paper.

For $P_{\mathrm{BIT}} \cong 1$, $P_{\mathrm{SYNC}} \cong 1$, $P_{FA\mathrm{SYNC},n} \ll 1$ and $a \ll 1$, we can write

$$\begin{aligned} P_L &\cong a \\ &= P_{F\mathrm{BIT},n}[(N_p + N_s) + P_{FA\mathrm{SYNC},n}(N_p + N_s + M_L)]. \end{aligned} \tag{19}$$

For the "DCD first" sync method, $P_{F\mathrm{BIT},n}$ may be selected so that $P_L$ is the highest error rate that is acceptable when there are no errors caused by noise ($P_D = 1$), and $P_{FA\mathrm{SYNC},n}$ is chosen so that the second term in $a$ does not dominate the value of $P_L$ for the message length of interest. For example, if $N_p + N_s = 80$, $M_L = 2000$, and the desired $P_{\mathrm{success}}$ in the absence of errors is 0.9999, ($P_L = 10^{-4}$) then using (19) we set $P_{F\mathrm{BIT},n} = 10^{-6}$ and $P_{FA\mathrm{SYNC},n} = 10^{-2}$. From (15), $P_{FA2,n} = 2.5 \times 10^{-4}$.

For the "no DCD" sync method, we assume that the bit synchronizer has no effect on the probability of false frame sync in noise. For this case, (19) is replaced by

$$P_L = P_{FA2,n}(N_s + M_L). \tag{20}$$

To illustrate, if $N_s = 40$ and $h = 5$, $P_{FA2,n} = b(0.5, 40, 5) = 6.91 \times 10^{-7}$, so that for $M_L = 2000$, (16) yields $P_L = 1.38 \times 10^{-3}$. Thus, a maximum $P_{\mathrm{success}}$ up to 0.9986 may be achieved if there are no bit errors and $h = 5$. For $M_L = 120$, $P_L = 10^{-4}$. A higher error tolerance $h > 5$ b will result in a higher $P_L$ and thus a lower maximum $P_{\mathrm{success}}$ in the absence of bit errors.

## VI. Numerical Results

For System 1, it is desired to maximize $P_{\mathrm{SYNC}}$ by choice of $e$ and $h$, with a specified upper bound on $P_{FA\mathrm{SYNC},n}$ (or equivalently on $P_{FA2,n}$). For each value of $h$, $e$ is chosen to be as large as possible without violating the bound on $P_{FA2,n}$. $p, s, p_n$, and $s_n$ are determined by $e$ and $E_b/N_o$ according to (10) and (11).

For System 2, $P_{\mathrm{SYNC}}$ is maximized by choice of $h$ only, with specified bounds on $P_{FA2,n}$ since $e = 0$, $s = s_n$ is fixed by the disturbance independent of $p$.

Numerical results based on calculation of (8), (12), and (13) indicate that $P_{\mathrm{SYNC}}$ may be improved by using errors-and-erasures decoding and an error tolerance $h$ greater than if errors-only decoding were used. To illustrate the improvement available, results are presented for the range of parameters listed in Table I. The only difference between the "no DCD" and the "DCD first" sync method is that the upper bound on $P_{FA2,n}$ may be higher in the latter case.

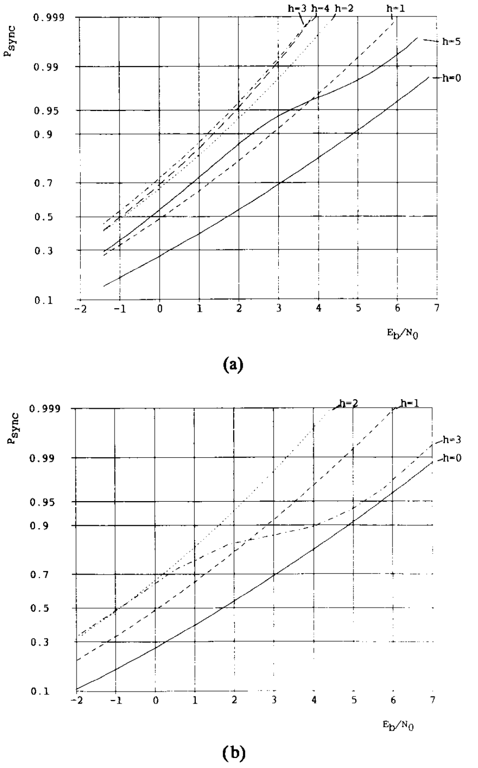
To obtain $P_D = P_{\mathrm{BIT}} \cdot P_{\mathrm{SYNC}}$, it is necessary to determine the bit synchronizer characteristic $P_{\mathrm{BIT}}$ versus $E_b/N_o$. Then $P_{\mathrm{success}} = P_D - P_L$.

In all numerical results, the values of $P_{\mathrm{SYNC}}$ are the lower bound according to (12). If $h$ is not too large, then $P_{FA\mathrm{SYNC},d} \ll 1$, and $P_{\mathrm{SYNC}} = P_{FS}$.

Fig. 2(a) shows $P_{\mathrm{SYNC}}$ versus $E_b/N_o$ for the 16 b marker $B433_{hex}$ with $P_{FA2,n} = b(0.5, 16, 0)$. For this case, if we use

TABLE I
SUMMARY OF NUMERICAL RESULTS

| Figure | Marker Length | Sync Method | $P_{FA2,n}$ Upper Bound | System |
|---|---|---|---|---|
| 2 | 16 | "no DCD" | $1.526 \times 10^{-5}$ | 1 |
| 3 | 40 | "no DCD" | $6.91 \times 10^{-7}$ | 1 |
| 4 | 40 | "DCD 1st" | $2.5 \times 10^{-4}$ | 1 |
| 5 | 40 | "no DCD" | $6.91 \times 10^{-7}$ | 2 |
| 6 | 40 | "DCD 1st" | $2.5 \times 10^{-4}$ | 2 |
| 7 | 16 | "DCD 1st" | $2.6 \times 10^{-4}$ | 2 |



(a)

(b)

Fig. 2. (a) $P_{\text{SYNC}}$ versus $E_b/N_o$ 16 b marker, $B433_{hex}$, System 1, $P_{FA2,n} \leq 1.525 \times 10^{-5}$. (b) $P_{\text{SYNC}}$ versus $E_b/N_o$ 16 b marker, $7E7E_{hex}$, System 1, $P_{FA2,n} \leq 1.525 \times 10^{-5}$.

the "no DCD" method and assume $M_L = 64$, then (20) yields $P_L = 0.0012$, so that $P_{\text{success}} < 0.9988$. The best results for $P_{\text{SYNC}}$ are obtained when $h = 3$ (with $e = 0.96942$), but the results for $h = 2$ and $h = 4$ are almost as good. If $h = 5$, then $P_{FA\text{SYNC},d}$ in (12) is not negligible and thus $P_{\text{SYNC}} < P_{FS}$. Compared to the results for $h = 0$, allowing an error and erasure tolerance results in a gain of about 3 dB at $P_{\text{SYNC}} = 0.5$, rising to 4.5 dB at $P_{\text{SYNC}} = 0.99$, without increasing $P_{FA\text{SYNC},n}$. Table II shows numerical results for $P_{FA\text{SYNC},d}$ and $P_{\text{SYNC}}$ for $E_b/N_o = -0.85$ dB such that $p = 0.1$ if $e = 0$.

Fig. 2(b) shows $P_{\text{SYNC}}$ versus $E_b/N_o$ for the 16 bit HDLC "flag" marker $7E7E_{hex}$. For this marker, $P_{FA\text{SYNC},d}$ is not negligible for $h = 3$, and thus the best results are obtained for $h = 2$.

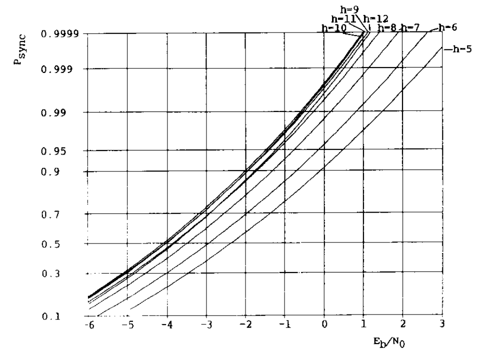


Fig. 3. $P_{\text{SYNC}}$ versus $E_b/N_o$ 40 b marker, System 1, $P_{FA2,n} \leq 6.91 \times 10^{-7}$.

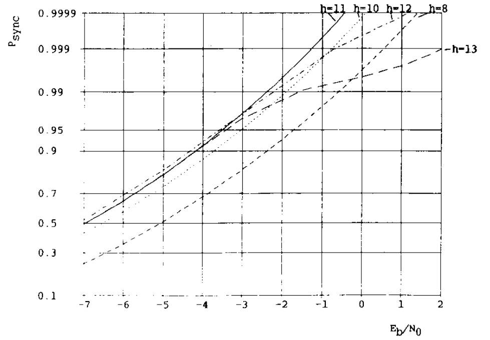


Fig. 4. $P_{\text{SYNC}}$ versus $E_b/N_o$ 40 b marker, System 1, $P_{FA2,n} \leq 2.5 \times 10^{-4}$.

Fig. 3 shows $P_{\text{SYNC}}$ versus $E_b/N_o$ for a 40 b marker with $h = 5$ and $P_{FA2,n} = b(0.5, 40, 5)$ for the "no DCD" sync method. The best results are obtained for $h = 10$, but the results for $h = 9$, 11, 12 are almost equivalent. Compared to the results for $h = 5$ and $e = 0$, the improvement represents a gain of approximately 2 dB over the range of $E_b/N_o$. Table III shows numerical results for $P_{\text{SYNC}}$ and $P_{FA\text{SYNC},d}$ at $E_b/N_o = -0.85$ dB.

Fig. 4 shows $P_{\text{SYNC}}$ for upper bound $P_{FA\text{SYNC},n}$, $< 10^{-2}$ using the "DCD first" sync method. (Here, $P_L = 10^{-4}$ if $M_L = 2000$ and $P_{F\text{BIT},n} = 10^{-6}$). For this case, if $e = 0$, then $h = 8$ yields $P_{FA2,n}$ below the upper bound, whereas $h = 9$ yields $P_{FA2,n}$ above the bound. By introducing an erasure zone $e$, $P_{FA2,n}$ can be selected to be exactly equal to the bound. The highest value of $P_{\text{SYNC}}$ is obtained with $h = 11$ and $e = 0.45025$. It may be seen from Table IV that $P_{FA\text{SYNC},d}$ is not negligible for $h = 12$ or $h = 13$ in this case.

Similar results are expected for other receiver designs where the expressions (10), (11) for $p, s, p_n$, and $s_n$ may be different.

For System 2 and the "no DCD" sync method, Fig. 5 shows $P_{\text{SYNC}}$ versus $E_b/N_o$ for a 40 b marker with $s = 0.04, 0.125$, and 0.25, and upper bound $P_{FA2,n} < b(0.5, 40, 5) = 6.91 \times 10^{-7}$. If $s = 0.25$ and erasure information is used, then $h$ can be raised from 5 to 7 without violating the upper bound on $P_{FA2,n}$, resulting in a significant improvement in $P_{\text{SYNC}}$. Similarly, if $s = 0.125$, then $h$ can be raised from 5 to 6. For smaller values

TABLE II

$P_{\text{SYNC}}$ VERSUS $e$, "NO DCD" SYNC METHOD 16 b MARKER, $P_{FA2,n} = b(0.5, 16, 0) = 1.525 \times 10^{-5}$ $E_b/N_o = -0.85$ dB

| $h$ | $e$ | $p$ | $s$ | $p_n$ | $s_n$ | $P_{FS}$ | $P_{FASYNC,d}$ | $P_{\text{SYNC}}$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0.0000 | 0.1000 | 0.0000 | 0.5000 | 0.0000 | 0.1853 | $1.15 \times 10^{-7}$ | 0.1853 |
| 1 | 0.2982 | 0.0570 | 0.1058 | 0.3826 | 0.2348 | 0.3510 | $2.20 \times 10^{-7}$ | 0.3510 |
| 2 | 0.6335 | 0.0277 | 0.2311 | 0.2629 | 0.4742 | 0.5104 | $1.08 \times 10^{-6}$ | 0.5104 |
| 3 | 0.9694 | 0.0122 | 0.3656 | 0.1660 | 0.6680 | 0.5625 | $2.13 \times 10^{-5}$ | 0.5625 |
| 4 | 1.330 | 0.0045 | 0.5149 | 0.0917 | 0.8166 | 0.5229 | $9.51 \times 10^{-4}$ | 0.5220 |
| 5 | 1.752 | 0.0012 | 0.6797 | 0.0399 | 0.9202 | 0.4010 | $1.89 \times 10^{-2}$ | 0.3821 |

TABLE III

$P_{\text{SYNC}}$ VERSUS $e$, "NO DCD" SYNC METHOD 40 b MARKER, $P_{FA2,n} = b(0.5, 40, 5) = 6.91 \times 10^{-7}$ $E_b/N_o = -0.85$ dB

| $h$ | $e$ | $p$ | $s$ | $p_n$ | $s_n$ | $P_{FS}$ | $P_{FASYNC,d}$ | $P_{\text{SYNC}}$ |
|---|---|---|---|---|---|---|---|---|
| 5 | 0.0000 | 0.1000 | 0.0000 | 0.5000 | 0.0000 | 0.7936 | $1.71 \times 10^{-9}$ | 0.7936 |
| 6 | 0.1424 | 0.0771 | 0.0549 | 0.4429 | 0.1141 | 0.8823 | $2.52 \times 10^{-9}$ | 0.8823 |
| 7 | 0.3119 | 0.0554 | 0.1109 | 0.3773 | 0.2455 | 0.9436 | $5.84 \times 10^{-9}$ | 0.9436 |
| 8 | 0.4765 | 0.0394 | 0.1711 | 0.3168 | 0.3168 | 0.9697 | $2.40 \times 10^{-8}$ | 0.9697 |
| 9 | 0.6394 | 0.0274 | 0.2331 | 0.2613 | 0.4775 | 0.9799 | $1.66 \times 10^{-7}$ | 0.9799 |
| 10 | 0.8033 | 0.0186 | 0.2938 | 0.2108 | 0.5783 | 0.9828 | $5.22 \times 10^{-7}$ | 0.9828 |
| 11 | 0.9712 | 0.0121 | 0.3661 | 0.1657 | 0.6687 | 0.9811 | $2.34 \times 10^{-5}$ | 0.9811 |
| 12 | 1.1465 | 0.0076 | 0.4387 | 0.1258 | 0.7484 | 0.9738 | $2.77 \times 10^{-4}$ | 0.9735 |

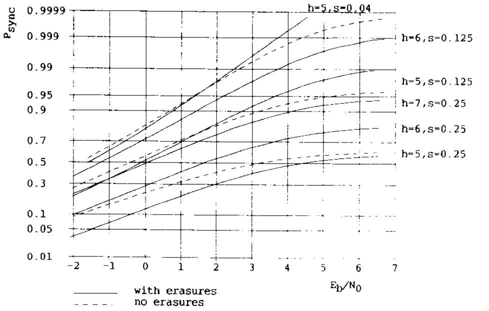


Fig. 5. $P_{\text{SYNC}}$ versus $E_b/N_o$ 40 b marker, System 2, $P_{FA2,n} \leq 6.91 \times 10^{-7}$.

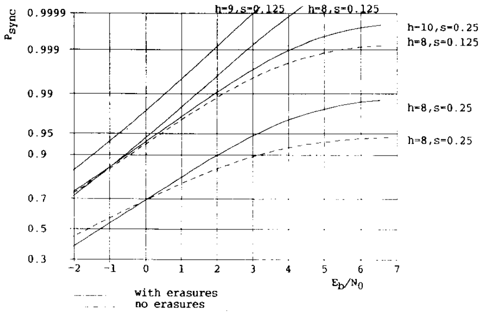


Fig. 6. $P_{\text{SYNC}}$ versus $E_b/N_o$ 40 b marker, System 2, $P_{FA2,n} \leq 2.5 \times 10^{-4}$.

of $s$, $h$ must remain at 5 to avoid exceeding the upper bound on $P_{FA2,n}$. For $h = 0.04$ and 0.125, $P_{\text{SYNC}}$ is improved with erasure decoding, provided that $E_b/N_o > 1.8$ dB.

For System 2 and the "DCD first" sync method, Fig. 6 shows $P_{\text{SYNC}}$ versus $E_b/N_o$ for a 40 b marker with $s = 0.125$ and 0.25, and upper bound $P_{FASYNC,n} \leq 10^{-2}$. $h$ may be set to 8 for this case if erasures are not considered. If $s = 0.25$, then $h$ can be raised to 10 without violating the upper bound, and $P_{\text{SYNC}}$ is improved significantly for all values of $E_b/N_o$. If $h$ is left at 8, then using erasure information yields an improvement in $P_{\text{SYNC}}$, provided that $E_b/N_o > 1$ dB. Table V shows numerical results for $P_{\text{SYNC}}$ and $P_{FASYNC,d}$ for selected values of $p$ and $s$. Similar results apply for $s = 0.125$.

For the 16 b marker $B433_{hex}$ with System 2 and the "DCD 1st" sync method, Fig. 7 shows $P_{\text{SYNC}}$ versus $E_b/N_o$ for selected values of $s$ and upper bound $P_{FASYNC,n} < 4.1 \times 10^{-3}$. For $s = 0.246$, $h$ may be increased from 1 to 2 without violating the upper bound, and $P_{\text{SYNC}}$ is improved for all values of $E_b/N_o$. For $s < 0.246$, $h$ cannot be increased without violating the upper bound. If $s < 0.081$, then erasure decoding yields an improvement in $P_{\text{SYNC}}$ for sufficiently high values of $E_b/N_o$.

## VII. DISCUSSION AND CONCLUSION

The probability of successful frame synchronization in packet transmission may be improved by using errors and erasures decoding rather than errors-only decoding, without changing the upper bound on the probability of false alarms. Twice as many erasures as errors are tolerated. An improvement of several dB is obtained on AWGN channels if an erasure zone is added to the receiver decision device. The size of the erasure zone and the error tolerance is chosen to maximize the probability of successful frame sync, subject to the upper bound on false alarms. The improvement is also significant on channels where erasures are caused by interference with a fixed probability independent of the signal-to-noise ratio. For both types of channels, the probability of false alarm when data is present (i.e., incorrect frame alignment) increases with $h$, but is found to be negligible unless $h$ is set too high.

The upper bound on false alarms in noise is determined by the maximum acceptable probability of missing a message due to a false sync event. This probability is calculated by modeling the arrival of false sync events as a Poisson process. The maximum

TABLE IV
$P_{\mathrm{SYNC}}$ VERSUS $e$, "DCD 1st" SYNC METHOD 40 b MARKER, $P_{FA2,n} = 2.5 \times 10^{-4}$ $E_b/N_o = -0.85$ dB

| $h$ | $e$ | $p$ | $s$ | $p_n$ | $s_n$ | $P_{FS}$ | $P_{FASYNC,d}$ | $P_{\mathrm{SYNC}}$ | $P_{FA2,n}$ |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 0.0000 | 0.1000 | 0.0000 | 0.5000 | 0.0000 | 0.9845 | $6.33 \times 10^{-6}$ | 0.9845 | $9.11 \times 10^{-5}$ |
| 9 | 0.0000 | 0.1000 | 0.0000 | 0.5000 | 0.0000 | 0.9949 | $6.48 \times 10^{-5}$ | 0.9849 | $3.40 \times 10^{-4}$ |
| 9 | 0.0225 | 0.0962 | 0.0076 | 0.4913 | 0.0174 | 0.9942 | $4.54 \times 10^{-5}$ | 0.9942 | $2.5 \times 10^{-4}$ |
| 10 | 0.2343 | 0.0647 | 0.0828 | 0.4073 | 0.1854 | 0.9987 | $6.43 \times 10^{-5}$ | 0.9987 | $2.5 \times 10^{-4}$ |
| 11 | 0.4502 | 0.0416 | 0.1616 | 0.3260 | 0.3481 | 0.9996 | $1.96 \times 10^{-4}$ | 0.9994 | $2.5 \times 10^{-4}$ |
| 12 | 0.6603 | 0.0259 | 0.2420 | 0.2538 | 0.4924 | 0.9998 | $1.02 \times 10^{-3}$ | 0.9988 | $2.5 \times 10^{-4}$ |
| 13 | .8761 | 0.0155 | 0.3273 | 0.1904 | 0.6193 | 0.9998 | $6.76 \times 10^{-3}$ | 0.9931 | $2.5 \times 10^{-4}$ |

TABLE V
$P_{\mathrm{SYNC}}$ WITH FIXED $s$, "DCD 1st" SYNC METHOD SYSTEM 2 40 b MARKER, $P_{FASYNC,n} < 10^{-2}$

| $p$ | $s$ | $p_n$ | $s_n$ | $h$ | $P_{FS}$ | $P_{FA2,n}$ | $P_{FA2,n}$ |
|---|---|---|---|---|---|---|---|
| 0.000 | 0.250 | 0.375 | 0.250 | 10 | 0.9998 | $1.41 \times 10^{-4}$ | $7.66 \times 10^{-9}$ |
| 0.125 | 0.000 | 0.500 | 0.000 | 8 | 0.9448 | $9.11 \times 10^{-5}$ | $2.64 \times 10^{-5}$ |
| 0.010 | 0.250 | 0.375 | 0.250 | 10 | 0.9989 | $1.41 \times 10^{-4}$ | $2.98 \times 10^{-7}$ |
| 0.135 | 0.000 | 0.500 | 0.000 | 8 | 0.9180 | $9.11 \times 10^{-5}$ | $4.18 \times 10^{-5}$ |
| 0.100 | 0.250 | 0.375 | 0.250 | 10 | 0.7290 | $1.41 \times 10^{-4}$ | $3.54 \times 10^{-4}$ |
| 0.225 | 0.000 | 0.375 | 0.250 | 8 | 0.4385 | $9.11 \times 10^{-5}$ | $5.65 \times 10^{-4}$ |

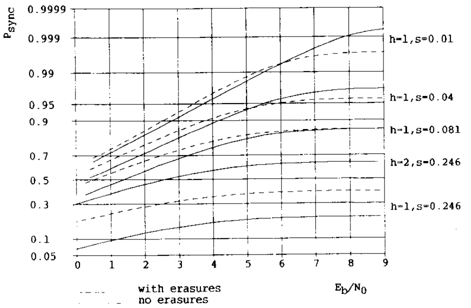


Fig. 7. $P_{\mathrm{SYNC}}$ versus $E_b/N_o$ 16 b marker, System 2, $P_{FA2,n} \leq 2.6 \times 10^{-4}$.

error and erasure tolerances and the size of the erasure zone (if applicable) are then chosen so that this probability is no greater than the expected probability of missing a message due to bit errors.

The upper bound on false alarms in noise may be higher if successful bit sync is required before the search for frame sync begins, but for this case an upper bound must also be imposed on the probability of false bit sync.

The numerical results presented here provide some indication of the improvements available by using errors-and-erasures decoding for frame sync. The system designer can use this information to trade off the additional cost with the performance improvement in the context of his particular system.

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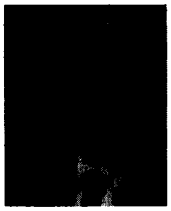
## REFERENCES

[1] R.A. Scholtz, "Frame synchronization techniques," *IEEE Trans. Commun.*, vol. COM-28, pp. 1204–1212, Aug. 1980.
[2] C.K. Rushforth and R.J. Currie, "Frame Synchronization in the presence of errors and erasures," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-19, pp. 498–505, 1983.
[3] ARINC Corporation, *Advanced Train Control Systems Specification 200: Communications Systems Architecture, Second Edition*, Annapolis, MD: Oct. 1988, pp. L1–L6.
[4] CCIR Study Group 8, "Mobile services," Rep. 903, Part E, 1986.
[5] J.K. Holmes, *Coherent Spread Spectrums Systems*. New York: Wiley, 1982, pp. 609–616.
[6] P.F. Driessen, "Binary frame synchronization sequences for packet radio," *Electron. Lett.*, vol. 23, no. 22, pp. 1190–1191, Oct. 1987.
[7] J.J. Hunter, Mathematical Techniques of Applied Probability. New York: Academic, 1983, vol. 1, p. 115.
[8] S.S. Rappaport and D.M. Grieco, "Spread-Spectrum signal acquisition: Methods and technology," *IEEE Commun. Mag.*, vol. 22, p. 6–21, 1984.
[9] S.S. Rappaport and D.L. Schilling, "A two-level coarse code acquisition scheme for spread spectrum radio," *IEEE Trans. Commun.*, vol. COM-28, pp. 1734–1742, Sept. 1980.
[10] M.N. Al-Subbagh and E.V. Jones, "Optimum patterns for frame alignment," *IEE Proc.*, vol. 135, Pt. F, pp. 594–603, 1988.
[11] P.F. Driessen, "Performance of frame synchronization in automatic train control communications systems," in *Proc. 39th IEEE Vehic. Technol. Conf.*, pp. 517–522, 1989, pp. 517–522.
[12] G.C. Clark and J.B. Cain, *Error-Correction coding for digital communications*. New York: Plenum, 1981.
[13] M. Schwartz, *Telecommunication Networks*. New York: Addison-Wesley, 1987.



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