

Zero-Crossing DPLL Bit Synchronizer with Pattern Jitter Compensation

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Abstract—A new digital phase-locked loop (DPLL) bit synchronizer which tracks the zero crossings of a bandlimited binary signal is proposed. This synchronizer reduces “pattern jitter” or “self noise” with a compensation signal in the synchronizer feedback loop without using a prefilter. Analytical results are derived for the timing jitter variance (additive noise and self noise) of the synchronizer. Computer simulations and laboratory measurements verify the effectiveness of the pattern jitter compensation technique for a synchronizer operating with both spectral raised cosine signaling pulses as well as for signaling pulses generated by a realizable filter network.

The pattern jitter compensation method can be implemented in an adaptive synchronizer structure for applications where *a priori* knowledge of the signaling pulse shape is not available.

I. INTRODUCTION

In the synchronization of band limited signals pattern jitter or self noise [1], [2] may be of concern. Signaling pulses overlapping in time will cause the synchronizer to generate a timing jitter component that is statistically independent of the timing jitter generated by the additive noise. At high signal to noise ratios, the jitter performance is bounded by the pattern jitter [1]. The synchronizer pattern jitter performance is of special concern in a regenerative synchronizer environment, where the timing signal is successively recovered along a chain of digital regenerators [3]. The maximum number of regenerators in the chain that can be used in a system is determined by the maximum allowable cumulative pattern jitter before the error probability is not acceptable [4].

A common synchronization technique for bandlimited systems is to pass the received signal through a nonlinear device to generate a discrete spectral line component at $1/T$, which is recovered by either a bandpass filter or a PLL [5], [6], [1]. This synchronizer will have a pattern jitter component present in the recovered timing signal. The pattern jitter can be reduced by reducing the bandwidth of the bandpass filter (or PLL) [7], at the expense of acquisition time [8].

It has been shown that for a synchronizer operating with a square law nonlinearity, the use of a bandpass prefilter with conjugate symmetry about $1/2T$ prior to the nonlinear device will eliminate pattern jitter [2]. For other nonlinearities a nearly optimum prefilter has been defined [9].

In this paper, a new approach to pattern jitter reduction which does not require a prefilter is presented. A zero crossing tracking digital phase locked loop is used in conjunction with a compensation signal that estimates the distortion of the zero-crossing locations caused by pulse overlap using knowledge of

the received data decisions and the channel impulse response $x(t)$. The digital phase-locked loop has several advantages. First, the interface between the received signal and the synchronizer is a simple hard limiter, eliminating the need for an analog to digital converter. Second, the system is suitable for low-cost digital circuit implementation in that only the hard limited (thus binary) signal is processed. Third, it will be shown that pattern jitter can be effectively eliminated for most practical signal to noise ratios (SNR) without the requirement of a prefilter. The cost saved by not using a prefilter may be significant in some applications.

The performance of the new synchronizer is determined in terms of the additive noise and self noise timing error (jitter) variances with the pattern jitter compensation technique incorporated into the analysis. For applications where little is known about the system impulse response, an adaptive pattern jitter compensation technique is also presented. Computer simulation results are presented for synchronization of both spectral raised cosine (SRC) signaling pulses [10] and for pulses that can be generated by a realizable filter network [11]. The computer simulations verify that pattern jitter may be significantly reduced with this synchronization technique in systems that operate fairly close to the Nyquist minimum bandwidth. Laboratory measurements of a digital signal processor implementation of a pattern jitter compensation synchronizer confirm the effectiveness of the technique.

This paper is organized as follows: the proposed pattern jitter compensation method and synchronizer operation is described in Section II. Section III contains the major analytical result of the paper, the timing jitter variance analysis of the proposed DPLL synchronizer for both additive noise and pattern jitter in terms of the DPLL feedback transfer function, the signaling pulse $x(t)$ and the signal to noise ratio (SNR). An adaptive scheme which does not require *a priori* knowledge of $x(t)$ is outlined in Section IV. The computer simulation results are presented in Section V with conclusions in Section VI.

II. PATTERN JITTER COMPENSATION AND SYNCHRONIZER OPERATION

A. Principles of Pattern Jitter Compensation

Consider a binary transmission system in the absence of noise. The received signal is

$$s(t) = \sum_k a_k x(t - kT) \quad (1)$$

where $a_k \in \{-1, +1\}$ are independent zero-mean binary numbers and $x(t)$ is the Nyquist filtered signaling pulse.

The Nyquist criterion for zero ISI guarantees that the signaling pulse overlap from adjacent symbols is zero at the decision times $t = kT$. However, at the zero crossing times, pulse overlap is most often not zero, and the zero crossing scatter can be quite significant. For zero pulse overlap (no scatter) at zero crossings,

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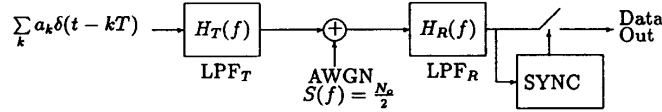


Fig. 1. Bandlimited baseband binary data transmission system.

$x(t)$ must be chosen to ensure an excess bandwidth extending to at least $1/T$ [10]. As the bandwidth of the system is reduced below $1/T$, pulse overlap will distort the location of the zero crossings. As the bandwidth is decreased, the peak to peak amplitude of the zero-crossing distortion will increase, as the precursor and postcursor tails of $x(t)$ will have a slower rate of decay [12]. A synchronizer that tracks the zero crossings will therefore have a significant pattern jitter component in the recovered timing signal.

If a_k and a_{k+1} are of opposite polarity, a zero crossing will occur at

$$t = kT + t_o + \tau_k \quad (2)$$

where t_o is the nominal zero-crossing location and the pattern jitter τ_k is a zero-mean random variable generated by the pulse overlap. If the entire sequence $\{a_k\}$ is known *a priori* a synchronizer can calculate τ_k exactly and subtract it out.

If the tails of $x(t)$ decay quickly, a synchronizer can use a finite number of estimated data values to estimate τ_k . The sequence of estimated data values

$$\{\hat{a}_k\} = \{\hat{a}_{k-l}, \dots, \hat{a}_k, \hat{a}_{k+1}, \dots, \hat{a}_{k+m+1}\}, \quad \hat{a}_k \in \{-1, +1\} \quad (3)$$

can be used to determine $\hat{\tau}_k$, the estimate of τ_k , by solving

$$\sum_{i=-l}^{m+1} \hat{a}_{k+i} x(\hat{\tau}_k + t_o - iT) = 0. \quad (4)$$

As m future bits relative to \hat{a}_{k+1} are required in $\{\hat{a}_k\}$, an m bit delay is required to calculate $\hat{\tau}_k$. The m bits will correspond to the expected length of the precursor, which for most applications will not be significantly longer than one or two bits [11]. In a practical system, the values of $\hat{\tau}_k$ can be determined for all combinations of $\{\hat{a}_k\}$ and stored in memory. During operation, the synchronizer can retrieve the stored values of $\hat{\tau}_k$. It will be shown in Section IV that the $\hat{\tau}_k$ values may also be determined with an adaptive synchronization structure.

B. Synchronizer Description

The proposed synchronizer operates on the binary communications system whose baseband equivalent model is illustrated in Fig. 1 [13]. The system consists of a transmit low pass filter (LPF_T), a receive low pass filter (LPF_R), and a synchronizer to generate the appropriate samples to recover the transmitted data. The $H_T(f)$ and $H_R(f)$ filters form a matched filter pair [13]. It is assumed that the channel frequency characteristic is flat, or that fixed equalization is used to compensate for the channel characteristic.

The received signal and noise at the LPF_R output is

$$y(t) = s(t - \epsilon) + \eta(t) \quad (5)$$

where $s(t)$ is defined by (1), ϵ is the delay of the received signal to be estimated by the synchronizer, and $\eta(t)$ is the filtered additive white Gaussian noise with single-sided power spectral density

(psd) N_o . The signaling pulse $x(t)$ is the impulse response of the matched filter cascade. We assume throughout this paper that there is negligible frequency offset between the local and incoming clocks, and therefore ϵ assumes a constant value.

The synchronizer used to analyze the performance of the proposed compensation technique is illustrated in Fig. 2. The synchronizer is a zero-crossing tracking phase-locked loop synchronizer [14] with the addition of the pattern jitter compensation. The hard limiter reveals the zero crossings in the received signal. The values of \hat{a}_{k+1} are determined by sampling at

$$t = kT + \hat{\epsilon}_k \quad (6)$$

where $\hat{\epsilon}_k$ is the synchronizer's estimate of ϵ for data symbol \hat{a}_{k+1} . The synchronizer timing error e_k is

$$e_k = \epsilon - \hat{\epsilon}_k. \quad (7)$$

The received sequence $\{\hat{a}_{k-m}\}$ is stored in a shift register, the values of which are used to locate in memory the correct value of $\hat{\tau}_{k-m}$. The phase detector (PD) generates an output w_k which is proportional to the time difference between the location of the zero crossing (2), and the predicted location $t = kT + t_o + \hat{\epsilon}_k$. The PD may be implemented digitally with a high-speed up/down counter with clock period $T_c \ll T$. The counter is reset to zero at the start of each bit interval and counts over the duration of the bit interval. The output of the hard limiter determines the direction of the count. The PD output $w_k = (a_k - a_{k+1})r_k$, where r_k is the counter result at the end of the bit interval. The PD quantizes the zero crossings to $N = \lfloor T/T_c \rfloor$ locations.¹ The remainder of the synchronizer consists of the m bit delay, a loop filter $F(z)$, and a numerically controlled oscillator (NCO).

C. Synchronizer Model

In this section, the model of the synchronizer used to determine the timing-error variance is discussed and assumptions are stated.

Following [14], we assume that the zero-crossing locations are sufficiently close to the nominal locations $t = kT + t_o + \epsilon$ to use a two term Taylor series expansion of $y(t)$ about the nominal zero-crossings as a linear approximation. Some comments about this assumption should be made. The assumption will not be valid for very small excess bandwidth systems where the pulse overlap is too large for a linear approximation to apply. The assumption will also fail if the noise $\eta(t)$ is not sufficiently bandlimited and the SNR is too low to assume either a single zero crossing in a bit interval, or zero crossings close to the nominal location. Simulation results in Section V indicate that these assumptions are reasonable for $E_b/N_o > 5$ dB and excess bandwidth $0.1 < \alpha < 1.0$ where α is the excess bandwidth factor relative to the minimum Nyquist bandwidth.

Following these assumptions [14], if $\hat{a}_k \neq \hat{a}_{k+1}$ a zero crossing in the received waveform $y(t)$ occurs at

$$t = kT + t_o + \epsilon + n_k + \tau_k \quad (8)$$

¹The PD implementation description assumes $t_o = T/2$, but the PD may easily be modified if nominal zero crossings do not occur in the center of the bit interval.

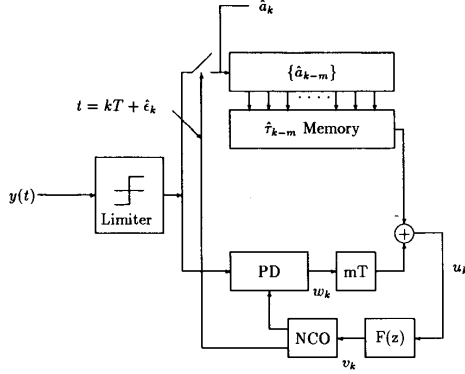


Fig. 2. Synchronizer with pattern jitter compensation.

where ϵ is the constant delay parameter, n_k is due to the additive noise, and τ_k is due to pulse overlap. The terms n_k and τ_k are statistically independent. A typical zero crossing waveform is illustrated in Fig. 3.

The linear approximation for n_k is

$$n_k = c \cdot a_k \eta(kT + t_o + \epsilon) \quad (9)$$

where c is the expected inverse slope of the zero crossing [14]

$$c = \frac{1}{x'(t_o) - x'(t_o - T)}. \quad (10)$$

Similarly, a linear approximation to τ_k can be made by determining the amplitude of the pulse overlap at the nominal zero-crossing location and multiplying by c [14]

$$\tau_k = c \cdot a_k \sum_{i \neq 0,1} a_{k+i} x(t_o - iT). \quad (11)$$

Ignoring the possibility of errors in the received data sequence, the linearized value of $\hat{\tau}_k$ is the summation in (11), including only the terms in the compensation sequence (3)

$$\hat{\tau}_k = c \cdot a_k \sum_{i=-1}^{m+1} a_{k+i} x(t_o - iT). \quad (12)$$

A discrete-time model of the synchronizer is shown in Fig. 4. The structure is very similar to a digital phase-locked loop [15], with the exception of the multiplier and the pattern jitter compensation signal in the feedback. At the input to the synchronizer, τ_k and n_k are the pulse overlap and additive noise disturbance parameters, respectively, and ϵ is the parameter to be estimated.

The value of b_k , the input to the multiplier, is determined by the presence of a transition [14]

$$b_k = \begin{cases} 1 & \text{if } a_k \neq a_{k+1} \\ 0 & \text{if } a_k = a_{k+1} \end{cases} \quad (13)$$

and so the multiplier input $2b_k$ may be written as

$$2b_k = (1 - a_k a_{k+1}). \quad (14)$$

In Fig. 4, the output of the multiplier is scaled by the PD gain constant K_{PD} . The PD output w_k is delayed m bits and the pattern jitter compensation signal $2b_{k-m} \hat{\tau}_{k-m} K_{PD}$ is subtracted from w_{k-m} . The resulting sequence u_k is filtered by $F(z)$, and the

filtered output sequence v_k is used to control the NCO. Timing adjustment are made according to

$$\hat{\epsilon}_{k+1} = \hat{\epsilon}_k + K_{NCO} v_k.$$

The discrete-time synchronizer model of Fig. 4 may be redrawn as shown in Fig. 5, where the transfer function $G(z)$ is

$$G(z) = \frac{K_{PD} K_{NCO} F(z) z^{-(m+1)}}{1 - z^{-1}}. \quad (15)$$

Referring to Fig. 4, the pattern jitter compensation signal $2b_{k-m} \hat{\tau}_{k-m} K_{PD}$ may be transferred backwards through the m bit delay, the phase detector gain constant K_{PD} , and the transition multiplier b_k , and therefore may be represented at the input by $\tilde{\tau}_k$ as shown in Fig. 5.

III. DETERMINATION OF TIMING-ERROR VARIANCE

In this section, an expression for the synchronizer timing-error variance (jitter variance) σ_e^2 is derived in terms of $x(t)$, $G(z)$, E_b/N_o and the number of data decisions $l + m + 2$ used to estimate $\hat{\tau}_k$ in (4). The two components of σ_e^2 of interest are the pattern jitter variance $\sigma_{p_j}^2$ and the noise jitter variance $\sigma_{n_j}^2$.

Due to the presence of the multiplier in the feedback path, a transfer function for the PLL cannot be directly derived. The performance of an analog synchronizer, based on the linear Taylor series approximation has been analyzed in [14]. This analysis is adapted here for the discrete-time model [16, Appendix B] with the pattern jitter compensation technique incorporated into the analysis.

The result for the timing-error variance in [14] is accurate only for narrow bandwidth synchronizers. In the present analysis, a new result for σ_e^2 is derived. It is shown that if the sampled noise sequence $\eta(kT + t_o + \epsilon)$ is a discrete-time white noise process (which for example is the case for any Nyquist matched filter system [16, Appendix C]), then the result for $\sigma_{n_j}^2$ is correct regardless of the synchronizer bandwidth. The result for $\sigma_{p_j}^2$ contains some approximations, but computer simulation results indicate that these approximations introduce only small errors, and for large bandwidth synchronizers the analysis is significantly more accurate than in [14].

The following procedure is used to determine σ_e^2 : first the autocorrelation function of the zero-mean component of the sequence $\{\hat{\epsilon}_k\}$ is evaluated. After manipulation and substitution, two approximations are made to simplify two of the less dominant cross-correlation expressions in the resulting equation. The z transform of the simplified equation is taken, from which σ_e^2 is found to be (31).

It is shown in [14] that if $G(z)$ has a pole at $z = 1$ (or $\omega = 0$) for $\epsilon = \text{constant}$, $\hat{\epsilon}_k$ is an unbiased estimate of ϵ , i.e., $E[\hat{\epsilon}_k] = \epsilon$. Therefore $\hat{\epsilon}_k = \epsilon + \tilde{\epsilon}_k$ where $\tilde{\epsilon}_k$ is the zero-mean random variable with mean-square value $R_{\tilde{\epsilon}}(0) = \sigma_e^2 = \sigma_{p_j}^2 + \sigma_{n_j}^2$.

The sequence $\tilde{\epsilon}_k$ may be written

$$\tilde{\epsilon}_k = \sum_{j=-\infty}^k g_{k-j} \{\gamma_j - 2b_j \tilde{\epsilon}_j\} \quad (16)$$

where g_j is the impulse response of $G(z)$ and

$$\gamma_k = 2b_k(\tau - \hat{\tau}_k) + 2b_k n_k. \quad (17)$$

The calculation of σ_e^2 begins by rearranging (16) to yield

$$\tilde{\epsilon}_k + 2 \sum_{j=-\infty}^k g_{k-j} b_j \tilde{\epsilon}_j = \sum_{j=-\infty}^k g_{k-j} \gamma_j. \quad (18)$$

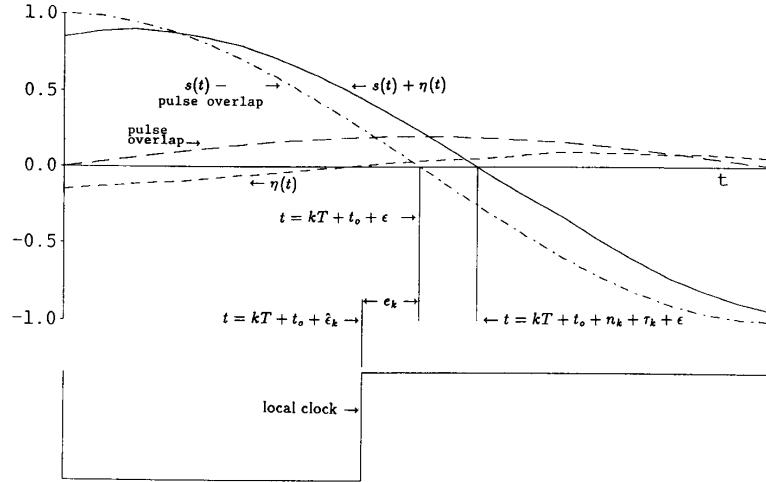


Fig. 3. Zero-crossing distortion generated by additive noise and pulse overlap.

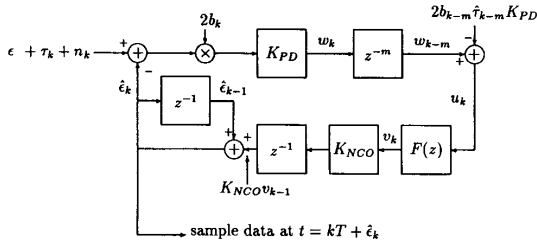


Fig. 4. Discrete-time synchronizer model.

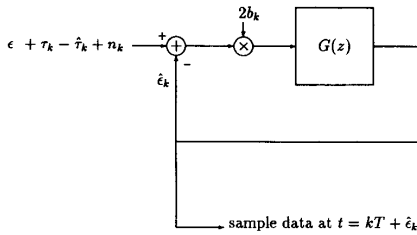


Fig. 5. Discrete-time synchronizer represented as a single transfer function feedback system.

The autocorrelation of (18) is

$$E \left\{ \left[\tilde{\epsilon}_k + 2 \sum_{i=-\infty}^k g_{k-i} b_i \tilde{\epsilon}_i \right] \left[\tilde{\epsilon}_{k+q} + 2 \sum_{j=-\infty}^{k+q} g_{k-j+q} b_j \tilde{\epsilon}_j \right] \right\} \\ = \sum_{i=-\infty}^k \sum_{j=-\infty}^{k+q} g_{k-i} g_{k+q-j} R_\gamma(i-j) \quad (19)$$

where $R_\gamma(q)$ is the autocorrelation function of γ_k .

In [16], it is demonstrated that after substitution of (16), the expectation in (19) may be evaluated to yield

$$R_\epsilon(q) + \sum_{i=-\infty}^k g_{k-i} R_\epsilon(k+q-i) + \sum_{j=-\infty}^{k+q} g_{k+q-j} R_\epsilon(j-k) \\ + \sum_{i=-\infty}^k \sum_{j=-\infty}^{k+q} g_{k-i} g_{k+q-j} \{ R_\epsilon(i-j) - \delta(i-j) R_\epsilon(0) \} \\ = \sum_{i=-\infty}^k \sum_{j=-\infty}^{k+q} g_{k-i} g_{k+q-j} R_\gamma(i-j). \quad (20)$$

The approximations

$$E(a_i a_{i+1} a_j a_{j+1} \tilde{\epsilon}_i \tilde{\epsilon}_j) \simeq R_\epsilon(0) \delta(i-j)$$

and

$$E(a_i a_j \tilde{\epsilon}_i \gamma_j) \simeq 0$$

needed to obtain (20) are justified in [16, Appendix D]. The terms retained in (20) were found to be the dominant terms by computer simulation, and the small errors associated with these approximations diminish as the synchronizer bandwidth is reduced.

The z transform can be applied to each term in (20) to obtain

$$S_\epsilon(z)(1+G(z))(1+G(1/z)) - G(z)G(1/z)R_\epsilon(0) \\ = G(z)G(1/z)S_\gamma(z) \quad (21)$$

where the z transform of the autocorrelation function $R_\epsilon(q)$ is defined to be

$$S_\epsilon(z) = \sum_q R_\epsilon(q) z^{-q} \quad (22)$$

with a similar definition for $S_\gamma(z)$. Rearranging (21) yields

$$S_\epsilon(z) = H(z)H(1/z)S_\gamma(z) + H(z)H(1/z)R_\epsilon(0) \quad (23)$$

where the DPLL feedback transfer function $H(z)$ is defined to be

$$H(z) \triangleq \frac{G(z)}{1+G(z)}. \quad (24)$$

The mean-squared value of $\tilde{\epsilon}_k$ is [17]

$$R_{\tilde{\epsilon}}(0) = \frac{1}{2\pi} \int_{-\pi}^{\pi} S_{\tilde{\epsilon}}(\omega) d\omega \quad (25)$$

where $S(\omega) = S(z)|_{z=e^{j\omega}}$.

Note that ω is normalized such that $T = 1$.

Substituting (23) in (25) and rearranging to solve for $R_{\tilde{\epsilon}}(0)$, we find

$$\sigma_{\tilde{\epsilon}}^2 = R_{\tilde{\epsilon}}(0) = \frac{\frac{1}{2\pi} \int_{-\pi}^{\pi} |H(\omega)|^2 S_{\gamma}(\omega) d\omega}{1 - 2B_L T} \quad (26)$$

where $2B_L T$ is the equivalent noise bandwidth of the transfer function $H(z)$ [15], [18]

$$2B_L T = \frac{1}{2\pi} \int_{-\pi}^{\pi} |H(\omega)|^2 d\omega. \quad (27)$$

The power spectral density (psd) $S_{\gamma}(\omega)$ is the Fourier transform of $R_{\gamma}(q)$. From statistical independence, γ_k defined in (17) is the sum of two mutually uncorrelated sequences with an autocorrelation function

$$R_{\gamma}(q) = 4E[b_k(\tau_k - \hat{\tau}_k)b_{k+q}(\tau_{k+q} - \hat{\tau}_{k+q}) + 4E[b_k n_k b_{k+q} n_{k+q}] \quad (28)$$

$$= R_I(q) + R_N(q) \quad (29)$$

where $R_I(q)$ is related to the pulse overlap (ISI) and $R_N(q)$ to the additive noise.

The psd $S_{\gamma}(\omega)$ is the Fourier transform of (29)

$$S_{\gamma}(\omega) = S_I(\omega) + S_N(\omega). \quad (30)$$

Substituting (30) into (26) yields

$$\sigma_{\tilde{\epsilon}}^2 = \frac{\frac{1}{2\pi} \int_{-\pi}^{\pi} |H(\omega)|^2 [S_I(\omega) + S_N(\omega)] d\omega}{1 - 2B_L T} = \sigma_{p_j}^2 + \sigma_{n_j}^2. \quad (31)$$

Comparing (31) to the result obtained for $\sigma_{\tilde{\epsilon}}^2$ in [14]² it is evident that the two equations differ in the sign of $2B_L T$ in the denominator [16, Appendix B].

The two terms $\sigma_{p_j}^2$ and $\sigma_{n_j}^2$ in (31) are evaluated in Appendixes A and B, respectively, in terms of $x(t)$, $G(z)$, E_b/N_o , l , and m , thus completing the determination of $\sigma_{\tilde{\epsilon}}^2$.

In Appendix C, $\sigma_{n_j}^2$ is given for $F(z) = 1$ in (15) and $\tau_k = \hat{\tau}_k = 0$ in (17) (no pulse overlap) in order to demonstrate the effect of the m bit delay in the feedback on $\sigma_{n_j}^2$ and $2B_L T$ when the loop gain $K \triangleq K_{PD}K_{NCO}$ is held constant.

IV. ADAPTIVE PATTERN JITTER COMPENSATION

The analysis of the pattern jitter compensation technique assumes that $x(t)$ is known at the synchronizer. Often due to filter imperfections and nonideal channel equalization $x(t)$ may not be accurately known. It is therefore of interest to examine an adaptive pattern jitter compensation technique based on the previous analysis.

Consider the linearized value of the compensation sequence $\hat{\tau}_k$ defined in (12). If $x(t)$ is not known, the value of $x(t_o - iT)$ may be replaced by an estimated value $\hat{x}_{k,i}$. The unknown constant

²Equation (62) of [14], with appropriate symbol substitutions and ignoring the psd due to pilot tone recovery.

c may also be lumped in with this estimate. Including the m bit delay the adaptive estimate of $\hat{\tau}_{k-m}$ may be written as

$$\hat{\tau}_{k-m} = a_{k-m} \sum_{\substack{i=-1 \\ i \neq 0,1}}^{m+1} a_{k-m+i} \hat{x}_{k,i}. \quad (32)$$

The estimates $\hat{x}_{k,i}$ may be recursively generated by applying the stochastic gradient algorithm [19] to yield the coefficient update equation

$$\hat{x}_{k+1,i} = \hat{x}_{k,i} + \beta u_k a_{k-m} a_{k-m+i} \quad (33)$$

where u_k is from Fig. 4 and β is the update equation gain constant. The value of β is chosen to be small enough to ensure that the adaptation does not interfere with the acquisition performance of the synchronizer.

V. SIMULATION RESULTS

A computer simulation of the pattern jitter compensation synchronizer is carried out to verify that the assumptions made in the analysis are reasonable, and to determine the effectiveness of the proposed synchronization technique.

The synchronizer used in the simulations operates with $F(z) = 1$, and loop gain K . Two simulation methods, a linear simulation and an actual simulation, are used. The linear simulation uses the linearized values of n_k , τ_k , and $\hat{\tau}_k$ from (9), (11), and (12), respectively, to determine the timing jitter variance $\sigma_{\tilde{\epsilon}}^2$ using Monte-Carlo methods. The actual simulation results are based on timing jitter variance estimates from the generation of actual signal and noise waveforms. Details of the simulation are described in [16, Appendix F].

Simulation results are presented for spectral raised cosine (SRC) signaling pulses [13]

$$x(t) = \frac{\sin(\pi t/T)}{(\pi t/T)} \left[\frac{\cos(\alpha \pi t/T)}{1 - 4\alpha^2(t/T)^2} \right]$$

and for a realizable data transmission filter [11] with a nominal cutoff frequency $1/2T$ with normalized ($T = 1$) poles and zeros as listed in Table I. The eye diagram for this filter, given in [11], clearly illustrates the presence of pulse overlap at the zero crossings, and the absence of ISI at the optimum sampling time.

The pattern jitter result in (31) does not depend on the matched filter model in Fig. 1 but only on the impulse response $x(t)$ of the cascade of the two filters. For the realizable filter, it is assumed that the variance σ_{η}^2 is equal to the optimum for matched filter operation [13], and is determined according to (B11). The samples $\eta(kT + t_o + \epsilon)$ in (9) are assumed to be independent from sample to sample. The correctness of these two assumptions is dependent on how accurately the filter can be partitioned into an approximate matched filter cascade.

In the following, the simulation results are compared to the calculated $\sigma_{n_j}^2$ and $\sigma_{p_j}^2$, determined by numerical integration of (B8) and (A1), respectively.

The performance of the pattern jitter compensation technique with SRC signaling pulses is compared to the uncompensated synchronizer for the following number of terms in the pattern jitter compensation estimate $\hat{\tau}_k$ in (4): 4 b ($l = m = 1$), 6 b ($l = m = 2$), and 8 b ($l = m = 3$). Simulation results are based on the linearized values for n_k , τ_k , and $\hat{\tau}_k$ from (9), (11), and (12), respectively, and an SRC $x(t)$.

Fig. 6 compares the calculated and linear simulation results for $\sigma_{p_j}^2$. The value of K is fixed such that in (C6) $2B_L T = 0.025$ for

TABLE I
POLES AND ZEROS OF THE DATA TRANSMISSION FILTER.

$p_{1,2}$	$-0.4236 \pm j3.01469$
$p_{3,4}$	$-0.71633 \pm j2.13020$
$p_{5,6}$	$-0.77845 \pm j1.05600$
p_7	-0.76847
$z_{1,2}$	± 2.12453
$z_{3,4}$	± 4.74191

the uncompensated synchronizer ($m = 0$). Thus $2B_L T$ will take on a different value for each m . It is apparent that at very small values of α , the data sequence lengths are not sufficient to yield a significant improvement. The improvement in σ_{pj}^2 for $\alpha \geq 0.2$ is quite good. Note that at some specific values of α the jitter variance of the longer length sequence is larger than that of the shorter sequence. This can be explained by recognizing the fact that at these values of α , the precursor and postcursor tails of the longer sequence pass through zero at $t = t_o - (m + 1)T$, and $t = t_o + lT$, respectively. Therefore, the longer sequence does not compensate for any additional pulse overlap, but performance will be degraded by the slightly larger $2B_L T$ due to the extra delay m in the feedback loop of the PLL. Similar results are obtained for other values of K [16].

The performance of the pattern jitter compensation technique in the presence of additive noise is illustrated in Fig. 7 with $\alpha = 0.3$ and K fixed such that $2B_L T = 0.10$ for $m = 0$. The simulation points are compared to the calculated timing-error variance $\sigma_e^2 = \sigma_{pj}^2 + \sigma_{nj}^2$, where σ_{nj}^2 and σ_{pj}^2 are determined by (B8) and (A1), respectively. The simulation points are in close agreement with the analytical results. The approximations used to obtain (20) account for the slight discrepancies between calculated and simulated results. At low E_b/N_o , the jitter variance σ_e^2 for different values of m is asymptotic to σ_{nj}^2 for the corresponding feedback delay m . The jitter reduces as E_b/N_o increases as expected, but is lower bounded by the residual pattern jitter. For $E_b/N_o \leq 35dB$, the performance of the 8 bit compensation sequence synchronizer has a jitter variance only slightly larger than that of σ_{nj}^2 . Therefore pattern jitter is effectively eliminated from the synchronizer output for all practical E_b/N_o . The larger value of $2B_L T$ due to the m bit delay in the feedback path is illustrated by the difference between the $m = 0$ and $m = 3$ curves calculated for σ_{nj}^2 .

For larger values of α the required sequence length to effectively eliminate pattern jitter will decrease. With $\alpha = 0.5$, a sequence length of only 6 b ($l = m = 2$) gives performance nearly equivalent to the synchronizer operating in the absence of pulse overlap at the zero crossings [16]. Again the simulation results are in close agreement with the analysis [16].

The proposed synchronizer is also evaluated using actual SRC pulses and a filtered noise waveform. The actual simulation yields results are very close to the linear analysis and the linear simulation [16], confirming that for an SRC system, the linear assumptions made in the analysis are a reasonable approximation to the actual case. For very small values of $\alpha < 0.1$, or for $E_b/N_o < 5dB$ there is some divergence between the linear and actual curves, where the pulse overlap and additive noise is too large for the linear analysis to apply.

The jitter variances σ_{pj}^2 and σ_{nj}^2 of a synchronizer operating on signaling pulses generated by the 7th-order transmission filter are calculated from (A1) and (B11), respectively. The calculated and simulated timing jitter variance $\sigma_e^2 = \sigma_{nj}^2 + \sigma_{pj}^2$ as a function of E_b/N_o is illustrated in Fig. 8. K is fixed so that the bandwidth of

the synchronizer is $2B_L T = 0.1$ for $m = 0$. Again, the agreement between the calculated and simulated results is quite good. Also apparent is that a 9 b compensation sequence ($l = 6, m = 1$) will effectively eliminate the pattern jitter for most practical E_b/N_o .

The adaptive synchronization technique described in Section IV is verified in [16]. In addition, an implementation of the synchronizer using a TMS 32020 digital signal processing integrated circuit was used to confirm the simulation results. Laboratory measurements indicate that for NRZ pulses filtered by a 4th-order Butterworth filter, pattern jitter is essentially eliminated using a 4 b compensation sequence with no feedback delay [16].

VI. CONCLUSION

The pattern jitter component of a zero-crossing tracking PLL synchronizer may be reduced well below the noise jitter component by using a short sequence of received data bits to predict the effect of pulse overlap on the zero-crossing locations. Pattern jitter compensation can be based on a known impulse response, measured zero-crossing locations, or in an adaptive implementation. The number of bits in the compensation sequence depends on the rate at which the system impulse response decays, which is generally determined by the operating bandwidth of the system. The advantage of this method of reducing pattern jitter is that a prefilter is not required. The bit synchronizer is suitable for a completely digital implementation.

Three methods are presented to determine the timing jitter variance performance of the synchronizer. First, analytical equations based on linear approximations are derived. The analysis is more complete than a previous result [14], and it also includes the pattern jitter compensation. The new result is exact for white noise disturbances (for example, additive noise at a matched filter output) and simulation results indicate that it is more accurate for nonwhite disturbances (e.g., pulse overlap) as well. Second, the linear assumptions made in the analysis can be used to generate a recursive timing equation which can be evaluated using Monte-Carlo techniques to determine the jitter variances. The third technique is to directly simulate the synchronizer by generating the required waveforms, and recovering the timing information. Any of the aforementioned methods can be used by designers to estimate the compensation sequence lengths to reduce the pattern jitter below a required level.

For operation with SRC signaling pulses, both the linear and actual simulation results are in close agreement with the analytical results. The analysis is also effective in predicting the jitter variance of a synchronizer operating on pulse waveforms generated by a 7th-order realizable data transmission filter.

The simulation results and analysis also verified the effectiveness of the proposed pattern jitter compensation technique. The results demonstrate that the technique can be used on SRC signaling pulses to greatly reduce the pattern jitter component of the synchronizer. For a small excess bandwidth $\alpha = 0.3$, the pattern jitter is essentially eliminated for $E_b/N_o < 35$ dB using an 8 b compensation sequence. An excess bandwidth of $\alpha = 0.5$ requires only a 6 b sequence.

The 7th-order realizable data transmission filter required a sequence length of 9 b, with only 1 b feedback delay ($m = 1$). The performance of the synchronizer indicates that it may find application in low-cost digital synchronizer implementations for a bandlimited binary data communications system, where the pattern jitter in the synchronizer is expected to be a concern.

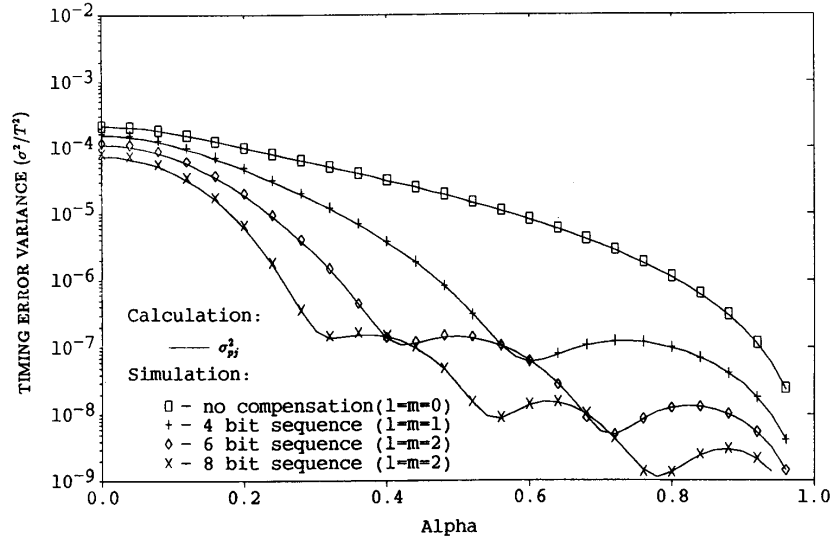


Fig. 6. Linear simulation of the synchronizer pattern jitter variance versus alpha. K is fixed such that $2B_L T = 0.025$ for $m = 0$.

For applications where the impulse response is not accurately known, the adaptive pattern jitter compensation technique may be appropriate. Alternately, the zero-crossing locations may be measured and fixed compensation sequence values used.

The performance of the compensation technique for multilevel signaling and in the presence of a frequency offset has not been addressed in the analysis or simulations, and is an area for further study.

APPENDIX A:

CALCULATION OF PATTERN JITTER VARIANCE

In this Appendix, the pattern jitter variance σ_{pj}^2 is determined using (31) with $S_N(\omega) = 0$, so that

$$\sigma_{pj}^2 = \frac{\frac{1}{2\pi} \int_{-\pi}^{\pi} |H(\omega)|^2 S_I(\omega) d\omega}{1 - 2B_L T} \quad (\text{A1})$$

where $S_I(\omega)$ is determined from $R_I(q)$. From (28) and (29)

$$R_I(q) = 4E[b_k(\tau_k - \hat{\tau}_k)b_{k+q}(\tau_{k+q} - \hat{\tau}_{k+q})]. \quad (\text{A2})$$

Substituting (11), (12), and (14) for τ_k , $\hat{\tau}_k$, and b_k , respectively, and retaining only the non-zero expectation terms in (A2)

$$R_I(0) = 2c^2 \sum_{i \notin P} x^2(t_o - iT) \quad (\text{A3})$$

$$R_I(\pm 1) = -c^2 \left\{ \sum_{i \notin P \cup Q} x(t_o - iT)x(t_o - (i+1)T) - A_2 B_{-2} \right\} \quad (\text{A4})$$

$$R_I(q) = c^2 [A_q - B_q][A_{-q} - B_{-q}] \quad \text{for } q \neq 0, \pm 1 \quad (\text{A5})$$

where P is the sequence

$$\{-l, \dots, 0, 1, \dots, m+1\} \quad (\text{A6})$$

Q is the sequence

$$\{-(l+1), \dots, -1, 0, \dots, m\} \quad (\text{A7})$$

$$A_q = \begin{cases} x(t_o - qT) & \text{for } q \notin P \\ 0 & \text{for } q \in P \end{cases} \quad (\text{A8})$$

$$B_q = \begin{cases} x(t_o - (q+1)T) & \text{for } q \notin Q \\ 0 & \text{for } q \in Q. \end{cases}$$

The psd $S_I(\omega)$ is the Fourier transform of $R_I(q)$

$$S_I(\omega) = R_I(0) + 2 \sum_{q=1}^{\infty} R_I(q) \cos(\omega q) \quad (\text{A9})$$

$S_I(\omega)$ is used in (A1) to determine σ_{pj}^2 .

If $x(t)$ has a Fourier transform $X(f)$ strictly bandlimited to the frequency interval $[-1/T, 1/T]$ with nominal zero-crossing locations $t_o = T/2$, then the infinite summations in (A3) and (A4) may be reduced to finite sums. Application of the Poisson summation formula

$$\sum_i v(iT) = \frac{1}{T} \sum_p V(-p/T)$$

to (A3) yields

$$R_I(0) = 2c^2 \left\{ \frac{1}{T} \sum_{p=-1}^1 (-1)^p \int_{-\infty}^{\infty} X^*(f)X\left(f + \frac{p}{T}\right) df - \sum_{i \in P} x^2(T/2 - iT) \right\}. \quad (\text{A10})$$

Similarly, for (A4) the result is

$$R_I(\pm 1) = -c^2 \left\{ \frac{1}{T} \sum_{p=-1}^1 (-1)^p \int_{-\infty}^{\infty} X^*(f)X\left(f + \frac{p}{T}\right) e^{-j2\pi f T} df - \sum_{i \in P \cup Q} x(T/2 - iT)x(-T/2 - iT) - A_2 B_{-2} \right\} \quad (\text{A11})$$

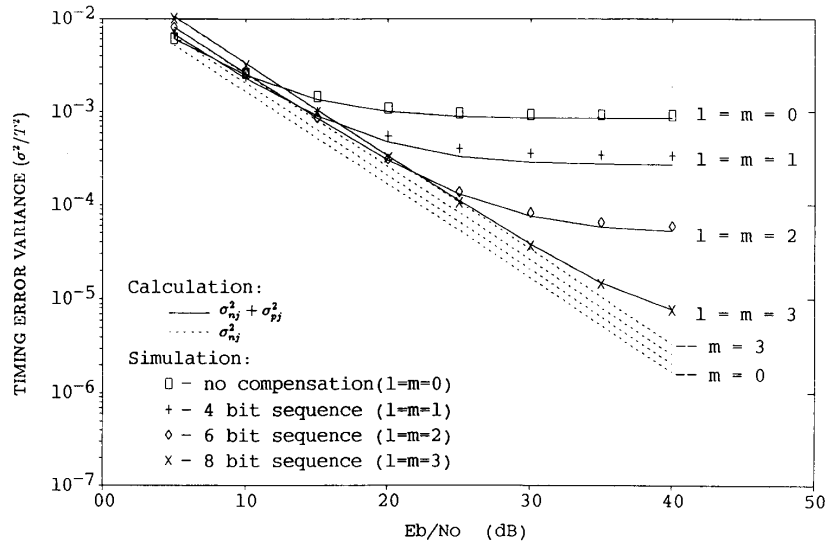


Fig. 7. Linear simulation of the synchronizer jitter variance versus E_b/N_0 with $\alpha = 0.3$. K is fixed such that $2B_L T = 0.10$ for $m = 0$.

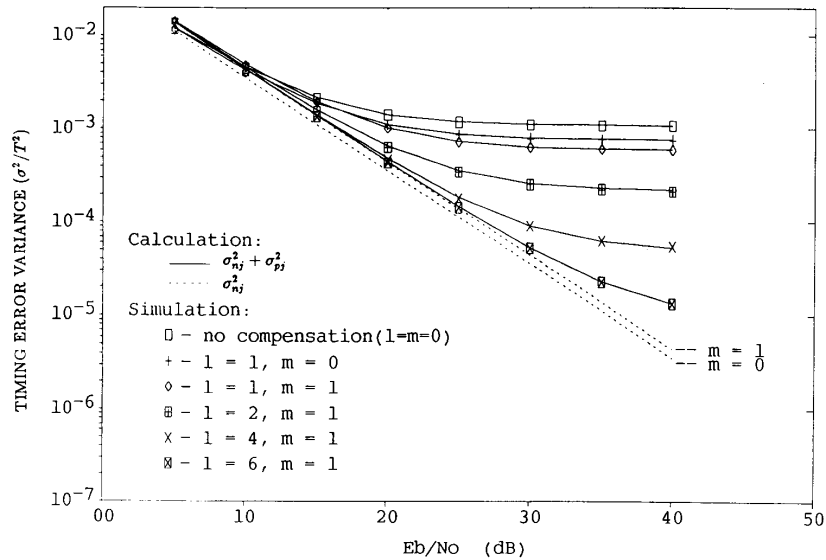


Fig. 8. Linear simulation of the synchronizer jitter variance for the 7th-order data transmission filter. K is fixed such that $2B_L T = 0.1$ for $m = 0$.

APPENDIX B:

CALCULATION OF ADDITIVE NOISE JITTER VARIANCE

In this Appendix, the noise jitter variance $\sigma_{n_j}^2$ is determined using (31) with $S_I(\omega) = 0$, so that

$$\sigma_{n_j}^2 = \frac{\frac{1}{2\pi} \int_{-\pi}^{\pi} |H(\omega)|^2 S_N(\omega) d\omega}{1 - 2B_L T} \quad (\text{B1})$$

where $S_N(\omega)$ is determined from $R_N(p)$. From (28) and (29)

$$R_N(q) = 4E[b_k n_k b_{k+q} n_{k+q}]. \quad (\text{B2})$$

Using the linear approximation (9) for n_k and (14) for b_k , and evaluating the expectation yields [14]

$$R_N(0) = 2c^2 R_\eta(0) \quad (\text{B3})$$

$$R_N(\pm 1) = -c^2 R_\eta(\pm T) \quad (\text{B4})$$

$$R_N(q) = 0 \quad \text{for } q \neq 0, \pm 1 \quad (\text{B5})$$

where $R_\eta(\tau)$ is the continuous autocorrelation function of $\eta(t)$.

The psd $S_N(\omega)$ is the Fourier transform of $R_N(q)$

$$S_N(\omega) = R_N(0) + 2R_N(1) \cos(\omega) \quad (\text{B6})$$

$$= 2c^2 \{ \sigma_\eta^2 - R_\eta(T) \cos(\omega) \} \quad (\text{B7})$$

where $R_\eta(0) = \sigma_\eta^2$ is the variance of the zero-mean $\eta(t)$.

$S_N(\omega)$ is used in (B1) to determine $\sigma_{n_j}^2$.

For any LPF_R filter that satisfies $R_\eta(\pm T) = 0$ (for example, a Nyquist matched filter system) the psd $S_N(\omega)$ is discrete white noise, thus

$$\sigma_{n_j}^2 = \frac{2c^2\sigma_\eta^2 2B_L T}{1 - 2B_L T}. \quad (\text{B8})$$

To express $\sigma_{n_j}^2$ in terms of E_b/N_o , $x(t)$ and $2B_L T$, we define the normalized pulse $\tilde{x}(t) \triangleq x(t)/A$, where A is the amplitude of the received data signal $s(t - \epsilon)$ at the optimum data sample location $t = kT + \epsilon$. Assuming $x(t)$ is reasonably symmetrical about $t = 0$, the nominal zero-crossings are located midway between the data samples. From (10), c may then be approximated by

$$c \approx \frac{1}{2A\tilde{x}'(T/2)}. \quad (\text{B9})$$

For optimal matched filter detection of binary antipodal signals it is known that [13]

$$\frac{A^2}{\sigma_\eta^2} = \frac{2E_b}{N_o} \quad (\text{B10})$$

where E_b is the transmitted bit energy at the LPF_R input. Thus

$$\sigma_{n_j}^2 \approx \frac{N_o B_L T}{2E_b(1 - 2B_L T)\{\tilde{x}'(T/2)\}^2}. \quad (\text{B11})$$

The noise jitter variance may be reduced by increasing E_b/N_o , or by reducing the PLL bandwidth $2B_L T$ (at the expense of acquisition performance), or by increasing the slope of the waveform $\tilde{x}(T/2)$.

APPENDIX C:

EFFECT OF m -BIT FEEDBACK DELAY ON THE ADDITIVE NOISE JITTER VARIANCE

To demonstrate the effect of the m bit delay in the feedback on $\sigma_{n_j}^2$ and $2B_L T$, we calculate $\sigma_{n_j}^2$ for $F(z) = 1$, $\tau_k = \hat{\tau}_k = 0$, and $R_\eta(\pm 1) = 0$. Instead of using (B8) which requires evaluating the integral (27), we start with (16) specialized for this case

$$\tilde{\epsilon}_{k+1} = \tilde{\epsilon}_k + 2Kb_{k-m}(n_{k-m} - \tilde{\epsilon}_{k-m}) \quad (\text{C1})$$

and evaluate the mean-squared value of both sides of (C1) to obtain [16]

$$\sigma_{n_j}^2 = R_{\tilde{\epsilon}}(0) = \frac{Kc^2\sigma_\eta^2}{\rho_{\tilde{\epsilon}}(m) - K} \quad (\text{C2})$$

where

$$\rho_{\tilde{\epsilon}}(m-p) = E[\tilde{\epsilon}_k \tilde{\epsilon}_{k-m-p}] / R_{\tilde{\epsilon}}(0), \quad p = 0, 1, \dots, m-1. \quad (\text{C3})$$

Substituting (C1) in (C3) and evaluating the expectation yields

$$\rho_{\tilde{\epsilon}}(m-p) = \rho_{\tilde{\epsilon}}(m-p-1) + K\rho_{\tilde{\epsilon}}(p+1), \quad p = 0, 1, \dots, m-1. \quad (\text{C4})$$

Recursive solutions to $\rho_{\tilde{\epsilon}}(m)$ for $m \leq 3$ are

$$\rho_{\tilde{\epsilon}}(m) = \begin{cases} 1 & m = 0 \\ \frac{1}{1+K} & m = 1 \\ \frac{1-K}{1+K(1-K)} & m = 2 \\ \frac{1-K(1+K)}{1+K+K(1-K(1+K))} & m = 3. \end{cases} \quad (\text{C5})$$

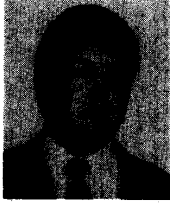
Equating (C2) and (B8) and solving for $2B_L T$ we find

$$2B_L T = \frac{K}{2\rho_{\tilde{\epsilon}}(m) - K}. \quad (\text{C6})$$

Since $\rho_{\tilde{\epsilon}}(m) \leq 1$, the m bit delay will generally degrade the noise performance of the synchronizer by increasing $2B_L T$. However, for small values of K and m , $\rho_{\tilde{\epsilon}}(m) \approx 1$, and the degradation will not be significant.

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