1. Draw the output waveforms of a NAND implemented RS latch which is initially reset when the following inputs are applied

\[
\begin{array}{c}
\text{r} \\
\text{s}
\end{array}
\]

2. Design using next state tables and excitation tables a D flip flop that uses a JK flip flop as the storage element.

3. Design using next state tables and excitation tables a T flip flop that uses a D flip flop as the storage element.

4. Design a 4 bit binary down counter that uses T flip flops.

5. An RS latch is modelled with 2 ideal NOR gates and a delay as shown below. What is the characteristic equation for the model? Use the characteristic equation to complete the following table that shows the response of the circuit to the given rs values.

\[
\begin{array}{c|c|c|c}
\text{tn} & \text{rn} & \text{sn} & \text{Qn} \\
0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 \\
2 & 0 & 1 & 1 \\
3 & 0 & 1 & 1 \\
4 & 0 & 0 & 0 \\
5 & 1 & 0 & 0 \\
6 & 1 & 1 & 1 \\
7 & 0 & 0 & 0 \\
8 & 0 & 0 & 0
\end{array}
\]

\[
\begin{array}{c}
\text{r} \\
\text{s}
\end{array}
\]

\[
\begin{array}{c}
\text{Qn+1} \\
\text{delay} \\
\text{Qn}
\end{array}
\]