This writeup describes the new CENG 440 design and implementation project. This project complements the lecture material of CENG 290 and CENG 440. The project is normally carried out during four 3 hour lab sessions and any additional time that may be required. The project is done in groups of 2 and one final report is required.

This project is intended to give you an introduction to state-of-the-art digital design and implementation using field programmable gate arrays (FPGA) and computer-aided-design (CAD) software from Xilinx.

Although the project is intended to be carried out using hardware and software supplied by the department, a student edition of the CAD software is available for about $120 and prototyping hardware is available for about $150. The software includes a manual that can be purchased separately for about $55. The lab has a limited number of the software manuals and Xilinx Data Books. The software has extensive online help. Detailed hardware data can be found at www.xilinx.com.

The hope is that this project will be interesting, challenging, educational, relevant and the appropriate amount of work.

This project involves the design, implementation and testing of an 8-bit nonrestoring division system. The theory of nonrestoring division is covered in the class notes on computer arithmetic. Your system is to use only a XC4010XL FPGA, switches and LEDs provided in the lab. Your system is to accept 2 8-bit unsigned numbers, execute its algorithm and display the resulting 8-bit quotient and remainder.
Your design must clearly separate the datapath and control functions. Use pseudocode and a state diagram to describe the control functions. Use the component macros available in the Xilinx Foundation CAD software for registers etc.. Your design is to be entered using schematic capture and simulated using functional simulation. Follow the examples given in the Practical Xilinx Designer Lab Book to help you learn how to do schematic capture, functional simulation, compilation and down loading to the hardware. Capture, simulate, compile and test small parts of the system as you work towards a total system. Use the hierarchical features of the software to encapsulate parts of the system. Bring internal signals out to pins so that a logic analyzer can be used for testing.

Your project report should describe what you did and give printouts of schematics, simulation waveforms, and logic analyzer waveforms. Good datapath diagrams and state diagrams are required. Resource reports available from the Foundation software should also be included in your project report.

The specifications and requirements given above are intended to give you considerable freedom in your design so that you will have to make critical design decisions. The project should consolidate what you have studied in CENG 290 and CENG 440 and give you confidence as a logic designer! This is not a mickey mouse lab!