CENG 440 ASSIGNMENT 2

1. An RS flip flop is built with 2 cross coupled NAND gates. If the gates are modeled as perfect gates with a 5 ns delay is the flip flop stable when a R and an S are simultaneously deasserted?

2. Answer question 1 when one gate has a 5 ns delay and the other a 10 ns delay.

3. Consider the FSM analyzed on page 44 of the class notes. If the gate delays are 5 ns and the flip flop propagation delays, setup times and hold times are 10 ns, 7 ns and 2 ns respectively, what is the maximum clock frequency and skew?

4. Consider a system for nonrestoring division as discussed in class. Assume an 8 bit quotient register, an 8 bit remainder register and a 3 bit counter for counting cycles. Give a state diagram and an ASM diagram for a suitable controller. Carefully define the input and output control signals of your controller.