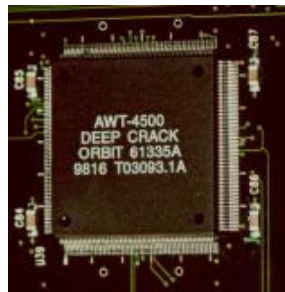


Computer Organization I

Lecture 3: von Neumann Architecture (Part I)

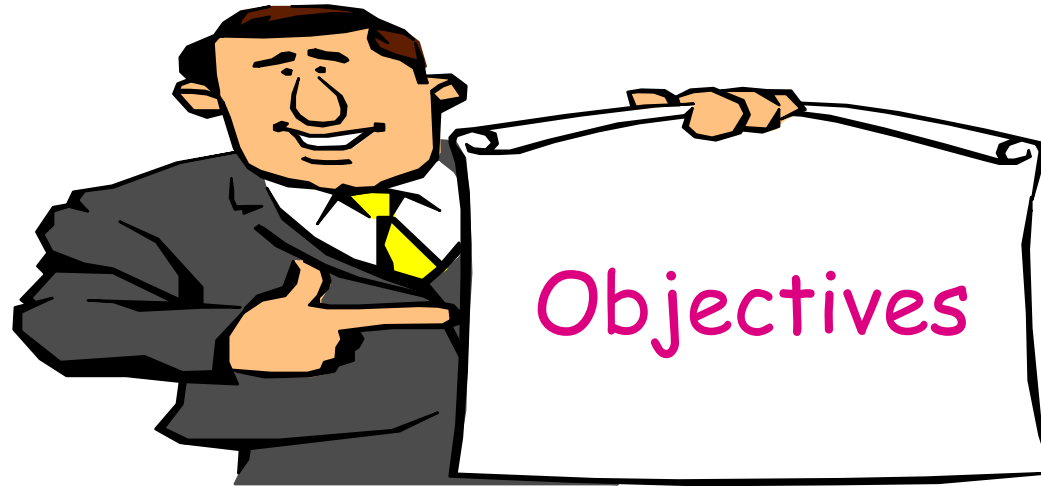


**von Neumann
Architecture**





- ✓ General Architecture of von Neumann Machine
 - Memory Subsystem;
 - Arithmetic Logic Unit;
 - Control Unit;

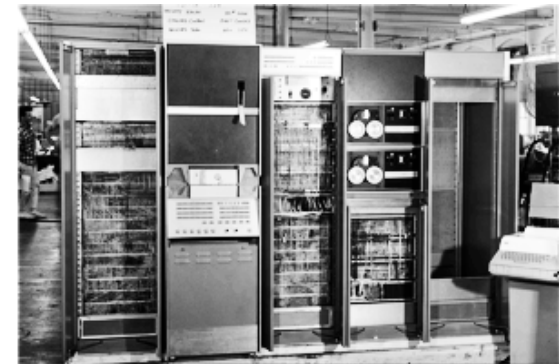


- ✓ Understand how the von Neumann machine works
- ✓ Understand the main functions of components included in von Neumann architecture

von Neumann Architecture

- why it is important?

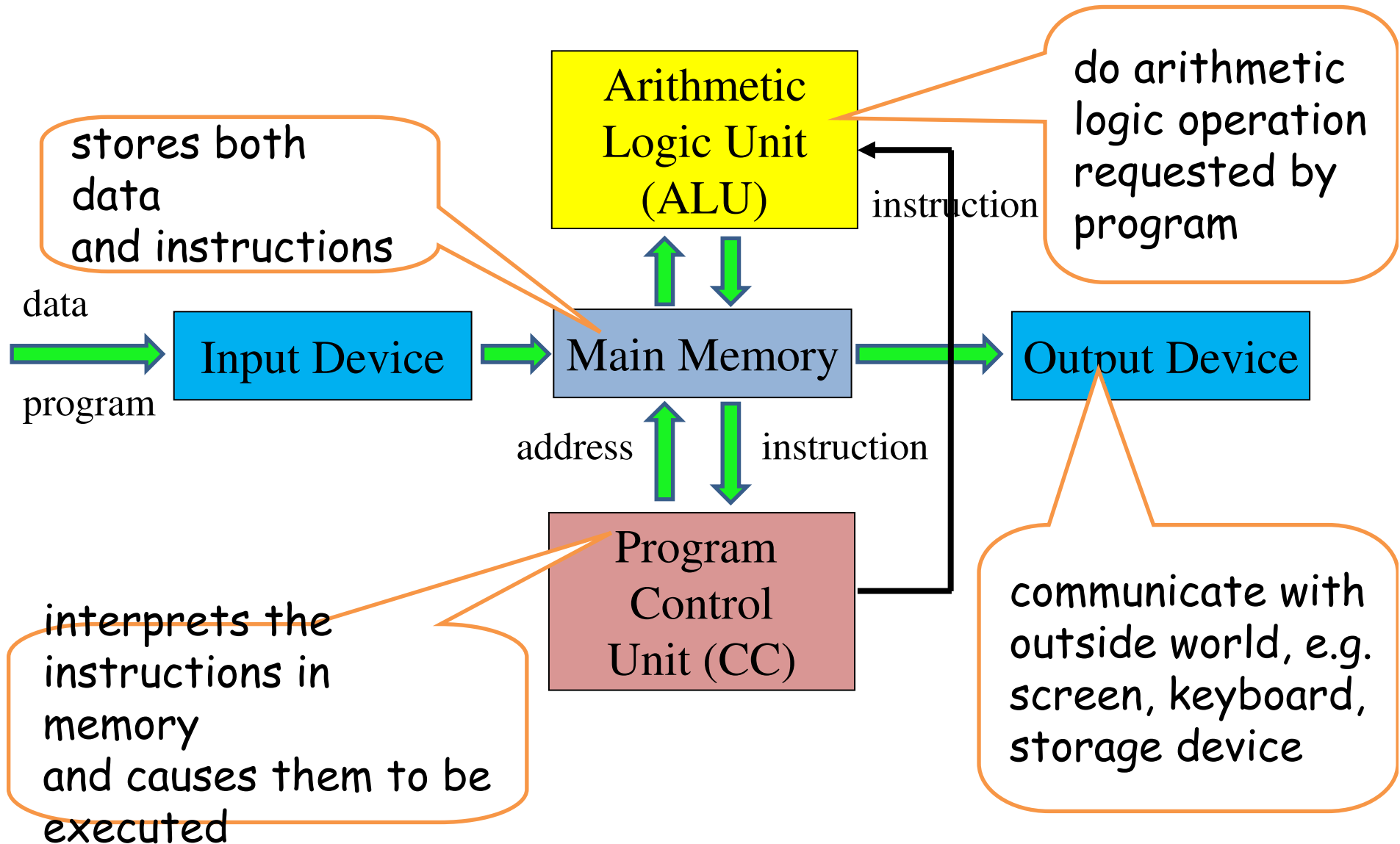
- All computers more or less based on the same basic design, the **von Neumann Architecture!** what ever it be a multi-million dollar mainframe or a Palm Pilot.



- The von Neumann architecture describes a general framework, or structure, that a computer's **hardware, programming, and data** should follow.

von Neumann Architecture

- what is von Neumann architecture?



von Neumann Architecture

- how von Neumann computer works?

Step 1. send data and program 1+1 to main memory through input device

data
1+1
program

Input Device

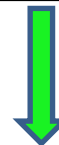


Arithmetic Logic Unit (ALU)



Main Memory

address



instruction

Program Control Unit (CC)

Step 4. ALU store results to memory

instruction

Output Device



Step 2. CC read + instruction from memory according to address

Step 3. CC send instruction to ALU, and then read data 1 and 1 from memory to ALU according to address

Step 5. output results from memory to output device through instruction



von Neumann Architecture

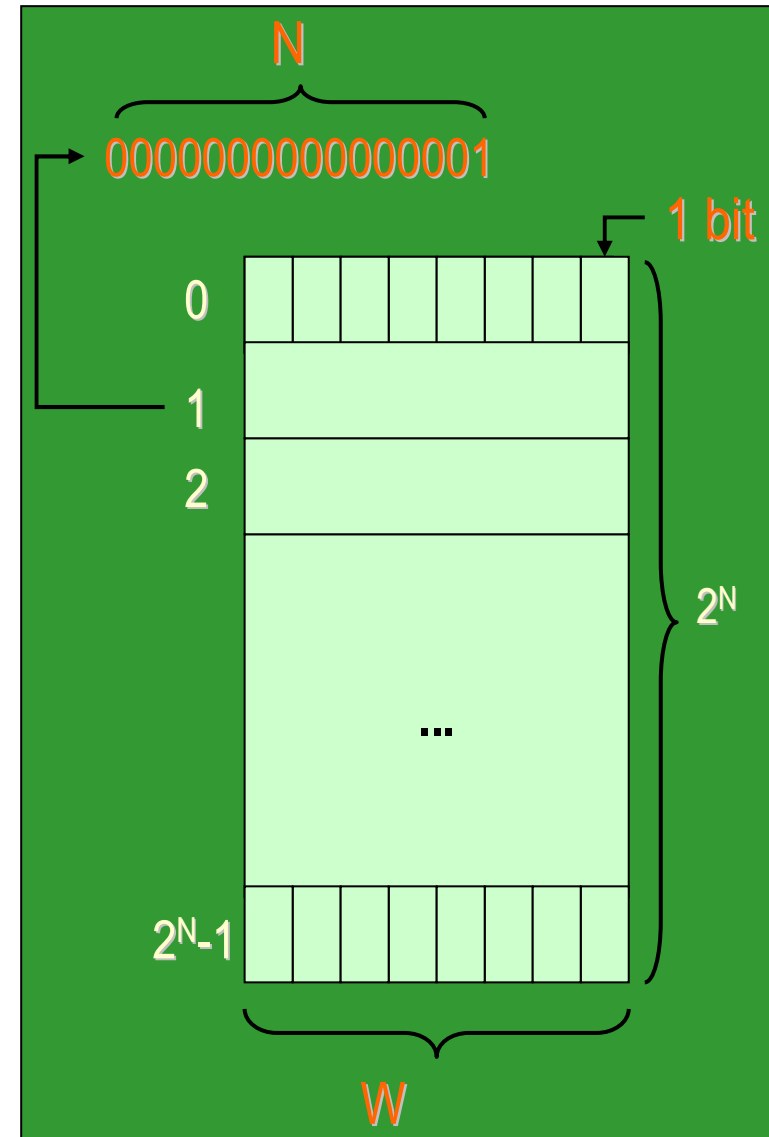
- what is memory subsystem?

- **Memory, also RAM (Random Access Memory)**
 - Consists of many memory cells (storage units) of a fixed size.
Each cell has an address associated with it: 0, 1, ...
 - Each cell has two important characteristics:
 - (1) its address (where it is),
 - (2) its contents (what's stored at the given location).

von Neumann Architecture

- what is memory subsystem?

- **Memory width (W)**
 - How many bits is each memory cell, typically one **byte** (=8 bits)
- **Address width (N)**
 - How many bits used to represent each address, determines the maximum memory size = **address space**
 - If address width is **N**-bits, then address space is 2^N ($0, 1, \dots, 2^N - 1$)
- **Address space**
 - the number of uniquely identifiable memory locations.



von Neumann Architecture - what is memory subsystem?

For example, for a 256 Mbyte memory, suppose its memory width is 8 bits (or 1 bytes)

What is its address space?

2^{28}

What is its address width?

28

von Neumann Architecture - what is memory subsystem?

For another example
a memory space is as follows:

000	
001	
010	
011	
100	0000 0110
101	
110	0000 0010
111	

- what is its memory width?
8 bits
- what is its address space?
8 bytes
- what is its address width?
3
- what is the content of memory
location address (4 = 100)?
(6 = 0000 0110)

von Neumann Architecture

- what is memory subsystem?

Measurements about RAM Size & Speed

- **Memory sizes:**
 - Kilobyte (KB) = 2^{10} = 1,024 bytes ~ 1 thousand
 - Megabyte (MB) = 2^{20} = 1,048,576 bytes ~ 1 million
 - Gigabyte (GB) = 2^{30} = 1,073,741,824 bytes ~ 1 billion
- **Memory access time (read from/ write to memory)**
 - 50-75 nanoseconds (1 nsec. = 0.000000001 sec.)
- **RAM is:**
 - volatile (can only store when power is on)

von Neumann Architecture

- what is memory subsystem?

Operations on Memory

- **Fetch (address):**
 - Fetch a copy of the content of memory cell with the specified address.
 - Non-destructive, copies value in memory cell.
- **Store (address, value):**
 - Store the specific value into the memory cell specified by address.
 - Destructive, overwrites the previous value of the memory cell.

von Neumann Architecture - what is memory subsystem?

Interface to Memory

- How does processing unit get data to/from memory?

MAR: Memory Address Register

MDR: Memory Data Register



- Fetch (Address):
 1. Load the address (A) into the MAR.
 2. Copy the content of memory cell with specified address into MDR.
- Store (Address, Value):
 1. Load the address into MAR; load the value into MDR
 2. copy content of MDR into memory cell with specified address.

von Neumann Architecture

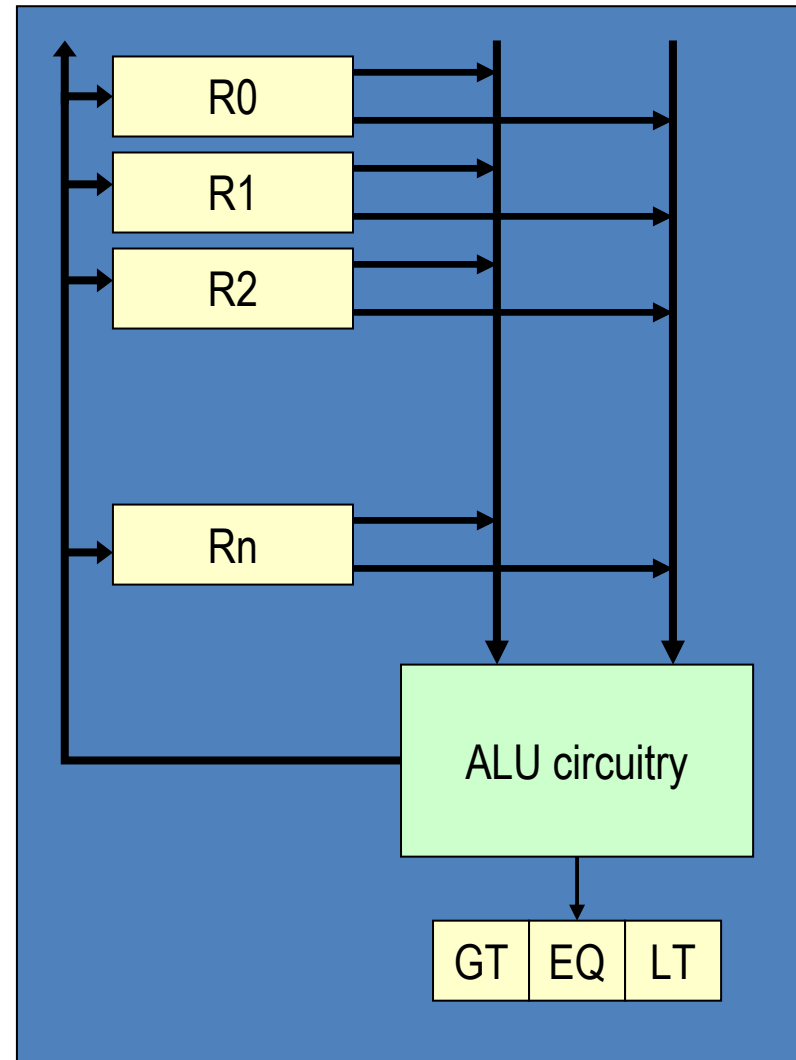
- what is ALU subsystem?

- The ALU (Arithmetic/Logic Unit) performs
 - mathematical operations (+, -, x, /, ...)
 - logic operations (=, <, >, and, or, not, ...)
- In today's computers integrated into the CPU
- Consists of:
 - Circuits to do the arithmetic/logic operations.
 - Registers (fast storage units) to store intermediate computational results.
 - Bus that connects the two.

von Neumann Architecture

- what is the structure of ALU subsystem?

- **Registers:**
 - very fast local memory cells, that store operands of operations and intermediate results.
 - CCR (condition code register), a special purpose register that stores the result of $<$, $=$, $>$ operations
- **ALU circuitry:**
 - Contains an array of circuits to do mathematical/logic operations.
- **Bus:** Data path interconnecting the registers to the ALU circuitry.



von Neumann Architecture

- what is control unit subsystem?

- Program is stored in memory
 - as machine language instructions, in binary
- The task of the control unit is to execute programs by repeatedly:
 - Fetch from memory the next instruction to be executed.
 - Decode it, that is, determine what is to be done.
 - Execute it by issuing the appropriate signals to the ALU, memory, and I/O subsystems.
 - Continues until the HALT instruction

von Neumann Architecture

- what is control unit subsystem?

Machine Language Instructions

- A machine language instruction consists of:
 - Operation code/opcode, telling which operation to perform
 - Address field(s)/operands, telling the memory addresses of the values on which the operation works.
- For Example: ADD X, Y (Add content of memory locations X and Y, and store back in memory location Y).
- Assume: opcode for ADD is 9, and addresses X=99, Y=100

Opcode (8 bits)	Address 1 (16 bits)	Address 2 (16 bits)
00001001	0000000001100011	0000000001100100