An Adaptive ENG Amplifier for Tripolar Cuff Electrodes

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***Abstract*—Electroneurogram (ENG) recording from tripolar cuff electrodes is affected by interference signals, mostly generated by muscles nearby. Interference reduction may be achieved by suitably designed amplifiers such as the true-tripole and quasi-tripole systems. However, in practice their performance is severely degraded by cuff imbalance, resulting in very low output signal-to-interference ratios. Although some improvement may be offered by post filtering, this considerably increases complexity, size and power dissipation, rendering the approach unsuitable for the development of a high-performance ENG recording system which is fully implantable. This paper describes an integrated, fully implantable, adaptive ENG amplifier developed to automatically compensate for cuff imbalance, and thus significantly improve the quality of the recorded ENG. Measured results show that the adaptive ENG amplifier has a yield of 100%, a cuff imbalance correction range of more than $\pm 40\%$, and an output signal-to-interference ratio of about 2/1 (6 dB) even for $\pm 40\%$ imbalance. The latter should be compared with an input signal-to-interference ratio of 1/500 (−54 dB). The circuit was fabricated in 0.8-μm BiCMOS technology, has a core area of 0.68 mm^2, and dissipates 7.2 mW from ± 2.5 V power supplies. The adaptive ENG amplifier advances the state-of-the-art in implantable tripolar nerve cuff electrode recording techniques.**

***Index Terms*—Analog integrated circuits, cuff imbalance, ENG amplifier, implanted devices, tripolar cuff electrodes.**

I. Introduction

ELECTRONEUROGRAM (ENG) recording techniques for peripheral nerves using cuff electrodes offer a noninvasive way of obtaining information regarding nerve operation [1]. In the case of spinal cord injury this information can be used for the improvement of implanted devices used for rehabilitation. Monitoring nerve operation allows some level of intervention by means of functional electrical stimulation for partial control of organs suffering from paralysis and for blockage of unwanted sensory and/or motor signals. Applications that have been investigated include the correction of foot-drop, stimulating hand-grasp, and controlling the urinary bladder after spinal cord injury [2]–[4].

Recording ENG effectively is not a trivial task, as the microvolt-order (typically 1–5 μV) nerve signals are often obscured by the millivolt-order (typically 1 mV) electromyogram (EMG) from muscles nearby and by noise, notably white noise from the interstitial fluid and from the electrode–tissue interface [5], [6]. Furthermore, the spectra of the two signals overlap considerably, making separation by means of filtering very difficult [7]; the ENG has an energy in the 500 Hz–10 kHz band with maximum power around 1 kHz, while the EMG lies in the 1 Hz–3 kHz band and peaks at about 250 Hz [6]. Various ENG amplifier configurations make use of the properties of the cuff electrodes, mainly the *linearization* of the EMG potential field inside the cuff [8]. Improved performance in terms of EMG reduction is offered by tripolar cuffs (i.e., cuffs with three equally spaced ring electrodes embedded in the inside wall [1]). Due to this linearization, the EMG potential differences between the central electrode and the outer electrodes are equal and opposite and can be cancelled by a differential amplifier arrangement. By contrast, the ENG signal does *not* cancel in this way and can be recovered. The amplifiers used with tripolar cuffs are the *quasi-tripole* (QT) [1], [6] and *true-tripole* (TT) [9]. However, EMG reduction in these systems is affected by the departure of the cuff–tissue interface from its ideal model, caused by factors like cuff asymmetry and tissue growth inside it after implantation, resulting in *cuff imbalance* as explained in more detail in Section II.

To automatically compensate for the possible presence of cuff imbalance, and thus minimize EMG artifacts in nerve cuff electrode recording, an adaptive version of the TT, termed the *adaptive-tripole* (AT), has been proposed [10] and its first integrated realization was reported in [11]. However, the realization in [11] showed poor performance in terms of output *signal-to-interference ratio* (SIR),[1] harmonic distortion, cuff imbalance correction range, and yield. This paper describes an improved realization of the AT which overcomes all the limitations of the first design. These enhancements were necessary in order to make the system fully implantable for the targeted biomedical application (i.e., bladder implant). The adaptive ENG amplifier to be described has a chip yield of 100%, a cuff imbalance correction range of more than $\pm 40\%$, and an output SIR of no less than 2 dB even for $\pm 40\%$ imbalance. The circuit was fabricated in 0.8-μm BiCMOS technology, occupies 0.68 mm^2, and dissipates 7.2 mW from ± 2.5 V power supplies.

The remaining sections of this paper are organized as follows. In Section II, the basic principles of ENG recording from tripolar cuff electrodes are briefly reviewed. Section III describes the AT architecture and examines the effect of phase errors on system performance. Section IV describes the circuit design of the various building blocks, while measured results are presented in Section V. Finally, conclusions are drawn in Section VI.

[1]SIR refers to the ratio of the peak amplitude of the ENG signal over that of the EMG signal.

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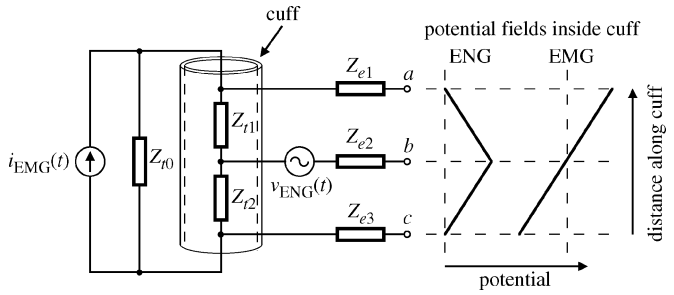

Fig. 1. Lumped-impedance model of the cuff and idealized ENG and EMG potentials inside the cuff [6], [12]. Typical impedance values: $Z_{t0} = 200\ \Omega$, $Z_{t1,2} = 1.25\ \mathrm{k}\Omega$, $Z_{e1,2,3} = 1\ \mathrm{k}\Omega$.

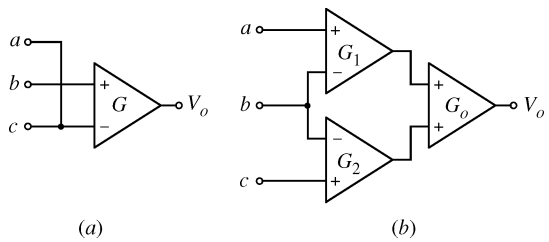

Fig. 2. Tripolar ENG amplifier configurations. (a) Quasi-tripole (QT). (b) True-tripole (TT).

II. Principles of Tripolar Cuff Electrode Recording

The ENG signal results from the action potentials propagating along the nerve fibers, which cause small action currents to flow through the fiber membranes into the extrafascicular medium [5]. Confinement within an insulating cuff causes the local impedance to be higher than outside the cuff, so that the action currents give rise to measurable potentials between the cuff electrodes. Simply stated, the nerve is an insulator, while the space between the nerve bundle and the cuff is filled with connective tissue and/or conducting fluid.

A very important function of the cuff is that, as a uniform insulating tube, any externally applied potential differences between the ends will produce a linear gradient inside [8]. This *linearization* effect is depicted in Fig. 1 in the basic electrical lumped-impedance model of the cuff [6], [12]. In this model, Z_{t1} and Z_{t2} represent the tissue impedances inside the cuff, Z_{t0} is the tissue impedance outside the cuff, Z_{e1}, Z_{e2}, and Z_{e3} are the electrode–tissue contact impedances, $i_{\mathrm{EMG}}(t)$ is the interfering EMG current that flows inside the cuff, and $v_{\mathrm{ENG}}(t)$ is the ENG voltage. At the frequencies of interest, the impedances may be regarded as purely resistive with typical values listed in the caption of Fig. 1. The EMG potentials across nodes *ab* and *cb* in Fig. 1 appear as anti-phase while the respective ENG potentials appear in-phase. Given the linear gradient of the EMG potential inside the cuff and equally spaced tripolar electrodes, the residual EMG at the output from either the QT or TT amplifier configurations (Fig. 2) will ideally be zero. However, in practice Z_{t1} and Z_{t2} are subject to uneven variations which destroy the tripolar cuff symmetry, resulting in *cuff imbalance*, defined as

$$X_{\mathrm{imb}} = \left(\frac{Z_{t1} - Z_{t2}}{Z_{t1} + Z_{t2}}\right) \times 100\%, \quad X_{\mathrm{imb}} < 100\%. \tag{1}$$

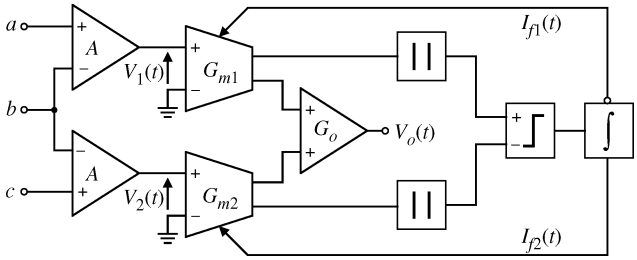

Fig. 3. Adaptive-tripole (AT) architecture.

The two main reasons for the variations in Z_{t1} and Z_{t2} are inhomogeneous tissue growth inside the cuff after implantation and manufacturing tolerances in positioning of the electrodes [10]. Secondary reasons affecting cuff imbalance include the position of the EMG source relative to the cuff [13]. Although the ENG signal recorded with the TT is about twice that recorded with the QT, the TT is much more sensitive to mismatch in Z_{t1} and Z_{t2} than the QT. On the other hand, the QT, unlike the TT, is very sensitive to mismatches in Z_{e1}, Z_{e2} and Z_{e3}. In the case of the TT, assuming unity gain for the output amplifier ($G_o = 1$), the residual EMG at its output is [14]

$$V_{o(\mathrm{EMG})} = i_{\mathrm{EMG}}(t)\left[\frac{Z_{t0}(G_1 Z_{t1} - G_2 Z_{t2})}{Z_{t0} + Z_{t1} + Z_{t2}}\right] \tag{2}$$

where G_1 and G_2 are the gains of the input differential amplifiers in Fig. 2(b). However, note that the term on the right-hand side of (2) can be made zero by *adjusting* G_1 and G_2 to compensate for any mismatch between Z_{t1} and Z_{t2} (this approach cannot be used with the QT). An automatic adjustment of the two amplifier gains is realized by the AT, which is described in Section III.

III. Adaptive Tripole Architecture

A. System Description

The block diagram of the AT implementation described in this paper is shown in Fig. 3. The system consists of two voltage preamplifiers, each with a fixed gain A, providing a very low-noise interface with the cuff electrodes. The preamplifiers are followed by two operational transconductance amplifiers (OTAs) with variable gains G_{m1} and G_{m2}, controlled by the differential feedback currents $I_{f1}(t)$ and $I_{f2}(t)$. The control stage operates by first obtaining the *moduli* of the currents at the output of the variable-gain OTAs and applying them to a current comparator to establish which is the largest. The comparator voltage output is subsequently applied to a large time-constant integrator which generates $I_{f1}(t)$ and $I_{f2}(t)$. The variable-gain OTAs counterbalance the presence of cuff imbalance, ideally by equalizing the amplitudes of the EMG signals at their outputs. As a result, when the output signals of the OTAs are summed at the input of the output-stage amplifier (gain G_o), the equal and anti-phase EMG signals from the two channels are cancelled, and the in-phase ENG signals are added and further amplified.

B. Sensitivity to Phase Errors

The AT achieves optimum artifact reduction when the EMG terms at the inputs of the output-stage amplifier (Fig. 3) are

exactly anti-phase. However, the use of ac coupling[2] in the preamplifiers for dc offset cancellation (see Section IV-A) will, in the case of mismatched filters, introduce additional phase shifts between the composite signals $V_1(t)$ and $V_2(t)$ in Fig. 3. The phase shifts will be more pronounced on the EMG as its frequency spectrum peaks at much lower frequencies than the ENG [6]. Even if there is some phase shift between the ENG terms of $V_1(t)$ and $V_2(t)$, it will still be possible to detect neural activity in the relevant nerve bundles.

Based on the above, it is desirable to establish the maximum tolerable phase mismatch between two first-order RC high-pass filters to achieve an output SIR of no less than unity. Assuming sinusoidal signals and a phase shift $\pi + \phi$ between the EMG term in $V_2(t)$ relative to that in $V_1(t)$, then with reference to the cuff model in Fig. 1 and for $Z_{t1} > Z_{t2}$, $V_1(t)$ and $V_2(t)$ are given by

$$V_1(t) = A\left[\frac{(1+X_{\rm imb})}{2}V_{\rm EMG}\sin(\omega_1 t) + V_{\rm ENG}\sin(\omega_2 t)\right] \quad (3)$$

$$V_2(t) = A\left[\frac{-(1-X_{\rm imb})}{2}V_{\rm EMG}\sin(\omega_1 t+\phi) + V_{\rm ENG}\sin(\omega_2 t)\right] \quad (4)$$

where $V_{\rm ENG}$ and $V_{\rm EMG}$ are the voltage amplitudes of $v_{\rm ENG}(t)$ and $i_{\rm EMG}(t)[Z_{t0}(Z_{t1}+Z_{t2})/(Z_{t0}+Z_{t1}+Z_{t2})]$ in Fig. 1, respectively, and ω_1 and ω_2 their respective frequencies. Furthermore, assuming that $I_{f1}(t)$ and $I_{f2}(t)$ in Fig. 3 have settled to their final values for a given $X_{\rm imb}$, such that

$$\begin{aligned} G_{m1} &= G_{mo}(1-X_{\rm imb}) \\ G_{m2} &= G_{mo}(1+X_{\rm imb}) \end{aligned} \quad (5)$$

where G_{mo} is the mean gain of each variable-gain OTA, the AT output is given by

$$V_o(t) = AG_{mo}G_o\left[\frac{(1-X_{\rm imb}^2)}{2}V_{\rm EMG}[\sin(\omega_1 t)-\sin(\omega_1 t+\phi)] + 2V_{\rm ENG}\sin(\omega_2 t)\right] \quad (6)$$

which using standard trigonometric identities modifies to

$$V_o(t) = AG_{mo}G_o\left[\frac{(1-X_{\rm imb}^2)}{2}V_{\rm EMG}\sqrt{2-2\cos(\phi)} \times \cos(\omega_1 t-\theta) + 2V_{\rm ENG}\sin(\omega_2 t)\right] \quad (7)$$

where $\theta = \tan^{-1}[(\cos(\phi)-1)/\sin(\phi)]$ is the phase shift of the residual output EMG relative to the input EMG (i.e., seen at the electrodes). Thus, if $\phi = 0$, the AT will (ideally) eliminate EMG. However, if $\phi \neq 0$, the amplitude of the residual output EMG will depend on ϕ. From (7), the output SIR can be defined as

$$\mathrm{SIR}_{\rm out} = \frac{4V_{\rm ENG}}{(1-X_{\rm imb}^2)V_{\rm EMG}\sqrt{2-2\cos(\phi)}}. \quad (8)$$

Thus, ϕ in radians can be calculated by

$$\phi = \pm\cos^{-1}\left[1 - 8\left(\frac{\mathrm{SIR}_{\rm in}/\mathrm{SIR}_{\rm out}}{(1-X_{\rm imb}^2)}\right)^2\right] \quad (9)$$

where $\mathrm{SIR}_{\rm in} = V_{\rm ENG}/V_{\rm EMG}$. For example, if $\mathrm{SIR}_{\rm out} = 1$, $\mathrm{SIR}_{\rm in} = 1/500$, and $X_{\rm imb} = \pm 40\%$, then $\phi = \pm 0.55°$. This can be converted to an error term ε for the maximum tolerable component mismatch of two first-order RC high-pass filters. Since the ENG does not exhibit very low-frequency components, a low-end ENG amplifier bandwidth of 100 Hz is usually realized [6]. The worst case ε for a cut-off frequency of 100 Hz is when the EMG frequency is also 100 Hz, giving $\varepsilon = 1.89\%$ between the two RC product values. It should be noted that although a mismatch between the -3-dB frequency of the two filters will also introduce magnitude errors, these will be seen by the control stage of the AT as cuff imbalance and corrected.

IV. Circuit Design

A. Low-Noise Preamplifiers

The preamplifiers, being the front-end interface with the cuff electrodes, are required to exhibit very low-noise performance and have reasonable voltage gain (about 40 dB), so that low noise is not a concern for the design of the subsequent system stages. The exact gain of the preamplifiers is not important because any gain mismatch between them will be compensated for by the control stage of the AT. Thus, a simple feedforward architecture was employed as depicted in Fig. 4, thereby avoiding the complexity and noise of feedback networks. Noise optimization of the preamplifiers was explicitly described in [16], where it was shown that in order to achieve the required noise specification with minimum die area and power dissipation, the input differential pair transistors $Q1$ and $Q2$ in Fig. 4 should be bipolar. Because of this requirement, the complete adaptive ENG amplifier was implemented in BiCMOS technology, although the control stage utilizes MOS transistors only.

The preamplifier circuit in Fig. 4 consists of a simple BiCMOS OTA ($Q1$, $Q2$, $M1$, and $M2$) terminated in the load resistor R_1 (40 kΩ, V_{ref} is a dc voltage source of 0.75 V), followed by a first-order bandpass filter, which restricts the bandwidth to about 100 Hz–10 kHz. The upper cut-off frequency is obtained by the combination of resistor R_2 (500 kΩ) and capacitor C_1 (27 pF), while the lower cut-off frequency is obtained by capacitor C_2 (80 pF) with the series combination of transistors $M6$ and $M7$, the latter transistor pair forming a high value (20 MΩ) grounded linear *active* resistor. In addition to eliminating low frequencies below the ENG passband, the high-pass section of the bandpass filter also removes some of the low-frequency flicker ($1/f$) noise voltage tail and ensures a dc offset-free preamplifier output. The ac coupling mechanism

[2]In an implantable ENG amplifier, ac coupling realized by RC high-pass filters is also included in series with the cuff electrodes to prevent dc currents flowing through the tissue which would cause electrolysis, and to cancel dc offsets stemming from the electrodes [15]. However, since passive components are usually used for such filters, their cut-off frequency can be made extremely low, thereby minimizing the possibility of phase shifts.

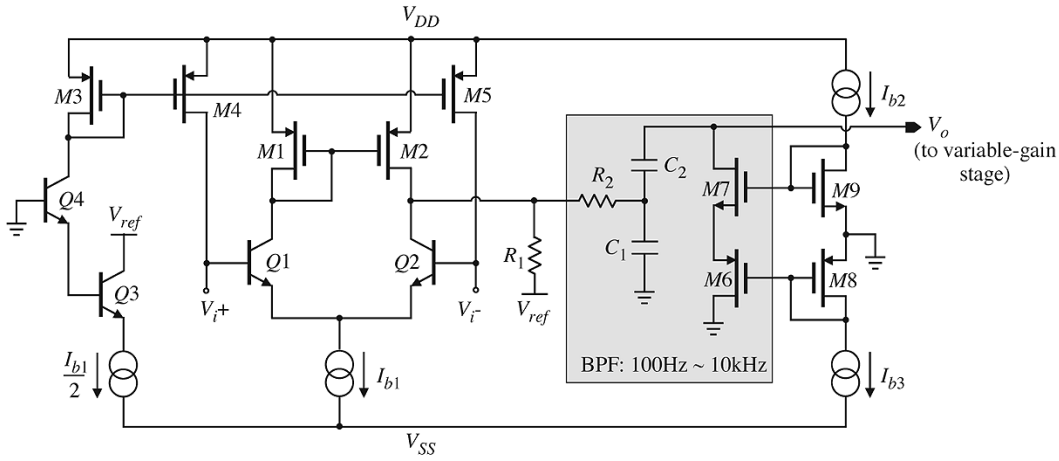

Fig. 4. Preamplifier circuit.

is very important since the succeeding variable-gain OTAs are driven single-ended, and thus, the presence of dc offset voltages (>1 mV) at their inputs would severely degrade the output SIR. By appropriate scaling of the aspect ratios of *M*6 and *M*7, a high value resistance is obtained with a maximum nonlinearity of 0.25% for a signal swing of ±85 mV. The dc bias voltages of *M*6 and *M*7 are provided by the diode-connected transistors *M*8 and *M*9, respectively, which are in turn biased by the dc current sources I_{b2} and I_{b3}.

As the base current of *Q*1 and *Q*2 cannot be supplied by the input interface, this was generated on-chip as shown in Fig. 4. Essentially, *Q*3 generates a replica of the base currents of *Q*1 and *Q*2, which is fed into the pMOS current mirror *M*3–*M*5 whose outputs feed the bases of *Q*1 and *Q*2, respectively. The base of *Q*4 is connected to ground to ensure that the emitter voltage of *Q*3 is at the appropriate level. Furthermore, the collector of *Q*3 is connected to V_{ref} to mimic as far as possible the dc conditions of *Q*1 and *Q*2 (the residual input dc base current is about 30 nA). The area of *M*4 and *M*5 were carefully chosen so that for an 800-nA drain current, their noise contribution is negligible. The bias currents for the OTA and the base current reduction circuits are provided by the dc current sources I_{b1}. The value of I_{b1} was appropriately selected so that the input-referred r.m.s. noise voltage of the preamplifier is 290 nV (noise bandwidth of 1 Hz–15 kHz). Both preamplifiers share the same current reduction and biasing circuits.

It should be noted that the preamplifiers could also be realized in CMOS technology by using the available paracitic lateral bipolar transistors. However, due to the poor matching of such devices, a larger die area and greater power dissipation would be required to meet the noise specification.

B. Variable-Gain OTAs

The composite signal at the input to each AT channel consists of EMG and ENG components with nominal peak–peak swing after preamplification of around ±50 mV (for $X_{\text{imb}} = 0$) and ±100 μV, respectively. The control stage is required to have sufficient gain to amplify the ENG to a reasonable amplitude (i.e., ±20 mV) and also sufficient linearity to accommodate the EMG

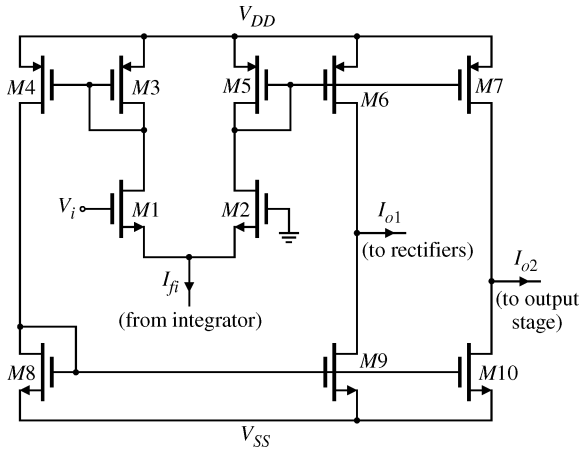

Fig. 5. Variable-gain OTA circuit.

signal. The decision to use an OTA to implement each variable-gain stage was based on the following two reasons: 1) using an OTA, variable-gain capability can be very simply achieved by changing its tail current, and 2) the output current signal from an OTA simplifies the design of the subsequent full-wave rectifiers and current comparator circuits. The basic requirement is that each variable-gain OTA must have enough linear gain range to allow even for extreme $X_{\text{imb}} = \pm 40\%$ as suggested in [13].

Although the nominal signal swing after preamplification with $X_{\text{imb}} = \pm 40\%$ is expected to be about ±70 mV, the linear input range of each variable-gain OTA was set to ±85 mV to allow for some variation in the nominal EMG amplitude picked-up from the cuff electrodes. The variable-gain OTA was designed for operation in strong inversion and its simplified schematic is shown in Fig. 5. The circuit essentially consists of a symmetrical simple CMOS OTA (input transistors *M*1 and *M*2) with current mirrors *M*3–*M*10 of unity current ratio which in practice were regulated cascodes [17]. The gain of the OTA is controlled by the feedback current I_{fi}, and the circuit has two current outputs, I_{o1} and I_{o2}, each connecting to the input of a full-wave rectifier or to the input of the output-stage amplifier.

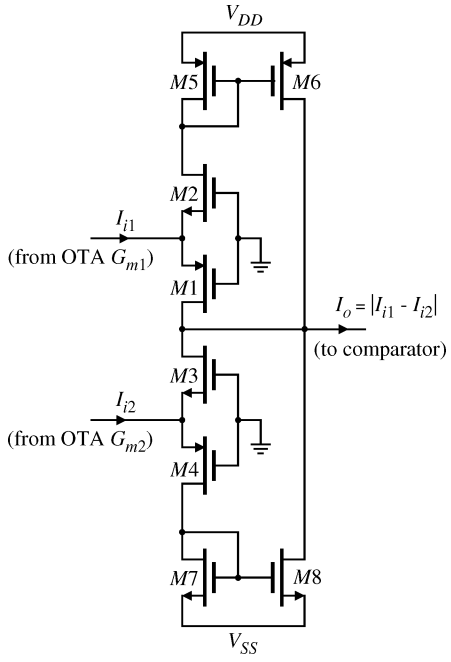

Fig. 6. Two full-wave rectifier circuits.

Assuming matched transistors and neglecting channel length modulation, each output current of the OTA in Fig. 5 is given by [18]

$$I_o = \sqrt{2I_{fi}k}V_i\sqrt{1-\frac{k}{2I_f}V_i^2}, \qquad |V_i| \le \sqrt{\frac{I_{fi}}{k}} \tag{10}$$

where V_i is the input voltage, $k = \mu C_{\rm ox}(W/2L)$ is the transconductance parameter, W and L are the channel width and length of the input transistors, μ is the carrier mobility, and $C_{\rm ox}$ is the gate oxide capacitance per unit area. The relationship between transconductance G_m and V_i can be obtained by taking the derivative of (10) with respect to V_i, yielding

$$G_m = \frac{\sqrt{2I_{fi}k}\left(1-(kV_i^2/I_{fi})\right)}{\sqrt{1-(kV_i^2/2I_{fi})}}. \tag{11}$$

For $V_i \ll \sqrt{I_{fi}/2k}$, the OTA transconductance simplifies to

$$\begin{aligned} G_m &= g_{m1,2} = \sqrt{2kI_{fi}} \\ &= \sqrt{2kI_{fo}(1\pm 2X_{\rm imb})} \approx G_{mo}(1\pm X_{\rm imb}) \end{aligned} \tag{12}$$

where $g_{m1,2}$ is the small-signal transconductance of transistors *M*1 and *M*2 in Fig. 5 and I_{fo} is the mean (dc) value of I_{fi}. Furthermore, in order to maintain less than 1% nonlinearity, it is required that

$$|V_i| \le 0.2\sqrt{\frac{I_{fi}}{k}}. \tag{13}$$

Given the nature of the signals after preamplification as discussed and aiming for an output-stage transimpedance gain of about 500 kΩ, a mean value for G_m of 185 μA/V was chosen. Thus, for $V_i = \pm 85$ mV, (12) and (13) can be solved for suitable values of k and I_{fi}.

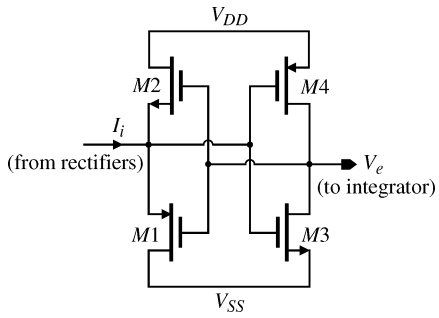

Fig. 7. Comparator circuit.

C. Full-Wave Current Rectifiers

The two full-wave rectifiers shown in Fig. 3 were realized by the current-mode circuit in Fig. 6. The upper rectifier (*M*1, *M*2, *M*5, *M*6) operates on current I_{i1} stemming from OTA G_{m1}, while the lower rectifier (*M*3, *M*4, *M*7, *M*8) operates on current I_{i2} stemming from OTA G_{m2}. The core of each current rectifier are the complementary transistors *M*1, *M*2 (upper rectifier) and *M*3, *M*4 (lower rectifier), each transistor performing half-wave precision current rectification [19]. During positive excursions of I_{i1} and I_{i2}, *M*1 and *M*4 are turned on and *M*2 and *M*3 are turned off. Thus, the drain currents of *M*1 and *M*4 equal I_{i1} and I_{i2}, respectively, while that of *M*2 and *M*3 are zero. During negative excursions of I_{i1} and I_{i2}, *M*2 and *M*3 are turned on and *M*1 and *M*4 are turned off. In this mode the drain currents of *M*2 and *M*3 equal I_{i1} and I_{i2}, respectively, while that of *M*1 and *M*4 are zero. For the upper rectifier, full-wave rectification is obtained by mirroring the drain current of *M*2 through the unity-gain pMOS current mirror *M*5, *M*6 and adding the mirror output to the drain current of *M*1. Similarly for the lower rectifier, full-wave rectification is obtained by mirroring the drain current of *M*4 through the unity-gain nMOS current mirror *M*7, *M*8 and adding the mirror output to the drain current of *M*3. In practice both current mirrors were realized by regulated cascodes [17]. The addition of the various drain currents is done at the input node of the current comparator, resulting in the output current $I_o = |I_{i1} - I_{i2}|$ as indicated in Fig. 6. Although a considerable voltage drop of about 2 V is generated at the input node of each rectifier, the use of regulated cascode mirrors with long transistors in the variable-gain OTAs, ensures that I_{i1} and I_{i2} are not degraded by channel length modulation.

D. Current Comparator

The output currents from the two full-wave rectifiers are summed at the input of the current comparator circuit [20] shown in Fig. 7 to form current I_i. The comparator uses a CMOS inverter (*M*3, *M*4) to apply negative feedback around a class-B voltage buffer (*M*1, *M*2). As a result of the feedback, the comparator input has a low-impedance (in general) and is thus ideal for determining the polarity of I_i. On the other hand, the output of the inverter does not swing between the power supplies and so some static power dissipation is present. Fortunately, since in this application low-speed operation is required, the inverter transistors can be scaled to minimize power dissipation. The buffer transistors have zero dc power dissipation.

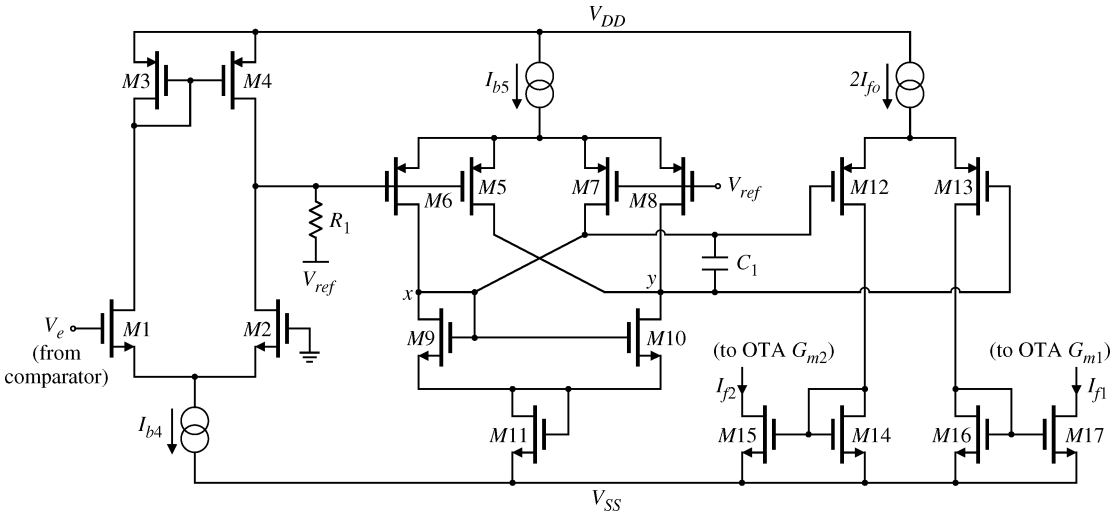

Fig. 8. Large time-constant integrator circuit.

E. Large Time-Constant Integrator

Because of the nature of cuff imbalance variations as discussed in Section II, the integrator time-constant should be as large as possible. System level simulations have shown that a time-constant of about 1 s is required for this application. The integrator schematic is shown in Fig. 8. The circuit comprises three stages. The first stage, consisting of the simple CMOS OTA (*M*1–*M*4) terminated in resistor R_1 (2 kΩ), is essentially an attenuator which also corrects amplitude variations between the comparator peak-positive and peak-negative output voltages. This is very important since significant comparator output offsets would affect the settling time and $\mathrm{SIR}_{\mathrm{out}}$ of the AT differently for positive and negative X_{imb} values. The second stage is the actual OTA-C integrator (operated in weak inversion), and this consists of a CMOS OTA (*M*5–*M*11) utilizing transconductance cancellation [21], and an integrating capacitor C_1 (47.5 pF) which is connected across the low and high impedance nodes x and y, respectively. The attenuation provided by the first stage ensures that the input voltage to the second-stage OTA is within its linear range of operation. The second-stage OTA is biased to achieve a transconductance G_{mc} of 6.9 nA/V given by $g_{m6,8} \times [(n-1)/(n+1)]$, where $g_{m6,8}$ is the small-signal transconductance of *M*6 and *M*8, and n is the ratio of the transconductance of *M*6 to *M*5 (or *M*8 to *M*7). Transistor *M*11 performs level-shifting of the output voltage for interfacing with the third stage.

The third stage (*M*12 – *M*17) is another transconductance stage converting the voltages across C_1 to the differential feedback currents I_{f1} and I_{f2}. The tail currents of the three integrator stages are provided by the dc current sources I_{b4}, I_{b5} and $2I_{fo}$. The OTA-C stage, being *lossy*, has the following transfer function:

$$T(s) = \frac{G_{mc}}{s2C_1 + g_o} \tag{15}$$

where s is the Laplace operator, and g_o is the small-signal output conductance seen into node y. The integrator time-constant is $2C_1/g_o$ and g_o is set by I_{b5}. Any possible dc offset voltages across nodes x and y resulting from transistor mismatches may be externally corrected by adjusting the dc voltage level of R_1 (e.g., by means of current injection). The dc voltage source V_{ref} is the same as in Fig. 4 and the simulated dc gain G_{mc}/g_o of the OTA-C stage is about 73. The integrator described here offers a simpler implementation than the design in [22], both addressing the same application.

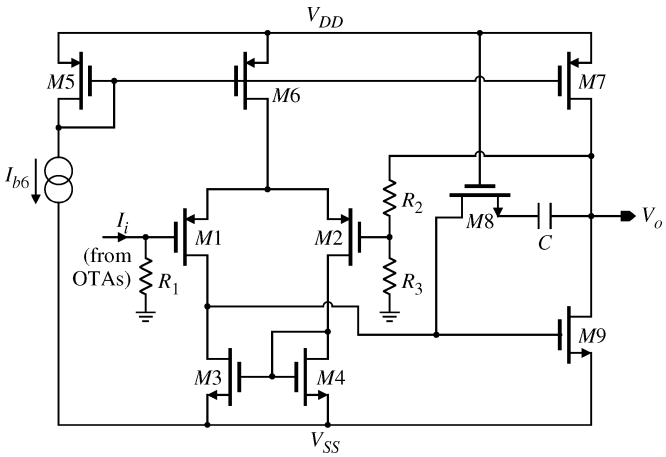

Fig. 9. Output-stage amplifier circuit.

F. Output-Stage Amplifier

The schematic of the output stage amplifier is shown in Fig. 9. The second output branch from each variable-gain OTA (Fig. 5) is hardwired to resistor R_1 (50 kΩ) where the two composite currents I_{i1} and I_{i2} are summed up to form I_i. Due to the corrective action of the control stage, the two EMG components in I_{i1} and I_{i2} are ideally of the same amplitude, and, being anti-phase, when added are cancelled out. On the other hand, the ENG components in I_{i1} and I_{i2} being in-phase, when added a voltage is generated across R_1 which is further amplified. The amplifier (*M*1–*M*9) in Fig. 9 is a standard two-stage op-amp configured as a noninverting amplifier through the feedback resistive network R_2 (90 kΩ) and R_3 (10 kΩ). The amplifier employs zero-pole compensation realized by the series combination of transistor *M*8 and capacitor C_1 (3.5 pF), and the circuit is biased

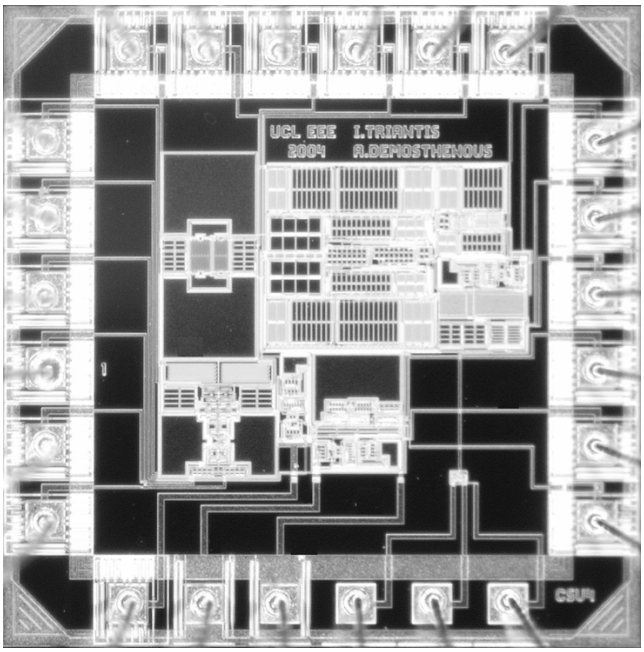

Fig. 10. Chip microphotograph.

TABLE I
MOS TRANSISTOR DIMENSIONS

Circuit	Transistor Label	*W/L* (μm/μm)
Preamplifier (Fig. 4)	*M*1, *M*2	150/10
	*M*3 – *M*5	20/10
	*M*6	2/519
	*M*7	2/371
	*M*8	7/7
	*M*9	5/8
Variable-gain OTA (Fig. 5)	*M*1, *M*2	150/30
Rectifiers (Fig. 6)	*M*1, *M*4	200/0.8
	*M*2, *M*3	80/0.8
Comparator (Fig. 7)	*M*1, *M*4	5/2
	*M*2, *M*3	2/2
Integrator (Fig. 8)	*M*5, *M*7	10/10
	*M*6, *M*8	10/9
	*M*9, *M*10	25/50
	*M*11	2/30
	*M*12, *M*13	200/5

by the dc current source I_{b6}. The simulated open-loop gain of the op-amp is 106 dB, and the input-referred r.m.s. noise current of the complete trasimpedance stage is about 100 pA (bandwidth of 1 Hz–15 kHz).

V. MEASURED RESULTS

The adaptive ENG amplifier chip, shown in Fig. 10, was fabricated in the austriamicrosystems 0.8-μm BiCMOS process [23] which includes a high resistive layer. A second chip containing the control stage configured as test structures was also fabricated. The substrates of all transistors were connected to their respective power supply rail (i.e., nMOS to V_{SS} and pMOS to V_{DD}), and the dc bias current sources I_{b1} (150 μA), I_{b2} (10 μA), I_{b3} (10 μA), I_{b4} (2 μA), I_{b5} (10 nA), $2I_{fo}$ (200 μA), and I_{b6} (50 μA), in Figs. 4, 8, and 9, were realized by an on-chip biasing circuitry (not described). Some of the key MOS transistor dimensions are listed in Table I. In total, 40 chips were fabricated (20 test structures and 20 complete systems); all showed correct operation.

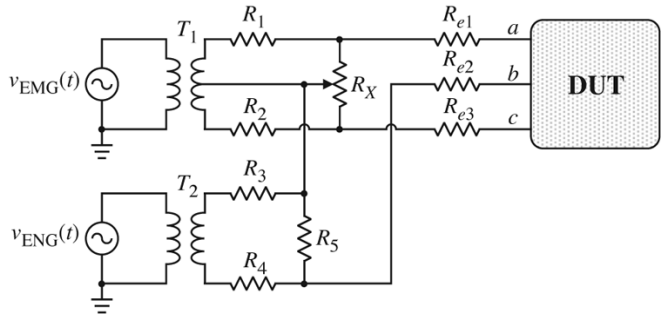

Fig. 11. Experimental setup.

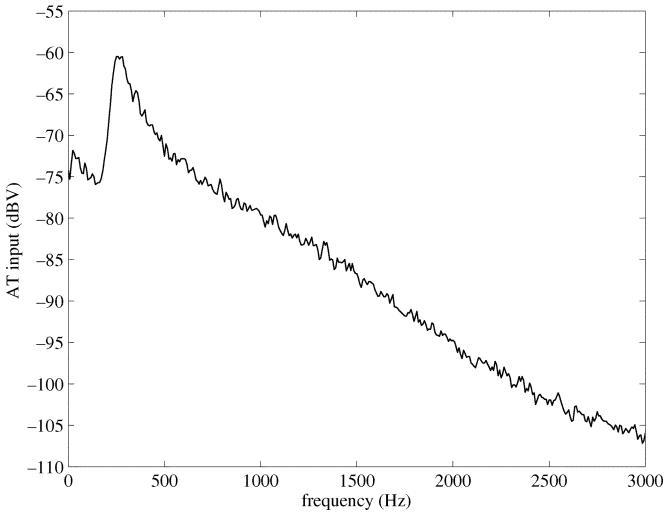

Fig. 12. Frequency spectrum of the composite input signal. The spectrum of the band-limited white noise signal representing the EMG resembles that of the real EMG.

The input ac signals to the AT chip (DUT) were provided by two audio transformers T_1 and T_2 (A262A7E) as illustrated in Fig. 11. The ac voltage sources, $v_{\rm EMG}(t)$ and $v_{\rm ENG}(t)$, generate the EMG and ENG signals, respectively, resistors R_1, R_2, R_3, R_4, R_5, and R_X provide attenuation, and the variable resistor R_X also generates amplitude imbalance (modeling $X_{\rm imb}$) between the EMG terms of the two composite signals across nodes *ab* and *cb*. Furthermore, resistors $R_{e1,2,3}$ represent the electrode resistances. Initially, the chips were tested with sinusoidal signals, $v_{\rm EMG}(t)$ (100 Hz) and $v_{\rm ENG}(t)$ (1 kHz), with nominal peak amplitudes across nodes *ab* (and *bc*) in Fig. 11 of $V_{\rm EMG} = 0.5$ mV and $V_{\rm EMG} = 1$ μV, respectively. Subsequently, in order to model a more realistic test, $v_{\rm EMG}(t)$ was replaced by an arbitrary signal (generated from band-limited Gaussian noise) with the frequency spectrum plotted in Fig. 12 (measured across *ac*). The frequency content of this signal varies between 1 Hz and 3 kHz, with a peak at approximately 250 Hz, which is the case with the real EMG signal [6]. The $v_{\rm ENG}(t)$ was kept in all measurements as a sinusoid with the characteristics mentioned above. In Fig. 12, the ENG magnitude (−114 dB) is buried under the spectrum floor of the random EMG signal.

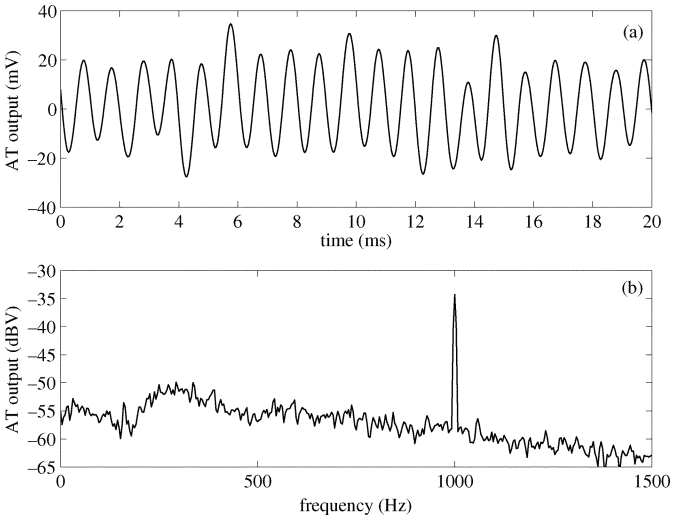

Fig. 13. System output for +20% imbalance. (a) Time-domain. (b) Frequency-domain.

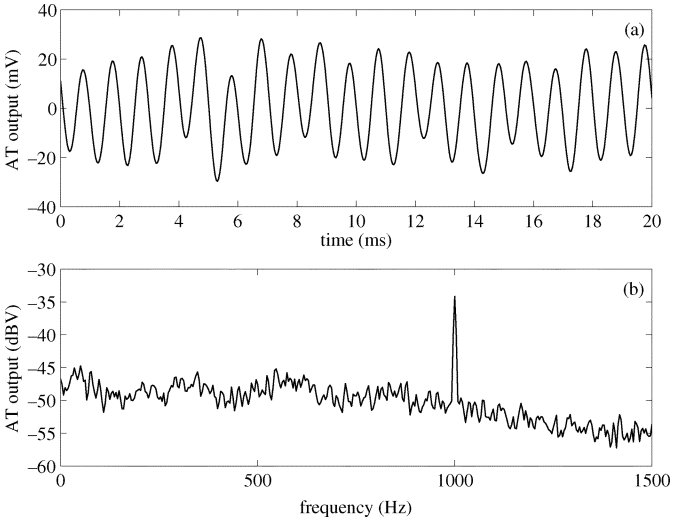

Fig. 14. System output for −40% imbalance. (a) Time-domain. (b) Frequency-domain.

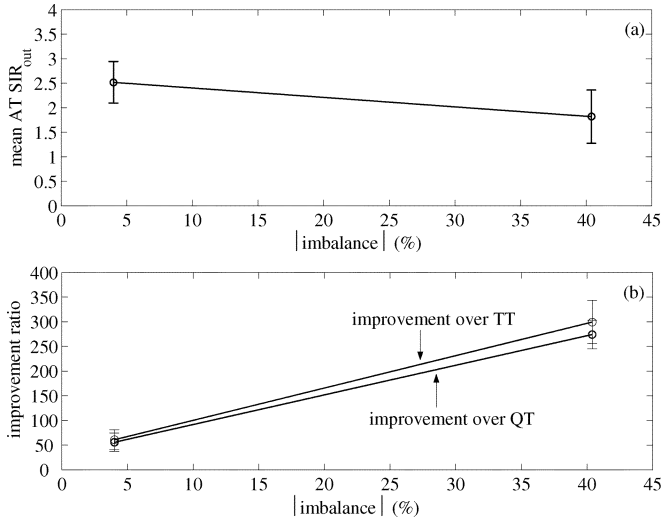

Fig. 15. (a) Mean AT $\mathrm{SIR}_{\mathrm{out}}$ versus (absolute) imbalance for all 20 chips. (b) $\mathrm{SIR}_{\mathrm{out}}$ improvement over the ideal TT and QT counterparts versus (absolute) imbalance.

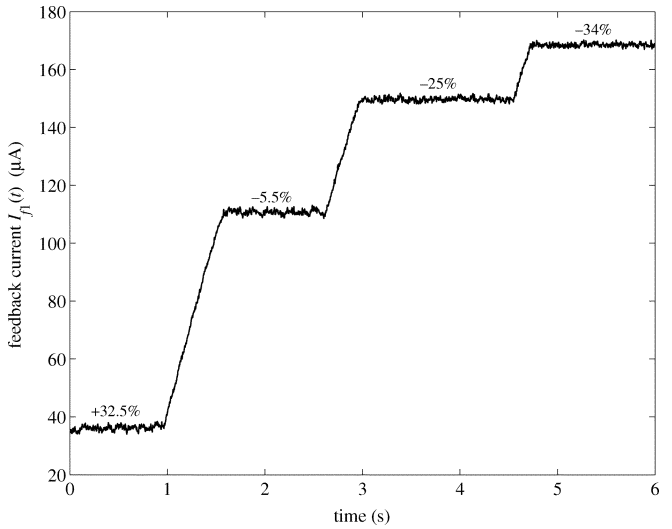

Fig. 16. Settling time of feedback current $I_{f1}(t)$ for abrupt changes in imbalance.

The time-domain tests were monitored on an Agilent 54835A Infiniium™ oscilloscope, and the frequency-domain tests on a Stanford Research Systems SR760 FFT spectrum analyzer.

Figs. 13 and 14 show the time-domain and frequency-domain outputs of the AT (after settling) for +20% and −40% imbalance, respectively. The spectra show that the $\mathrm{SIR}_{\mathrm{out}}$ is better than 3 (9.54 dB) even for 40% imbalance. This should be compared with a $\mathrm{SIR}_{\mathrm{in}}$ of 1/500 (−54 dB). These results show the superiority of the AT relative to any filtering technique because its operation is not frequency related. The average $\mathrm{SIR}_{\mathrm{out}}$ for all 20 (complete) AT chips as a function of imbalance is plotted in Fig. 15(a) (Matlab best linear-fit), where it can be seen that even for extreme values of imbalance, the mean AT $\mathrm{SIR}_{\mathrm{out}}$ is better than 2 (6 dB). The error bars in the plot indicate the spread of values from all 20 chips. For comparison, Fig. 15(b) shows the mean $\mathrm{SIR}_{\mathrm{out}}$ improvement over the theoretical TT and QT amplifier configurations as a function of imbalance (for the TT the input amplifiers were assumed to be matched, and for the QT the electrode impedance values listed in the caption of Fig. 1 were assumed). From the plot, it is apparent that the AT significantly outperforms both counterparts in the presence of imbalance. Fig. 16 shows the settling time of the feedback current $I_{f1}(t)$ in Fig. 3 for abrupt step-like changes in imbalance. The imbalance was changed successively between +32.5%, −5.5%, −25%, and −34%. The corresponding settling time (to 1%) is about 20 ms per percent change in X_{imb}.

Finally, in order to test the sensitivity of the AT architecture to phase variations, phase shifts were introduced between the two input EMG terms to the system (the additional test structure chip was used for this test). Fig. 17 shows the $\mathrm{SIR}_{\mathrm{out}}$ as a function of phase shift for both measured and theoretical cases, the latter calculated from (9) and for 40% imbalance. The two graphs show excellent agreement, but for phase values near the origin, the theoretical $\mathrm{SIR}_{\mathrm{out}}$ tends to infinity, which would never be the case for a practical realization. Saline-bath testing of the AT chip (not described here) also confirmed its high performance. The main design features of the AT chip are summarized in Table II.

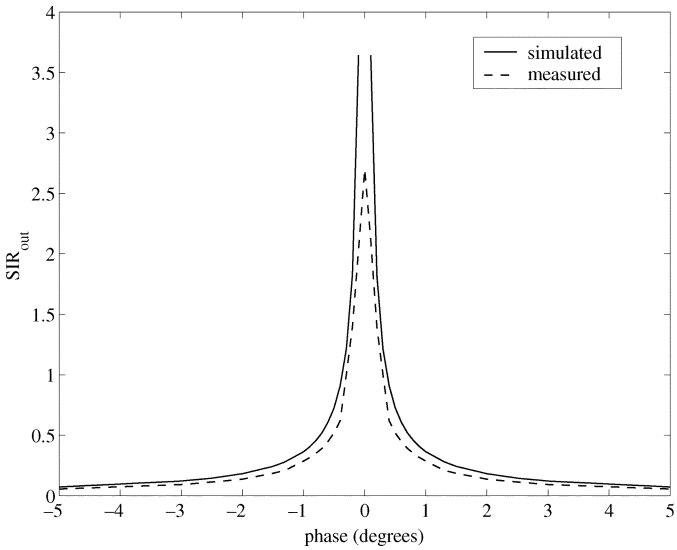

Fig. 17. Sensitivity of AT $\mathrm{SIR_{out}}$ to phase shifts.

TABLE II
SUMMARY OF PERFORMANCE

Parameter	Value
Technology	0.8 µm BiCMOS
Power supply	± 2.5 V
Power consumption	7.2 mW
Active area (core)	0.68 mm^2
$\mathrm{SIR_{out}}$	> 6dB
Imbalance correction range	> ± 40%
Total ENG path gain	87dB
Setting time (step-change)	
± 20 % imbalance	480 ms
± 40 % imbalance	960 ms

VI. CONCLUSION

The design of an adaptive ENG amplifier for interface to tripolar cuff electrodes has been described. The adaptive ENG amplifier offers a fully implantable solution to the problem of cuff imbalance, thereby significantly advancing the state-of-the-art in the field. The described realization overcomes many of the limitations of a previous design in terms of reliability, cuff imbalance correction range, output SIR and output signal distortion. The operation of the circuit has been thoroughly verified by tests on 40 fabricated chip samples, all exhibiting correct behavior. Although the described adaptive ENG amplifier has been developed for a next-generation bladder implant, it can also be seen as a generic high-performance ENG amplifier for any functional electrical stimulation application employing tripolar nerve cuff electrodes.

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REFERENCES

[1] J. J. Struijk, M. Thomsen, J. O. Larsen, and T. Sinkjaer, "Cuff electrodes for long-term recording of natural sensory information," *IEEE Eng. Med. Biol. Mag.*, vol. 18, no. 3, pp. 91–98, May/Jun. 1999.

[2] T. Sinkjaer, M. K. Haugland, and J. Haase, "Natural neural sensing and artificial muscle control in man," *Exp. Brain Res.*, vol. 98, pp. 542–545, 1994.

[3] M. Haugland, A. Lickel, J. Haase, and T. Sinkjaer, "Control of FES thump force using slip information obtained from the cutaneous electroneurogram in quadriplegic man," *IEEE Trans. Rehab. Eng.*, vol. 7, no. 2, pp. 215–227, Jun. 1999.

[4] M. Hansen, M. Haugland, T. Sinkjaer, and N. Donaldson, "Real time foot drop correction using machine learning and natural sensors," *Neuromodulation*, vol. 5, pp. 41–43, Jan. 2002.

[5] R. Stein, C. Davis, A. Jhamanda, T. Mannard, and T. Nichols, "Principles underlying new methods for chronic neural recording," *Le J. Canadien des Sciences Neurologiques*, vol. 2, pp. 235–244, 1975.

[6] Z. M. Nikolić, D. B. Popović, R. B. Stein, and Z. Kenwell, "Instrumentation for ENG and EMG recordings in FES systems," *IEEE Trans. Biomed. Eng.*, vol. 41, no. 7, pp. 703–706, Jul. 1994.

[7] B. Upshaw and T. Sinkjaer, "Digital signal processing algorithms for the detection of afferent nerve activity recorded from cuff electrodes," *IEEE Trans. Rehab. Eng.*, vol. 6, no. 2, pp. 172–181, Jun. 1998.

[8] J. Struijk and M. Thomsen, "Tripolar nerve cuff recording: Stimulus artifact, EMG, and the recorded nerve signal," in *Proc. 17th Int. Conf. IEEE EMBS*, vol. 2, Montreal, Canada, 1995, pp. 1105–1106.

[9] C. Pflaum, R. R. Riso, and G. Wiesspeiner, "Performance of alternative amplifier configurations for tripolar nerve cuff recorded ENG," in *Proc. 18th Int. Conf. IEEE EMBS*, vol. 1, Amsterdam, The Netherlands, 1996, pp. 375–376.

[10] M. S. Rahal, "Optimization of nerve cuff electrode recordings for functional electrical stimulation applications," Ph.D. dissertation, University College London, London, U.K., 2000.

[11] I. F. Triantis, R. Rieger, J. Taylor, A. Demosthenous, and N. Donaldson, "A CMOS adaptive interference reduction system for nerve cuff recordings," in *Proc. 28th Eur. Solid-State Circuits Conf.*, Florence, Italy, 2002, pp. 113–116.

[12] M. Sahin and M. D. Durand, "An interface for nerve recording and stimulation with cuff electrodes," in *Proc. 19th Int. Conf. IEEE EMBS*, Chicago, IL, 1997, pp. 2004–2005.

[13] I. F. Triantis, A. Demosthenous, and N. Donaldson, "On cuff imbalance and tripolar ENG amplifier configurations," *IEEE Trans. Biomed. Eng.*, to be published.

[14] M. Rahal, J. Winter, J. Taylor, and N. Donaldson, "An improved configuration for the reduction of EMG in electrode cuff recordings: A theoretical approach," *IEEE Trans. Biomed. Eng.*, vol. 47, no. 9, pp. 1281–1284, Sep. 2000.

[15] K. Papathanasiou and T. L. Ehmann, "An implanatable CMOS signal conditioning system for recording nerve signals with cuff electrodes," in *Proc. ISCAS 2000*, vol. 5, Geneva, Switzerland, pp. 281–284.

[16] R. Rieger, J. Taylor, A. Demosthenous, N. Donaldson, and P. Langlois, "Design of a low-noise preamplifier for nerve cuff electrode recording," *IEEE J. Solid State Circuits*, vol. 38, no. 8, pp. 1373–1379, Aug. 2003.

[17] E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 289–298, Feb. 1990.

[18] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.*, vol. CAS-31, no. 10, pp. 891–894, Oct. 1984.

[19] Z. Wang, "Novel pseudo RMS current converter for sinusoidal signals using a CMOS precision current rectifier," *IEEE Trans. Instrum. Meas.*, vol. 39, no. 4, pp. 670–671, Aug. 1990.

[20] H. Träff, "Novel approach to high-speed CMOS current comparators," *Electron. Lett.*, vol. 28, pp. 310–312, Jan. 1992.

[21] P. Garde, "Transconductance cancellation for operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 12, no. 6, pp. 310–311, Jun. 1977.

[22] R. Rieger, A. Demosthenous, and J. Taylor, "A 230-nW 10-s time constant integrator for an adaptive nerve signal amplifier," *IEEE J. Solid State Circuits*, vol. 39, no. 11, pp. 1968–1975, Nov. 2004.

[23] "0.8 μm BiCMOS Process Parameters," AustriaMicroSystems (AMS) Int. AG, Doc. 9933008, 2.0 ed., 2001.

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