VLSI Implementation of Wireless Power and Data Transmission Circuits for Micro-Stimulator

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ABSTRACT

This paper presents the realization of the radio frequency (RF) power and data transmission for implantable micro-stimulators. This implantable device includes an internal RF front-end circuit, a control circuit, and a stimulator. A 2MHz AM modulated signal including the power and data necessary for the implantable device is received, and a stable DC voltage and digital data will be extracted to stimulate the neuromuscular stimulation. The stimulator is a current-source stimulator, which is capable to generate a wide range of stimulation waveforms and stimulation patterns for a nerve cuff electrode. In this paper, most of the integrated circuits for the implantable device have been proposed and verified by using Hspice according to the technology of TSMC 0.25 um CMOS process.

INTRODUCTION

Various implantable micro-stimulators have been designed for various clinical applications [1], such as cardiac pacemakers, cochlear implants, retinal prostheses, and functional neuromuscular stimulation (FNS) systems. For the implanted micro-stimulator system, the power is the major concern in the system design. Due to the lifetime limitation, the battery is not the optimal choice in the implanted device. In recent years, electromagnetic propagation through inductive coupling links is commonly used to deliver power and information to these implantable micro-stimulators. The approach can avoid the risk of causing infection and the problem of battery life. In general, an implantable stimulator must satisfy the following requirements: 1) long-life time, 2) high reliability, 3) small size, and 4) high degree of reprogrammability. Based on the considerations, we propose the prototyping design of an 8-channel implantable stimulator for different neuro-prosthesis applications. The digital part of the stimulator is implemented by field programmable gate array (FPGA), and the analog part is implemented with CMOS 0.25um technology and fabricated by TSMC. The latter occupies a silicon area smaller than 0.00638 mm^2 and produces very linear output current for stimulation. Besides, it generates a maximum current of 2.77 mA through 1kΩ load while the stimulation frequency is 20Hz and the stimulation current pulse width is 300us.The paper is organized as follows. In Section II, the whole stimulation system is introduced briefly. Circuit design and implementation of the stimulation system are described in detail in Section III. Section IV describes the simulation and test results. Finally, the conclusion is summarized in Section IV.

SYSTEM ARCHITECTURE

In the recent years, RF coupling is widely used in the design of implantable micro-stimulators [2]. The power and data are simultaneously coupled into implantable micro-simulators, and separated by way of the process of internal circuits. In such an implantable system, the designers must consider the efficiency of RF telemetry and the carrier frequency first. In general, a class-E power amplifier is employed in an external transmitter for a high efficiency transmission. On the other hand, the carrier frequency also must be well considered, because of power absorption by tissues and losses in the reflection on the tissue interfaces. Besides, high carrier frequency will produce extra heat, and this will cause injury to tissues of body. So most of carrier frequency used is usually below 20MHz in such a micro-system. In this study, the 2MHz will be chosen as carrier frequency. Fig. 1 shows the overall system block diagram of a micro-stimulator with wireless power and data transmission.

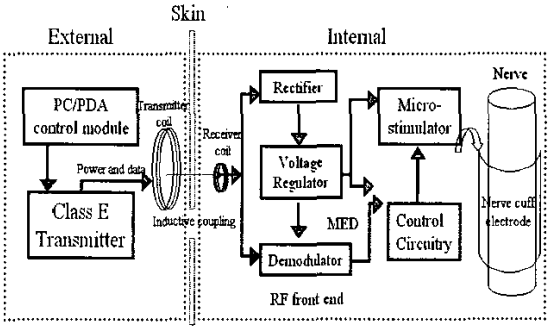

Figure 1. Block diagram of a micro-stimulator system.

The external unit includes a control module, a transmitter coil and a high efficient class-E power amplifier. It is responsible for the transmitting of power and data by way of the RF telemetry. The internal unit is an implantable device. It includes a receiver coil, a RF front-end circuit, a control circuit, and a micro-stimulator. Through the receiver coil and the RF front-end circuit, the power can be extracted to provide the supply voltage for the internal circuits and the demodulated data will be used to stimulate the nerve through micro-stimulator and nerve cuff electrode.

CIRCUIT DESCRIPTION

RF Front-End Circuit

The RF front-end circuit is responsible for the extraction of power and data. This circuit is the first stage to receive external RF signals. It consists of three main blocks, such as full-wave rectifier, voltage regulator, and demodulator. The voltage rectifier is made of two pairs of diodes and capacitors to compose a full-wave rectification circuit. The full wave rectifier receives an AM modulated 2 MHz signal and its output is a dc voltage with little ripple which provide the supply voltage for the following circuits. At the same time, RC circuits and transistors P1 and N1 detect the transition of input RF signal. Transistors P2 and N2 amplify and reverse the output of P1 and N1 [3]. The final output is the digital information carried by the external transmitting RF signal and restored by the demodulator. The circuit implementation is shown in Fig. 2.

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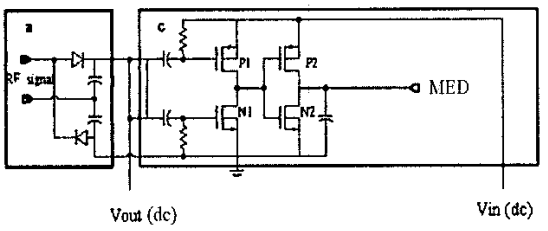

Figure 2. Circuit implementation of voltage rectifier and demodulator.

The voltage regulator provides a stable and precise 2.5V DC voltage source for the following implantable stimulator. Fig. 3 shows the architecture of the voltage regulator.

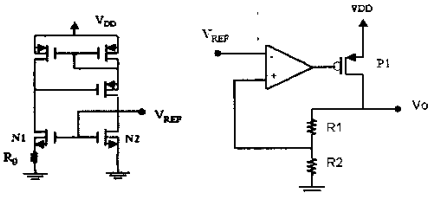

Figure 3. Architecture of voltage reference and voltage regulator.

In the voltage reference circuit, when each transistor is biased at its active mode, ignoring the channel-length modulation effect, the reference voltage can be described as

$$V_{REF} = V_T + 2(\sqrt{\beta_1} - \sqrt{\beta_2})/(R_0 \bullet \sqrt{\beta_1} \bullet \beta_2) \quad \text{.....(1)}$$

Where $\beta = \mu * Cox * W/L$ and V_T is the threshold voltage of NMOS transistor, μ is the carrier mobility, and Cox is the gate capacity per unit area. The voltage V_{REF} is the operational amplifier (op-amp) negative input. It can be controlled by way of the suitable adjusting the W/L of transistors N1 and N2. The transistor P1, which introduces 180° of phase difference and is the op-amp positive input, establishes the negative feedback. The positive and negative inputs of the op-amp are forced to be equal because of the existence of the negative feedback and very high dc gain of the op-amp. Therefore, the relational equation between V_O and V_{REF} can be built as follows:

$$V_O = V_{REF}(1+R_1/R_2) \quad \text{.....(2)}$$

Since the technology of TSMC 0.25 um CMOS process is used, the value of V_O is designed to be 2.5V dc level. Fig.4 is the schematic view of the voltage regulator.

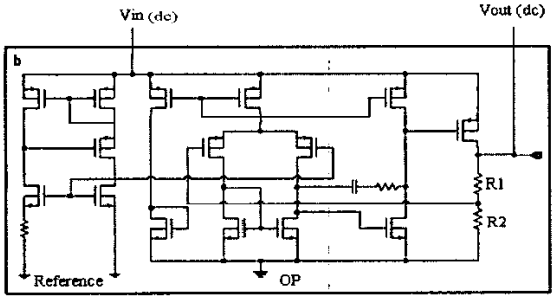

Figure 4. Circuit implementation of voltage regulator.

Control Circuit

Fig. 5 shows the functional blocks of the control circuit. It consists of three components: the Manchester decoder, the serial-to-parallel converter, and the finite state machine. These components are implemented by way of digital circuits. The main function of Manchester decoder is to decode the MED and to recuperate data and clock. The data extracted by Manchester decoder is in serial sequence, but the parallel-typed data is more convenient for later use. Therefore, a serial-to-parallel converter is used behind the Manchester decoder. In addition, the output data of the serial-to-parallel converter are used to control the micro-stimulator through the control center, finite state machine. In this design, eight different stimulation channels are employed for FNS. The object of the finite state machine is to determine the proper stimulation channel and the scale of stimulation current by using the previously decoded data. In other words, each time it will enable the selected current stimulator with a proper current.

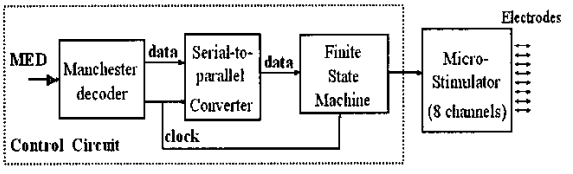

Figure 5. Functional blocks of the control circuit.

Micro-Stimulator

The current-source micro-stimulator is composed of eight stimulation channels. According to the direction from finite state machine, each channel could output constant current to the corresponding electrode. Since the unsuitable stimulation frequency and current pulse width would make muscle fatigue quickly, we have to carefully take them into account while we design the stimulation channel. In the general specification of FNS, the stimulation frequency is about 20 Hz and the stimulation current pulse width is about 300 μs . Hence, we adopt the specifications in the design. In addition, the typical impedance of nerve is 1 kΩ, so the proposed stimulation channel is designed to generate a maximum current of 3.5 mA through 1 kΩ load.

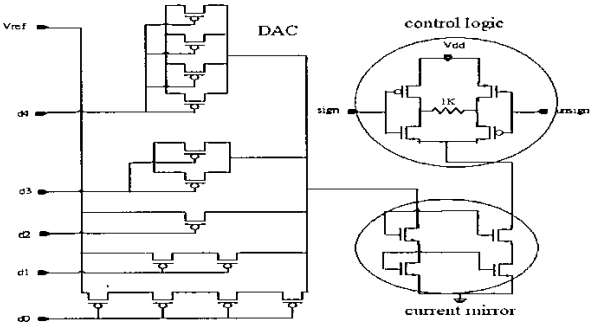

Figure 6. Circuit diagram of constant current source.

To maintain the stability and linearity of the output current is the main issue during analog VLSI design [4]. In our design, the current stimulation channel is composed of three components as shown in Fig.6, current-mode digital-to-analog converter (DAC), current mirror, and control logic. The output current of DAC can be varied in

32 different levels ranging from 0 to 3.5 mA, thus the difference of each level is about 108 uA. The reason of choosing 5-bit DAC is that we must concern with the sensitivity of nerve. The transistors in DAC are placed in parallel or in series to produce the programmable current. In order to maintain the linearity of output current, we have to adjust the dimensions of the transistors so that they can output the appropriate reference current, denoted as I_{ref}. Then, I_{ref} is amplified by the following current mirror [5]. Since biphasic pulse could avoid ion-charge accumulation in tissues, the control logic is designed to produce biphasic electrical stimulation pulses. It consists of two pairs of P and N transistors and uses two input signals, SIGN and UNSIGN, to determine the current direction through the nerve.

EXPERIMENT RESULTS

RF Front-End Circuit

In order to verify the function of this voltage rectifier, a sinusoidal wave is used as the RF coupling input signal, which amplitude is at 6~7V (peak to peak), and the frequency is at 2 MHz. The simulation result using Hspice is shown in Fig. 7 and the rectifier circuit can output a 3.3V with 0.1V ripple voltage.

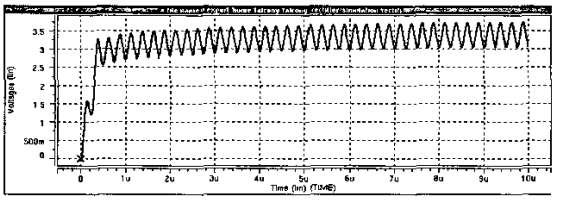

Figure 7. The simulating result of voltage rectifier circuit.

The output of the rectifier with some ripple can not meets our requirement. Hence a voltage regulator is necessary to deal with this voltage, and then to supply a stable dc level voltage for implantable devices. In addition, voltage regulator is made up with a two-stage operational amplifier and p-type transistor to form a negative feedback. For this reason, the performance of op-amp must be well designed for the application. The gain in our op-amp design is 55dB, and its phase margin is 80°. Based on simulation results, these specifications are efficient for a voltage regulator.

The simulation result of voltage regulator is shown in Fig. 8. The top one in Fig.8 is the output voltage of the rectifier at 3.3V with 0.1V ripple. The bottom one is the output voltage of the regulator. It is a stable output at 2.4V dc voltage.

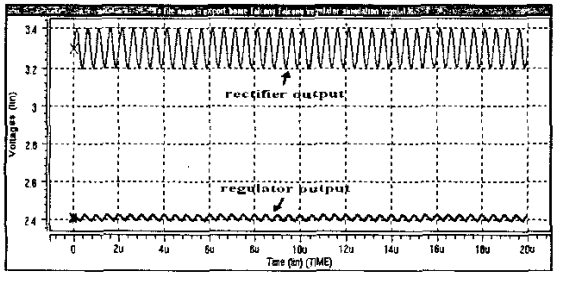

Figure 8. The output voltage of the voltage rectifier and regulator circuits.

Because the input voltage of the rectifier may fluctuate significantly with the unstable RF coupling signal and this variation affects the input voltage of the regulator. It is desirable to analyze the stability of regulator output with fluctuated input voltage. The simulation result is shown in Fig. 9. We can observe that the output voltage of the regulator can hold at 2.4V to 2.5V dc output when the input is higher than 3.3 V. Thus, the input regulation is less than 4%, and this specification meets our design goal.

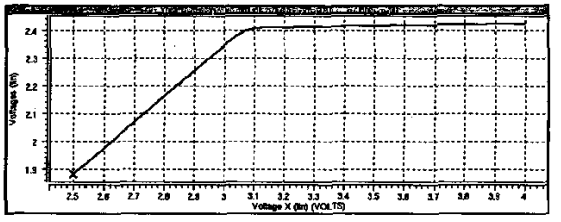

Figure 9. The output of voltage regulator versus the supply voltage.

Finally, Fig. 10 shows the simulation result of the demodulator output. This modulation signal is a 2MHz sinusoidal wave with 3V peak-to- peak amplitude, as shown in top panel. Middle panel shows the coding digital data with a repeating 5-bit high-low signal (01010). Bottom panel shows the extracting digital from top panel. We can find clearly that it is the same as the original data in panel 2. These results demonstrate that the demodulator can accurately extract out digital data modulated by external devices.

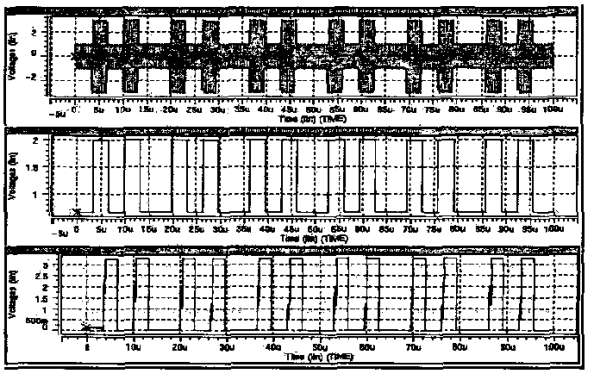

Figure 10. The simulation results of the demodulator.

Control Circuit

The control circuit is implemented with FPGA of Altera MAX7128. Fig. 11 shows the waveform of Manchester decoder where Channel_1 represents the extracted clock and Channel_2 represents the extracted data. The encoded data is 0000001101011,which is generated by the 8051 microprocessor.

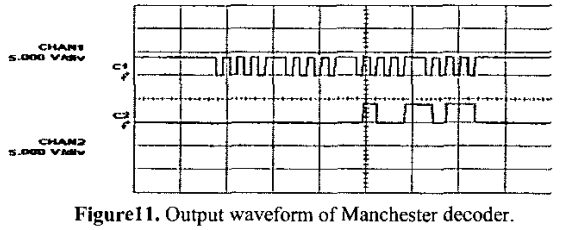

Figure11. Output waveform of Manchester decoder.

The current-source stimulator is designed by using the TSMC 0.25um CMOS technology. The layout of whole current-source

stimulator is shown in Fig. 12. Large transistor size is used in this design to maintain the linearity of the current source output.

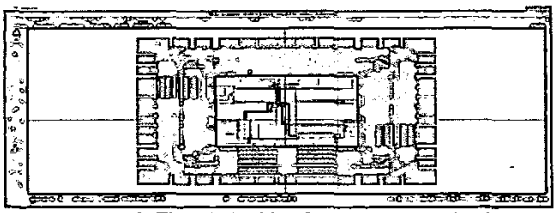

Figure 12. The whole chip of current-source stimulator.

The control circuit and micro-stimulator are combined in a PCB for hardware verification and shown in Fig. 13.

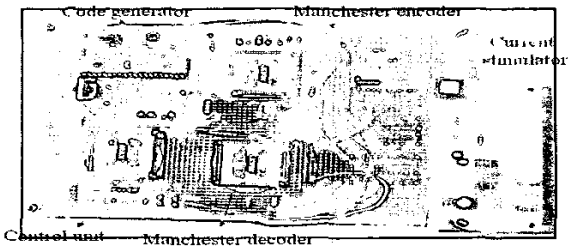

Figure 13. Physical circuits of the complete stimulation system.

In our design, the current stimulator produces 32 different currents. In software verification, the output current could be varied between 32 different levels ranging from 0 to 3.42 mA with approximately 108 uA for each level. However, in hardware verification the output current could be just up to 2.77 mA with approximately 87 uA for each level. The maximum power consumption of the current stimulator is less than 14 mW. Fig. 14 depicts the linearity of the current output. In Fig. 14, the star line is the linearity analysis simulated by MATLAB, and the circle line is the measured results of the current stimulator chip. Nonlinearity is occurred in large signal output.

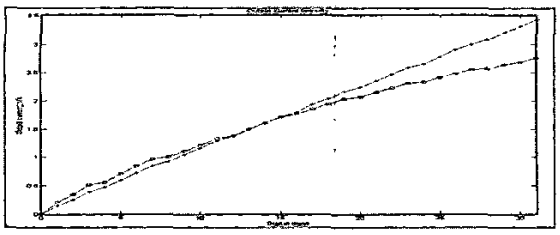

Figure 14. The linearity of the current output.

Finally, Fig. 15 and 16 show the verification of pulse width 300us and stimulation frequency 20Hz, respectively. The measured results show the match with the former design and fit the system requirement.

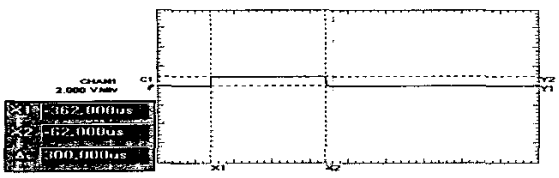

Figure 15. The pulse width of output current.

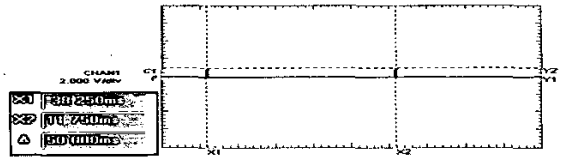

Figure 16. The Stimulation frequency.

CONCLUSION

In this study, most of the functional blocks for the implantable device have been verified by using Hspice according to the technology of TSMC 0.25um CMOS process. Our simulation results show that the RF front-end circuits can provide a stable 2.5V DC voltage and extract digital data accurately. All the simulation results can be a base for future fabrication of implantable bio-devices. Besides, the prototype of an 8-channel implantable microstimulator is proposed for functional neuromuscular stimulation in this paper. The digital circuits are implemented by the field programmable gate array. The analog circuits are implemented with CMOS 0.25um technology and fabricated by TSMC. The current stimulator can generate a maximum current of 2.77 mA through 1kΩ load while the stimulation frequency is 20Hz and the stimulation current pulse width is 300us.

The proposed designs for different blocks of micro-stimulator could be used as building block to realize other implantable devices. The Manchester code has been proved to be a good choice for transmission of implantable systems. The clock and the original data could be extracted from the Manchester decoder. The architecture of current stimulator could generate bi-directional current. Simulation results show a good linearity. And the prototype stimulation system could achieve the general specification of FNS (stimulation frequency 20Hz and stimulation current pulse width 300us). In the future, we will further integrate these presented components in a single chip of implanted animal for FNS experiment.

ACKNOWLEDGMENT

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