LOW NOISE PREAMPLIFIER DESIGN FOR NERVE CUFF ELECTRODE RECORDING SYSTEMS

Robert Rieger[1], John Taylor[1] and Nick Donaldson[2]

[1]Department of Electronic and Electrical Engineering,
[2]Department of Medical Physics and Bioengineering
University College London
j.taylor@ee.ucl.ac.uk

ABSTRACT

This paper discusses certain crucial issues involved in the design of a preamplifier for an implantable neuralprosthesis. The preamplifier has a nominal gain of 100, a bandwidth of 15KHz and is required to combine very low noise with low power consumption. In particular, due to the low frequencies involved, $1/f$ noise assumes great significance. We consider three possible architectures for the input stage of the preamplifier: (a) BICMOS and CMOS in (b) weak and (c) strong inversion. We demonstrate that although the CMOS amplifiers can approach the performance of the BICMOS circuit, this is only possible at the cost of greater power consumption and enormously increased circuit area. Against these arguments must be set the greater cost of a BICMOS process.

1. INTRODUCTION

Neural signals (ENG) recorded from insulating cuffs fitted with electrodes and placed around nerve bundles are replacing artificial sensors in providing feedback signals in *functional electrical stimulation* (FES) applications. Typical applications include correction of foot-drop [1] and hand grasp in tetraplegic patients [2]. Unfortunately, the ENG signal recorded using this method is on the order of a few μV and is embedded in noise generated by various mechanisms, notably *random noise* from the interstitial fluid and from the electrode-tissue interface. Amplifiers also contribute random noise and, especially in the case of MOS-based circuits, flicker or $1/f$ noise (which because of its spectrum is particularly harmful in a low frequency application such as this). In addition to random noise, *interfering signals* can have amplitudes of many mV. The main source of interference is the *electromyographic* (EMG) potential generated by excited muscles near the cuff. It is vital therefore, to amplify the ENG signals with as little extra noise as possible, while at the same time designing the system for maximum immunity to interference.

Nerve cuff electrodes are currently the most suitable recording devices, with safe implantation being reported for as long as 15 years [3,4]. Fig. 1 shows a cylindrical cuff fitted to a nerve bundle. If a symmetrical tripolar electrode structure of the type shown in Fig 1 is employed, the interfering signals appearing between each of the outer electrodes and the centre electrode are equal and opposite and can be cancelled by a suitably designed differential amplifier arrangement. In practice, exact cancellation is impossible due to manufacturing tolerances and tissue inhomogeneity. However in one particular tripolar arrangement, called the *true tripole* [5] these types of mismatch can be cancelled by adjusting the gains of the differential amplifiers. A suitable system to adaptively cancel interfering signals such as EMG by automatically adjusting the amplifier gains has been described in [6].

In order to simplify the design of the control system, the variable gain amplifiers are preceded by *preamplifiers* with a nominal gain of 100. The gain was chosen to be sufficiently high that noise would not be an issue in the design of the subsequent adaptive stages of the recording system.

In this paper we describe the design of the *preamplifiers* (an outline specification is given in Table 1, together with preliminary measured data). We seek to establish that an optimum arrangement in terms of performance, size and power consumption employs *npn* bipolar input transistors in a BICMOS design. The paper takes the form of a comparison between three designs with bipolar and MOS input stages. Although it has been suggested [7] that CMOS input stages operating in *weak inversion* can be used to advantage in this type of application, we show that this can only be achieved at the cost of increased power consumption and, particularly, an enormous increase in circuit area.

2. DESIGN CONSIDERATIONS

Since in this application, both very low noise and low power consumption are critical, it was decided to use a simple feed-forward architecture avoiding the use of physical resistors on the input side. The basic arrangement is shown in Fig 2 and consists of an *operational transconductance amplifier* (OTA) terminated in a resistor, *R1*. The combination of *R2* and *C* is chosen to

0-7803-7448-7/02/$17.00 ©2002 IEEE

restrict the bandwidth to about 15KHz, which is suitable for this application.

The OTA in Fig 2 consists of a differential pair transconductance stage terminated in a current mirror. For the purposes of comparison, signals and noise were measured in a short circuit at the output and the noise referred to the origin as an equivalent voltage. In addition, for the bipolar case, the input-referred current noise was taken into account by passing it through a noiseless 1KΩ resistance (representing the approximate ohmic resistance of the cuff electrodes in the relevant frequency band).

Three possible OTA architectures were considered: MOS transistors throughout, consisting of a PMOS differential stage and NMOS mirror using (a) *strong inversion* (si) and (b) *weak inversion* (wi) and, finally, (c) a BICMOS approach using *npn* bipolar transistors in the input differential pair with PMOS transistors (si) for the mirror. These basic circuits are shown in Fig 3.

(1) Transconductance gain, Gm

In all cases a transconductance (*Gm*) of 1mA/V was chosen and the device parameters are those for a 0.8μm BICMOS process. In the bipolar and *wi* MOS cases, knowledge of *Gm* allows the *tail* currents, *Is*, of the differential stages to be chosen immediately. Using the well-known expressions for the transconductance of these OTAs [8], these currents are 55μA and 78μA respectively. For all the MOS transistors, the aspect ratios, W/L, must be chosen initially to ensure (i) the correct region of operation (i.e. si/wi) and (ii) that the devices remain in saturation with the given supply voltages (±2.5V). The threshold between *wi* and *si*, is given by the following equation [8]:

$$I_D = \frac{W}{L} KP.2V_{th}^2 \qquad \ldots (1)$$

where I_D is the DC drain current, *KP* is the transconductance parameter and V_{th} is the thermal voltage (26mV at room temperature). For OTA(b), all devices are in *wi*. For the already-calculated value of I_S (78μA) and applying a safety factor of 4 in eqn (1) results in W/L = 3846/1 and 1358/1 for the input (PMOS) and mirror (NMOS) transistors respectively (these also satisfy the requirement (ii)).

In the *si* CMOS case, *Gm* depends on both the aspect ratios of the transistors, W/L and I_S. The solution is therefore not unique and in this example, the minimum value of I_S was chosen, for low power consumption. Allowing a safety factor of 8, eqn (1) was solved with the expression for *Gm* giving values of I_S and W/L of 150μA and 222/1, respectively.

Finally, for the BICMOS case, a value of W/L of 1.5/1 was chosen initially, as satisfying the basic requirements (i) and (ii).

(2) Input-referred noise

The input-referred voltage noise of CMOS OTAs at low frequencies was first discussed by Bertails in 1979 [9]. By representing the noise sources of each transistor by a voltage source at its input, the total noise contribution can be calculated by considering the voltage gains from the device to the amplifier output. For equal transconductances of all transistors, the input-referred *1/f* noise voltage of an OTA in *si* is given by:

$$\sqrt{\overline{v^2}} = \sqrt{\frac{2}{f}}\sqrt{\frac{KF_{in}}{W_{in}L_{in}} + \frac{KP_m KF_m L_{in}}{KW_{in}L_m^2}} \qquad \ldots (2)$$

where *'in'* denotes the input MOS and *'m'* the mirror transistors and *KF* is the flicker noise coefficient. In *wi* and with all *n* taken to be equal:

$$\sqrt{\overline{v^2}} = \sqrt{\frac{2}{f}}\sqrt{\frac{KF_{in}}{W_{in}L_{in}} + \frac{n^2 KF_m}{W_{in}L_m}} \qquad \ldots (3)$$

For *bipolar* input transistors:

$$\sqrt{\overline{v^2}} = \sqrt{\frac{2}{f}}\sqrt{\frac{KF_b I_c}{\beta} 2q(r_b + R_s)^2 + \frac{2KPV_{th}^2 KF_m}{I_c L_m^2}} \qquad \ldots (4)$$

where I_c is the collector current, β is the forward current gain, r_b is the base spreading resistance and R_s is the cuff (source) resistance.

The procedure to minimise both the noise floor and the 1/*f* noise, is summarised in Table 2. Notice that for all cases, the *noise floor* is strongly linked to *Gm* and hence in this example is constrained by the preselected value of 1mA/V. On the other hand, the 1/*f* components are dominated by the device geometries. In line with these requirements, some preliminary choices of device sizes were made. These are given in Table 3 and form the basis of the simulation results presented in the next section.

3. PRELIMINARY RESULTS AND DISCUSSION

A model of the OTA input stage was simulated using the CADENCE design tools. For the example design described above, the resulting input-referred noise values are plotted in Fig 4. The noise floors are quite similar for each design, the BICMOS having the lowest value at about $4nV/\sqrt{Hz}$. The BICMOS case also has the best 1/*f* noise performance, followed respectively by the CMOS *si* and *wi* OTAs. However, as Table 3 shows, in order to obtain this performance from the CMOS OTAs, more power and, in particular, a huge increase in device size is required compared to the BICMOS case. This should, of course be set against the extra cost of using a BICMOS process.

The example described is, of course, not unique. However, it was felt that the choice presented showed a reasonable compromise solution to the requirements of an implanted device for a neural prosthesis.

5. REFERENCES

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TABLE 1
Preamplifier Outline Specification and Preliminary Measured Results

	Specification	**Measured**
Voltage gain	100	110
Bandwidth	15KHz	14KHz
Common mode rejection ratio	100dB	82dB
Total equivalent input voltage noise	$< 5nV/\sqrt{Hz}$	$3.8nV/\sqrt{Hz}$
Power supplies	±2.5V	±2.5V
Power consumption	1.2mW	1.3mW

TABLE 2
Procedure for Noise Reduction in OTAs
at constant *Gm*

Circuit	**Minimise noise floor**	**Minimise 1/*f* noise**
(a) CMOS, *si*	(depends on *Gm*)	Maximise input transistor *width* Maximise mirror transistor *length*
(b) CMOS, *wi*	(depends on *Gm*)	Maximise all transistor *areas*
(c) BJT input transistors PMOS mirrors in *si*	Reduce *base spreading resistance*, r_b. (also depends on *Gm*)	Maximise mirror transistor *length*

TABLE 3
Transistor Dimensions for Simulation Example
(all device dimensions in μm or μm^2)

Device	**BICMOS**	**CMOS OTA (si)**	**CMOS OTA (wi)**
Input transistors		17,250/75	73,000/18
Mirror transistors	120/80	2,400/1,200	62,750/46
Active area	19,296	8,347,500	8,401,000
Tail current	55μA	150μA	78μA
Powerconsumption (±2.5V)	275μW	750μW	390μW

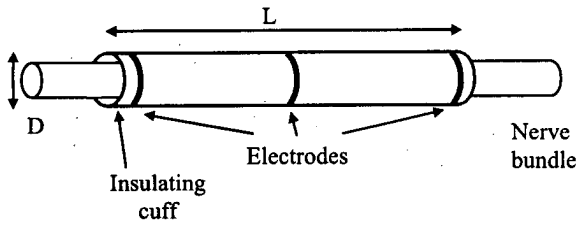

Fig 1: An insulating cuff and *tripolar* electrode assembly fitted to a nerve bundle.

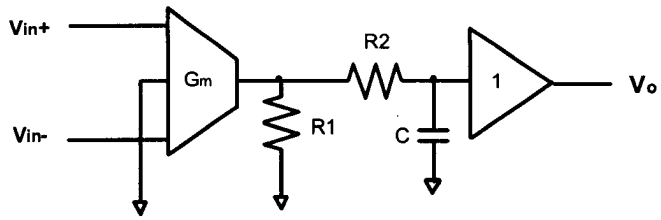

Fig 2: Basic Preamplifier Architecture

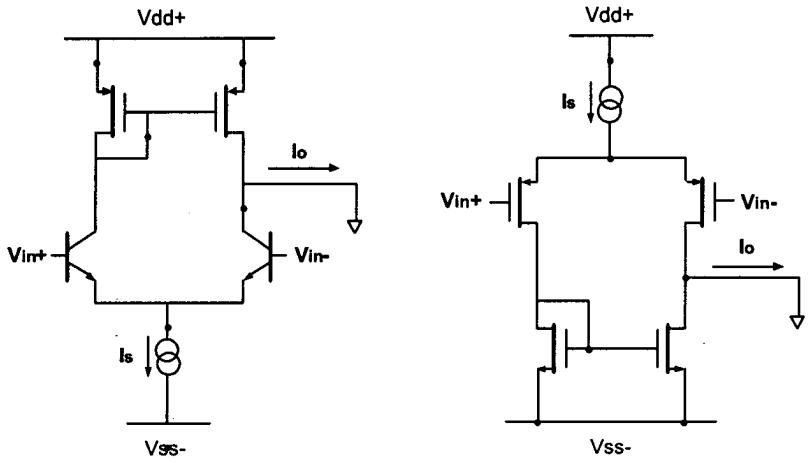

Fig 3: Candidate OTA Circuits

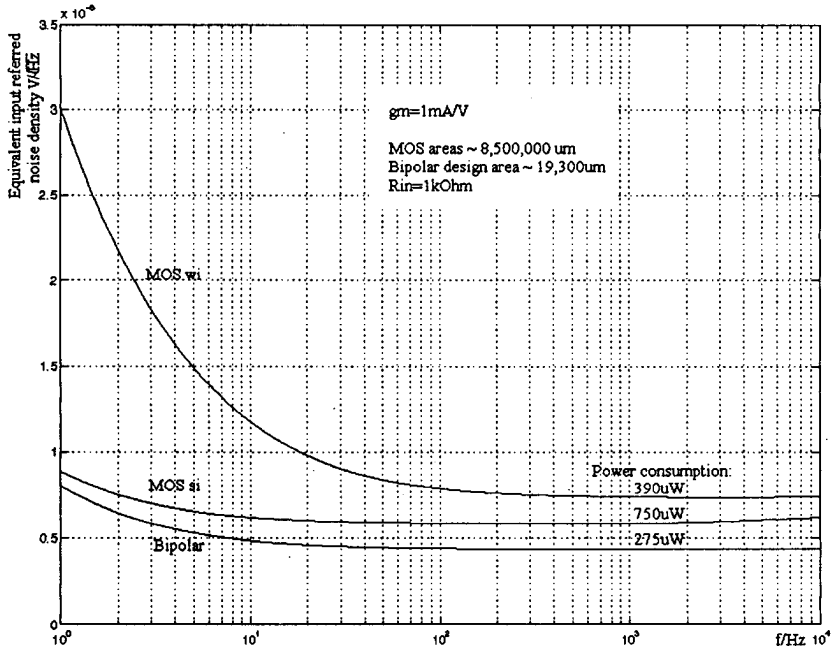

Fig 4: Input Referred Noise for Each OTA