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A HIGH-PERFORMANCE ADAPTIVE ENG AMPLIFIER

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ABSTRACT

This paper describes an integrated adaptive amplifier for recoding electroneurogram (ENG) from tripolar cuff electrodes. The amplifier can automatically compensate for cuff imbalance, thus offering a fully implantable solution to this problem. The circuit was fabricated in 0.8 μm BiCMOS technology with an active area of 0.7 mm^2. Measured results showed that the ENG amplifier has a cuff imbalance correction range of > ±40%, and a signal-to-interference ratio of about 2/1 (6 dB) even for ±40% imbalance.

1. INTRODUCTION

Nerve cuff electrodes are the only proven chronic method for recording neural signals (ENG) [1]. Monitoring nerve operation allows some level of intervention by means of functional electrical stimulation for partial control of organs suffering from paralysis. Unfortunately, cuff electrodes have poor *signal-to-interference ratio* (SIR), because the ENG signal is so small (μV). Moreover, cuffs are prone to myoelectric interference (EMG) from nearby muscles which produce mV potentials.

Various schemes have been proposed to combat this problem. One of the established approaches employs tripolar electrodes in a cuff, connected to two differential amplifiers whose outputs are subtracted. In this *true-tripole* (TT) configuration [2], EMG interference from outside the cuff, appears equally on the two channels because of the cylindrical insulating cuff, and is thus, in theory at least, cancelled. However, in practice, due to *cuff imbalance* caused by various factors [3], significant EMG artifact remains.

To automatically compensate for cuff imbalance, and thus, improve the quality of the recorded ENG, the *adaptive-tripole* (AT) has been proposed, and its first integrated realization was reported in [4]. However, the realization in [4] showed poor performance in terms of SIR, harmonic distortion, imbalance correction range and yield. This paper describes an improved realization of the AT which overcomes all the limitations of the first design. These enhancements were necessary in order to make the system fully implantable. The targeted biomedical application is a bladder implant.

The remaining sections of the paper are organized as follows. Section 2 outlines the system description, while Section 3 describes the circuit design of the various building blocks. *In-vitro* measurements are presented in Section 4, and conclusions are drawn in Section 5.

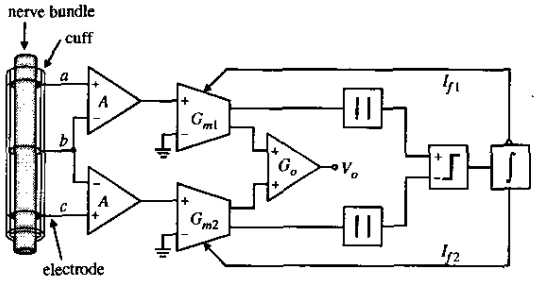

Fig. 1. The adaptive-tripole (AT) architecture.

2. SYSTEM DESCRIPTION

The block diagram of the AT realization described in this paper is shown in Fig. 1. The system consists of two voltage preamplifiers, each with a fixed gain A, providing a low-noise interface with the cuff electrodes. These are followed by two operational transconductance amplifiers (OTAs) with variable gains G_{m1} and G_{m2}, controlled by the differential feedback currents I_{f1} and I_{f2}. The control stage operates by first obtaining the moduli of the currents at the output of the variable-gain OTAs and applying them to a current comparator to establish which is the largest. The comparator output is applied to a large time constant integrator which generates I_{f1} and I_{f2}. The variable-gain OTAs counterbalance the presence of cuff imbalance, by equalizing the amplitudes of the EMG signals at their outputs. As a result, when the output signals of the OTAs are summed at the input of the output-stage amplifier (gain G_o), the equal and anti-phase EMG signals from the two channels are cancelled, and the in-phase ENG signals are added and further amplified.

In practice, cuff imbalance (X_{imb}) can be calculated by:

$$X_{imb} = \left(\frac{|V_{ab}| - |V_{cb}|}{|V_{ab}| + |V_{cb}|} \right) \times 100\% \qquad (1)$$

where V_{ab} and V_{cb} are the voltages across nodes *ab* and *cb* in Fig. 1, respectively.

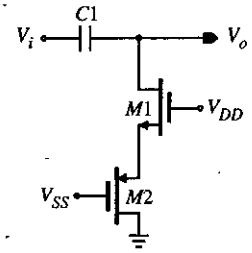

Fig. 2. Preamplifier AC-coupling.

3. CIRCUIT DESIGN

3.1. Low-noise preamplifiers

The design of the BiCMOS preamplifiers was described in [5], and thus, it is not repeated here. The output of each preamplifier is AC-coupled by means of the passive high-pass filter shown in Fig. 2. The series combination of transistors *M*1 and *M*2, forms a high value (20 MΩ) grounded linear *active* resistor, and combined with *C*1 (80 pF) provides a cut-off frequency of about 100 Hz.

3.2. Variable-gain OTAs

The composite signal at the input to each AT channel consists of EMG and ENG with nominal values after pre-amplification of around ±50 mV and ±100 μV, respectively. The control stage is required to have sufficient gain to amplify the ENG to a reasonable amplitude (±20 mV) and also sufficient linearity to accommodate the EMG signal. Each variable-gain stage was realized by a symmetrical CMOS OTA of the type shown in Fig. 3. The circuit has two current outputs, I_{o1} and I_{o2}, each connecting to the input of a full-wave rectifier or to the input of the output-stage amplifier. In practice, all current mirrors (*M*3-*M*10) are regulated cascodes [6] for high accuracy.

In strong inversion and assuming matched transistors

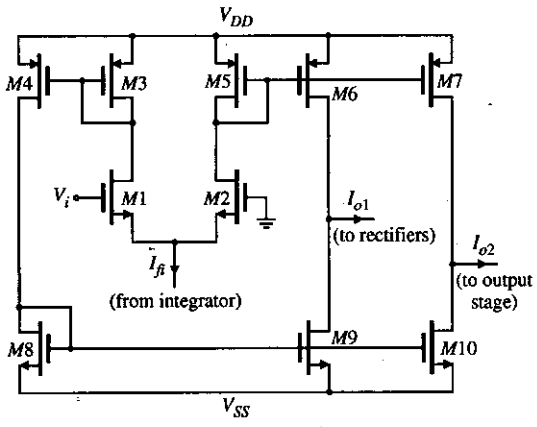

Fig. 3. Variable-gain OTA circuit.

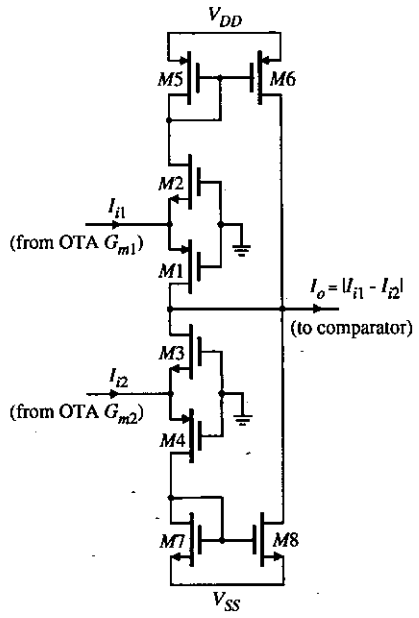

Fig. 4. Current-mode rectifiers.

in Fig. 3, the OTA transconductance is given by

$$G_m = \sqrt{2I_{fi}k}, \quad V_i << \sqrt{I_{fi}/2k} \qquad (2)$$

where k is the transconductance parameter, V_i is the input voltage, and I_{fi} is the feedback current. To maintain less than 1% nonlinearity, it is required that

$$|V_i| < 0.28\sqrt{I_{fi}/2k} \qquad (3)$$

From (2) it is seen that gain control may be implemented by varying I_{fi} either side of its mean value.

3.3. Full-wave current rectifiers

The two full-wave rectifiers shown in Fig. 1 were realized by the current-mode circuit in Fig. 4. The upper rectifier (*M*1, *M*2, *M*5, *M*6) operates on current I_{i1} stemming from OTA G_{m1}, while the lower rectifier (*M*3, *M*4, *M*7, *M*8) operates on current I_{i2} stemming from OTA G_{m2}. The core of each rectifier are the complementary transistors *M*1, *M*2 (upper rectifier) and *M*3, *M*4 (lower rectifier), each transistor performing half-wave precision current rectification [7]. During positive excursions of I_{i1} and I_{i2}, *M*1 and *M*4 are turned on and *M*2 and *M*3 are turned off. During negative excursions of I_{i1} and I_{i2}, *M*2 and *M*3 are turned on and *M*1 and *M*4 are turned off. In practice, the two unity-gain current mirrors (*M*5 – *M*8) are regulated cascodes. The addition of the various drain currents is done at the input node of the current comparator, resulting in the output current $I_o = |I_{i1} - I_{i2}|$.

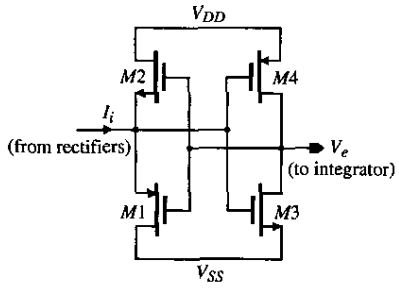

Fig. 5 Current comparator.

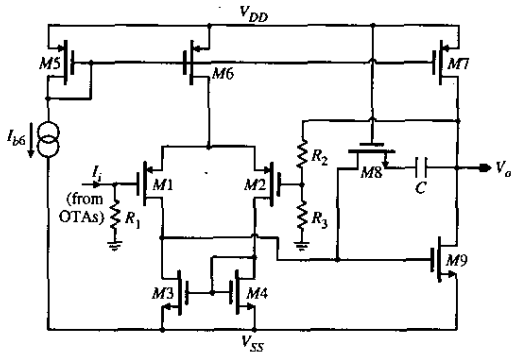

Fig. 7. Output-stage amplifier.

3.4. Current comparator

The current comparator [8] shown in Fig. 5 uses a CMOS inverter (*M*3, *M*4) to apply negative feedback around a class-B voltage buffer (*M*1, *M*2). As a result of the feedback, the comparator input has a low-impedance (in general) and is thus ideal for determining the polarity of the input current I_i.

3.5. Large time constant integrator

Because of the nature of cuff imbalance variations, the integrator time constant should be large. System level simulations have shown that a time constant of about 1 s is required for this application. The integrator schematic is shown in Fig. 6 and the circuit comprises three stages. The first stage consisting of the simple CMOS OTA (*M*1 – *M*4) terminated in resistor *R*1 (2 kΩ), is an attenuator which also corrects amplitude variations between the comparator peak-positive and peak-negative output voltages. The second stage is the actual OTA-C integrator (operated in weak inversion), and this consists of a CMOS OTA (*M*5 – M11) utilizing transconductance cancellation [9], and an integrating capacitor *C*1 (47.5 pF). The attenuation provided by the first stage ensures that the input voltage to the second stage OTA is within its linear range of operation. Transistor *M*11 performs level-shifting of the output voltage for interfacing with the third stage (*M*12 – *M*17), the latter generates currents I_{f1} and I_{f2}. The tail currents of the three stages are provided by the DC current sources I_{b1}, I_{b2} and I_{b3}. The integrator time constant is $2C1/g_o$, where g_o is the small-signal output conductance seen into node *y*, and g_o is set by I_{b2}.

3.6. Output-stage amplifier

The output-stage amplifier is shown in Fig. 7. The second output branch from each variable-gain OTA (Fig. 3) is hardwired to resistor *R*1 (50 kΩ) where the two composite currents I_{i1} and I_{i2} are summed-up to form I_i. The op-amp (*M*1 – *M*9) is configured as a non-inverting amplifier through the feedback resistive network *R*2 (90 kΩ) and *R*3 (10 kΩ). The op-amp employs zero-pole compensation realized by the series combination of transistor *M*8 and capacitor *C* (3.5 pF), and biasing is provided by the DC current source I_{b4}.

4. MEASURED RESULTS

The adaptive ENG amplifier was fabricated in the austriamicrosystems 0.8 μm BiCMOS process. The input AC signals V_{ENG} (representing the ENG) and V_{EMG} (representing the EMG) to the chip, were provided by

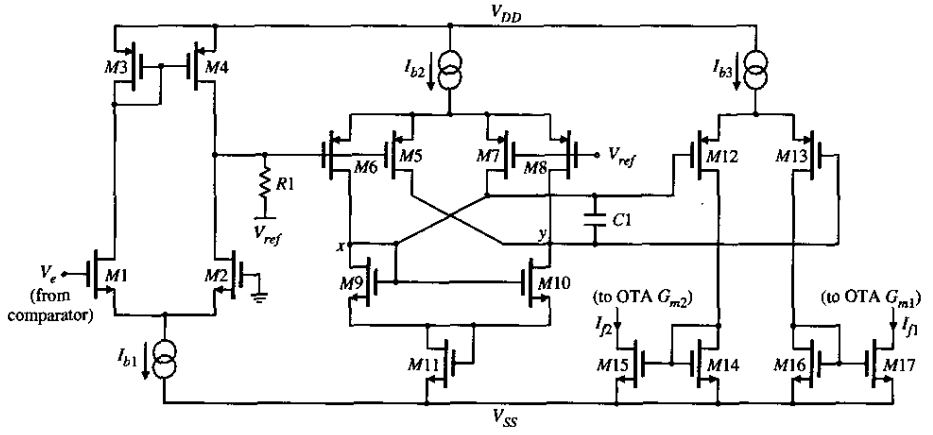

Fig. 6. Large time constant integrator circuit.

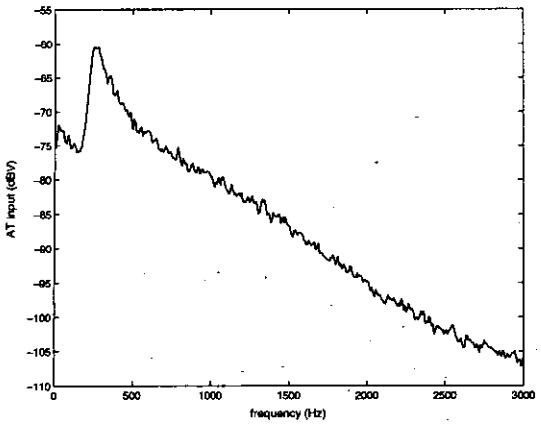

Fig. 8. Spectrum of input composite signal.

two audio transformers. Initially, the chips were tested with sinusoidal V_{EMG} (100 Hz) and V_{ENG} (1 kHz) with nominal peak amplitudes across nodes *ac* in Fig. 1 of 1 mV and 2 μV, respectively. Subsequently, in order to model a more realistic test, V_{EMG} was replaced by an arbitrary signal with the frequency spectrum plotted in Fig. 8. The frequency content of this signal varies between 1 Hz and 3 kHz, with a peak at approximately 250 Hz, which is the case with a real EMG signal [10]. The V_{ENG} was kept in all measurements as a sinusoid with the characteristics mentioned above. In Fig. 8, the V_{ENG} (-114dB) is buried under the spectrum floor of the V_{EMG}.

Fig. 9 shows the time-domain and frequency-domain outputs of the AT for -40% imbalance. The spectrum shows that the SIR is better than 3 (9.54 dB) even for 40% imbalance. This should be compared with an input SIR of 1/500 (-54 dB) and a corresponding TT output SIR of 1/200 (-46 dB). This result shows the superiority of the AT relative to any filtering technique because its operation is not frequency related. The main parameters of the AT chip are summarized in Table 1.

Table 1. Summary of performance.

Parameter	Value
Technology	0.8 μm BiCMOS
Power consumption	7.5 mW
Active area (core)	0.7 mm^2
SIR	> 6dB
Imbalance range	> ± 40%
Chip yield	100%

5. CONCLUSION

The design of a high-performance adaptive ENG amplifier for interface with tripolar cuff electrodes has been described. The device offers a fully implantable solution to the problem of cuff imbalance. The described realization overcomes many of the limitations of a previous design in terms of SIR, harmonic distortion, imbalance correction range and yield.

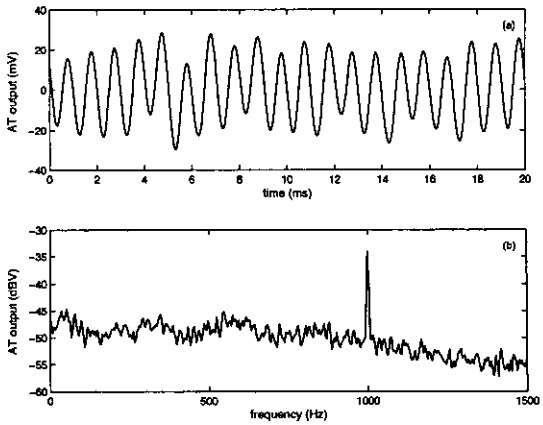

Fig. 9. System output for -40% imbalance. (a) time-domain; (b) frequency domain.

6. ACKNOWLEGEMENTS

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7. REFERENCES

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