### **Circuit Layout Techniques And Tips (Part I of VI)**

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# The Art Of Laying Out Two-Layer Boards

In this highly competitive, battery-powered marketplace, cost objectives usually dictate that a designer use two-layer boards in the design. Although the multi-layer board (4-, 6- and 8-layers) allows the designer to build cleaner solutions in terms of size, noise and performance, financial pressures force the engineer to rethink layout strategies with the two-layer board in mind. In this article we discuss the use or misuse of auto-routing, the concept of current return paths with and without ground planes, and recommendations for component placement where two-layer boards are concerned.

### Pay Now Or Pay Later With The Auto-Router And Analog Circuits

It is tempting to use the auto-router when designing printed circuit board (PCB.) More often than not, a purely digital board, (especially if the signals are relatively slow, and the circuit density is low) will work just fine. But as you try to lay out analog, mixed-signal or high-speed circuits with the auto-routing tool that is available with your layout software there may be some issues. The probability of creating serious circuit performance problems is very real.

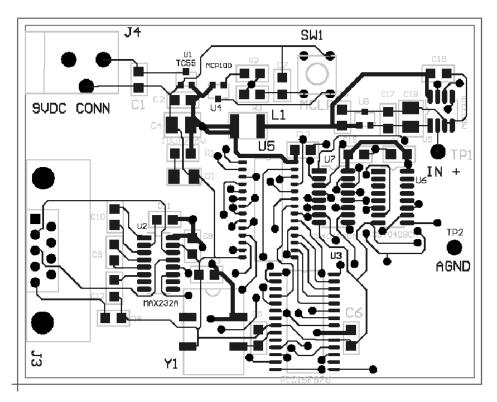


Figure 1. Top layer of an auto-routed layout of circuit diagram shown in Figure 3.

For instance, the auto-routed top layer of a two-layer board is shown in Fig. 1. The bottom layer of this board is in Fig. 2, and the schematic for these layers is in Figs. 3a and

3b. For the layout of this mixed-signal circuit the devices were manually placed on the board with careful thought to separating the digital and analog parts.

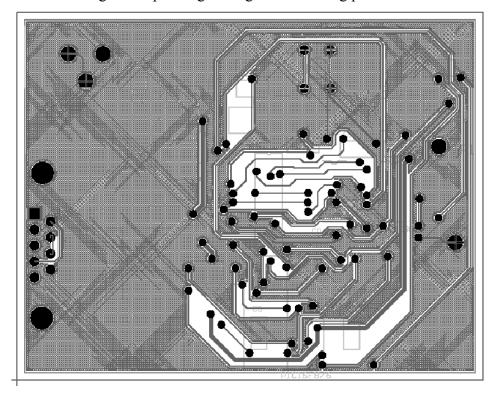


Figure 2. Bottom layer of an auto-routed layout of circuit diagram shown in Figure 3.

With this layout there are several areas of concern, but the most troubling issue is the grounding strategy. If the ground traces are followed on the top layer, every device is connected through traces on that layer. A second ground connection for every device uses the bottom layer with vias at the far right-hand side of the board. The immediate red flag that one should see when examining this layout strategy would be the existence of several ground loops. Additionally, the ground return paths on the bottom side are interrupted with horizontal signal lines. The saving grace with this grounding scheme is that the analog parts (MCP3202, 12-bit ADC and MCP4125, 2.5-V voltage reference) are at the far right-hand side of the board. This placement ensures that digital ground signals do not pass under these analog chips.

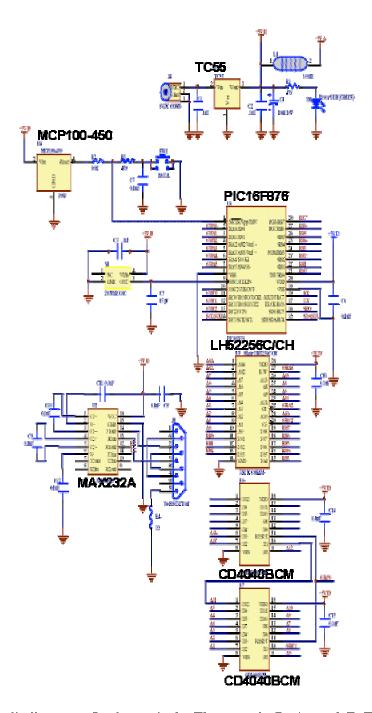


Figure 3a. Circuit diagram for layouts in Figures 1, 2, 4, and 5. This is the circuit diagram from Microchip's MXDEV $^{TM}$  board, evaluation board for the 10- and 12-bit ADCs (MCP300X and MCP320x).

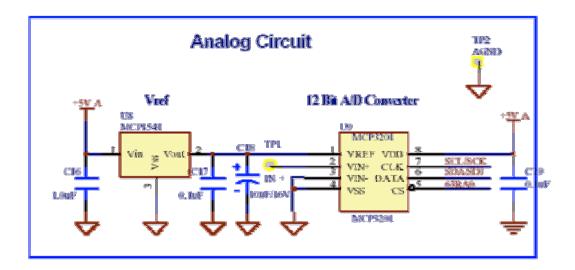


Figure 3b. Analog section of circuit diagram for layouts in Figures 1, 2, 4, and 5. This is the circuit diagram from Microchip's MXDEV<sup>TM</sup> board, evaluation board for the 10- and 12-bit ADCs (MCP300X and MCP320x).

The manual layout of the circuit shown in Figs. 3a and 3b is given in Figs. 4 and 5. With this manual layout a few general guidelines are followed to ensure positive results:

- Use the ground plane as a current return path as much as possible.
- Separate the analog ground plane from the digital ground plane with a break.
- If interruptions from signal traces are required on the ground-plane side, make them vertical to reduce the interference with the ground current return paths.
- Place analog circuitry at the far-end of the board and digital circuitry closest to the power connects. This reduces the effects of  $\delta i/\delta t$  from digital switching.

Note that with both of these two-layer boards there is a ground plane on the bottom. This is only done so that an engineer working on the board can quickly see the layout when trouble shooting. This strategy is typically found with a manufacturer's demo and evaluation boards. But, more typically, the ground plane is on the top of the board, thereby reducing electromagnetic interference (EMI.)

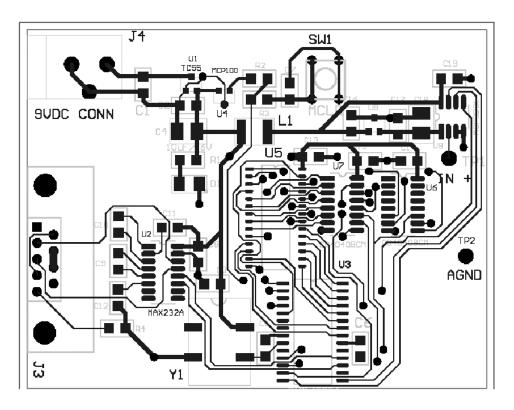


Figure 4. Top layer of a manual routed layout of circuit diagram shown in Figure 3.

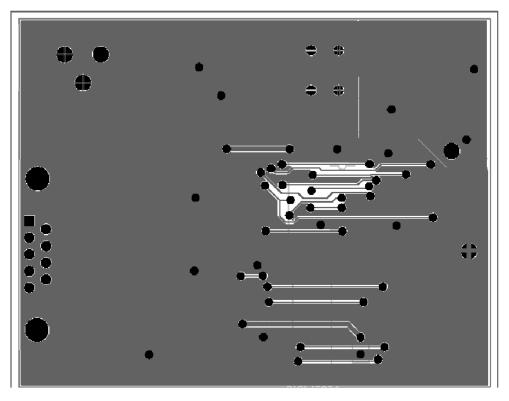


Figure 5. Bottom layer of a manual routed layout of the circuit diagram shown in Figure 3.

#### **Current Return Paths With Or Without A Ground Plane**

The fundamental issues that should be considered when dealing with current return paths are:

- In the event that you are considering using traces for the ground connects on your PCB, they should be designed to be as wide as possible. This is a good rule of thumb, but also understand that the thinnest width in your ground trace will be the effective width of the trace from that point to the end, where the "end" is defined as the point furthest from the power connection.
- Ground loops should be avoided.
- If no ground plane is available, star connection strategies should be used.

A graphical example of a star connection strategy is shown in Fig. 6.

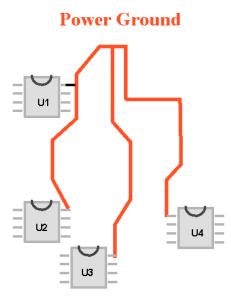


Figure 6. If a ground plane is not feasible, current return paths can be handled with a "star" layout strategy.

With this type of approach the ground currents return to the power connection independently. You will note that in Fig. 6 all of the devices do not have their own return path. With U1 and U2, the return path is shared. This can be done if guidelines #4 and #5 below are followed.

- 1. Digital currents should not pass across analog devices.
- 2. During switching, digital currents in the return path are fairly large, but only briefly. This phenomenon occurs due to the effective impedance (inductance and resistance) of the ground. With the inductance portion of the ground plane or trace, the governing formula is  $V = L\delta i/\delta t$ , where V is the resulting voltage, L is the inductance of the ground plane or trace,  $\delta i$  is the change in current from the digital device and  $\delta t$  is the time span considered for the event. To calculate the effects of the resistance portion

- of the ground plane, changes in the voltage simply change because of V = RI, again where V is the resulting voltage, R is the ground plane or trace resistance and I is the current change caused by the digital device. These changes in the voltage of the ground plane or trace across the analog device will change the relationship between ground and the signal in the signal chain.
- 3. High-speed current should not pass across lower speed parts. Ground-return signals of high-speed circuits have a similar effect on changes to the ground plane. Again the more important formulas that determine the effects of this interference are V = Lδi/δt for the ground plane or trace inductance and V = RI for the ground plane or trace resistance. As with digital currents, high-speed circuits that ground activity on the ground plane or that trace across the analog part change the relationship between ground and the signal in the signal chain.
- 4. Regardless of the technique used, the ground return paths must be designed to have a minimum resistance and inductance.
- 5. If a ground plane is used, breaks in the plane can improve or degrade circuit performance. Use with care.

A clean way of separating analog and digital ground planes is shown in Fig. 7.

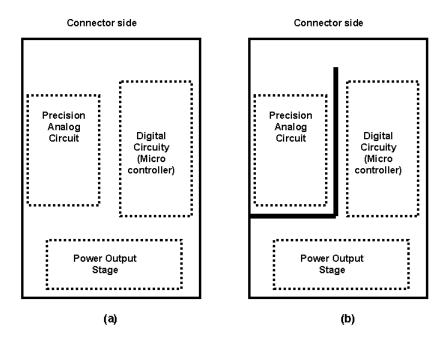


Figure 7. Sometimes a continuous ground plane is less effective than if the ground plane was separated. In this Figure a) shows a less desirable grounding layout strategy than is shown in b).

The precision analog (Fig. 7) is closer to the connector, but it is isolated from the activity in the digital network as well as the switching currents from the power supply circuit. This is a very effective way of keeping the ground return paths separated. This technique was also used in the layout previously discussed in Figs. 4 and 5.

## **Two Layer Board Layout Hints - Conclusion**

At every layout-related presentation that I give in a seminar setting, a question that is always asked in one form or another is, "What if management tells me I can't have two layers or a ground plane, and I still need to reduce noise in the circuit? How do I design my circuit to work around the need for a ground plane?" Typically, I instruct the person asking the question to simply inform management that a ground plane is required if they want reliable circuit performance. The primary reason for using ground planes is lower ground impedance. They also provide a degree of EMI reduction.

But, if you are unable to win that battle because of cost constraints, this article offers some suggestions such as star networks, and current return paths, which if used properly will give a little relief with circuit noise.

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