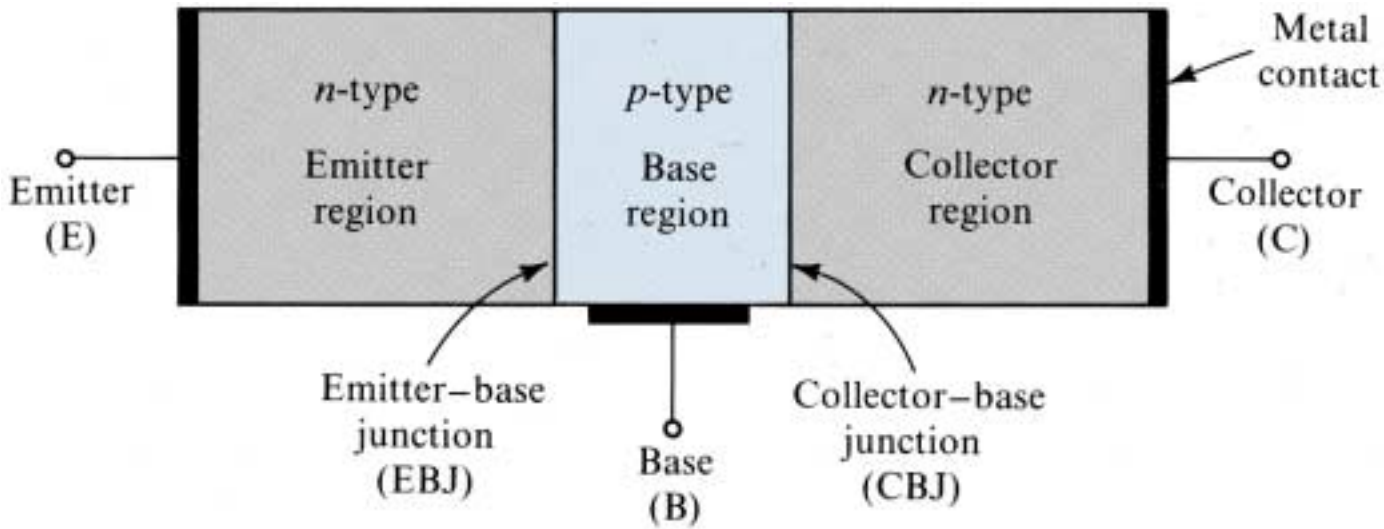
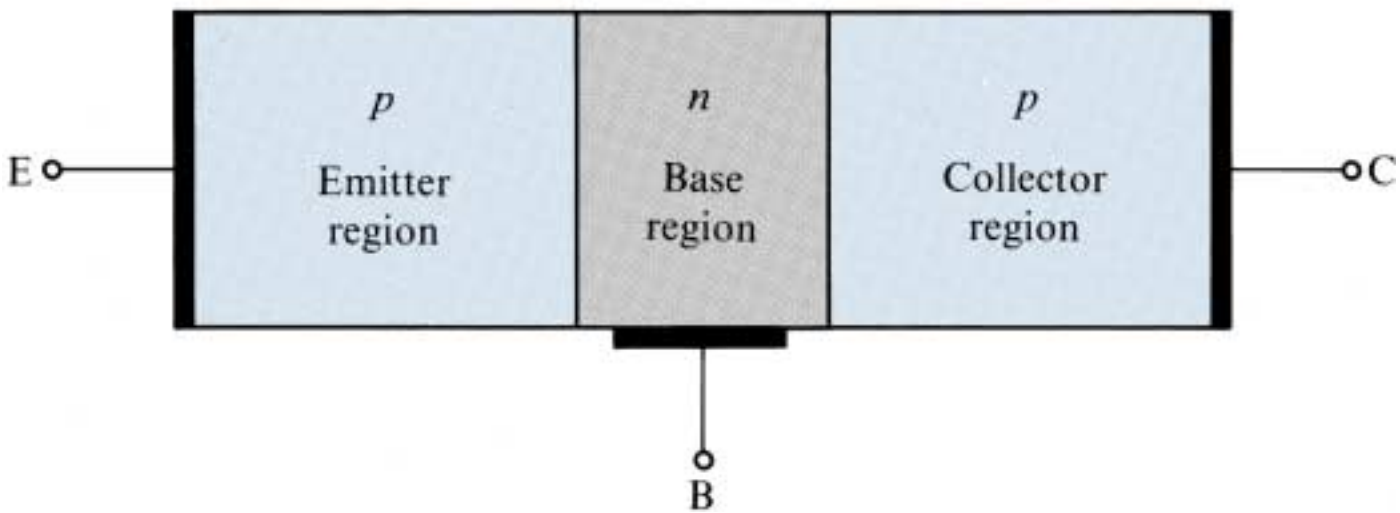
EE-4232

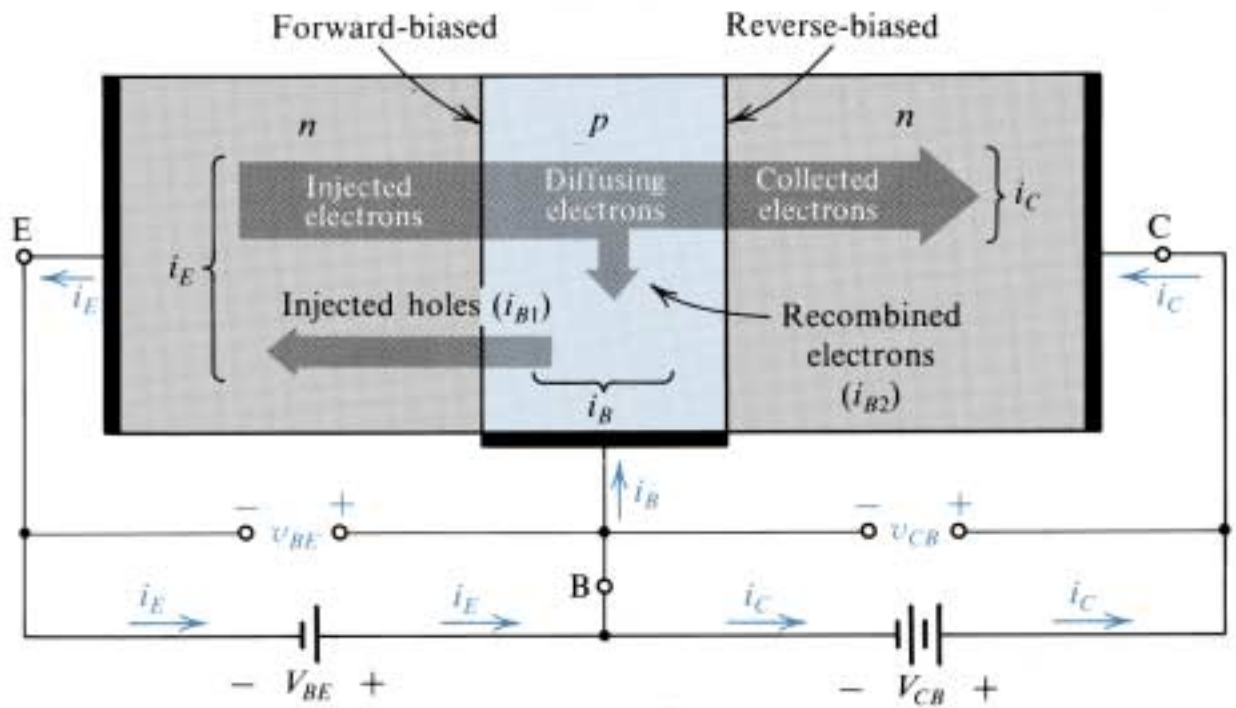
Review of BJTs, JFETs and MOSFETs



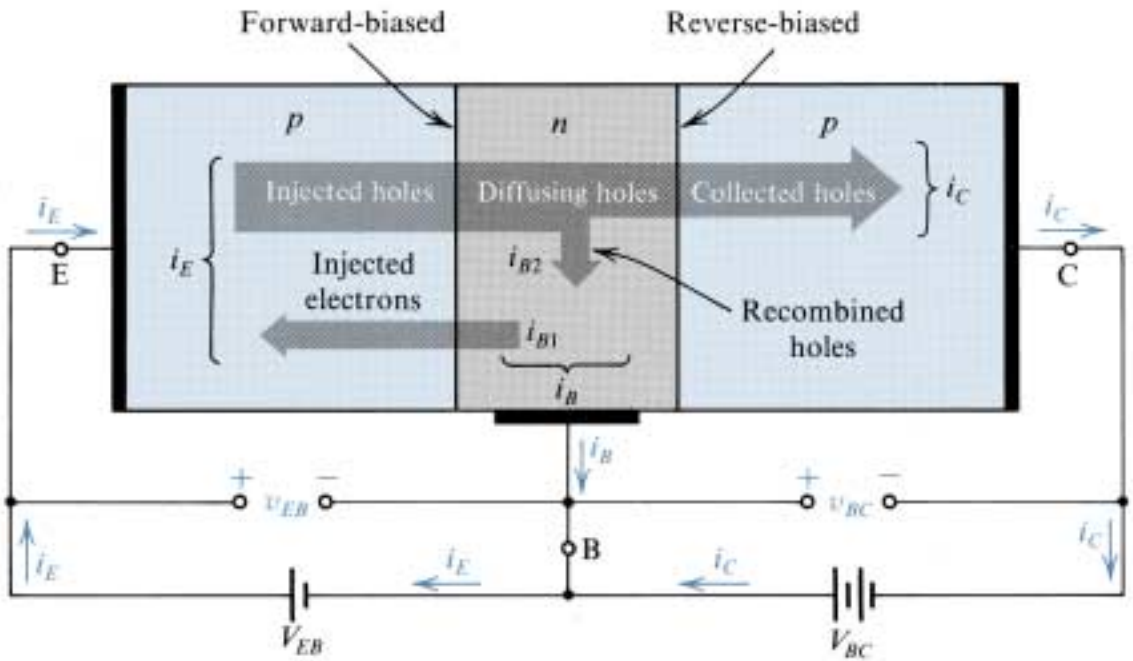
A simplified structure of the *npn* transistor.



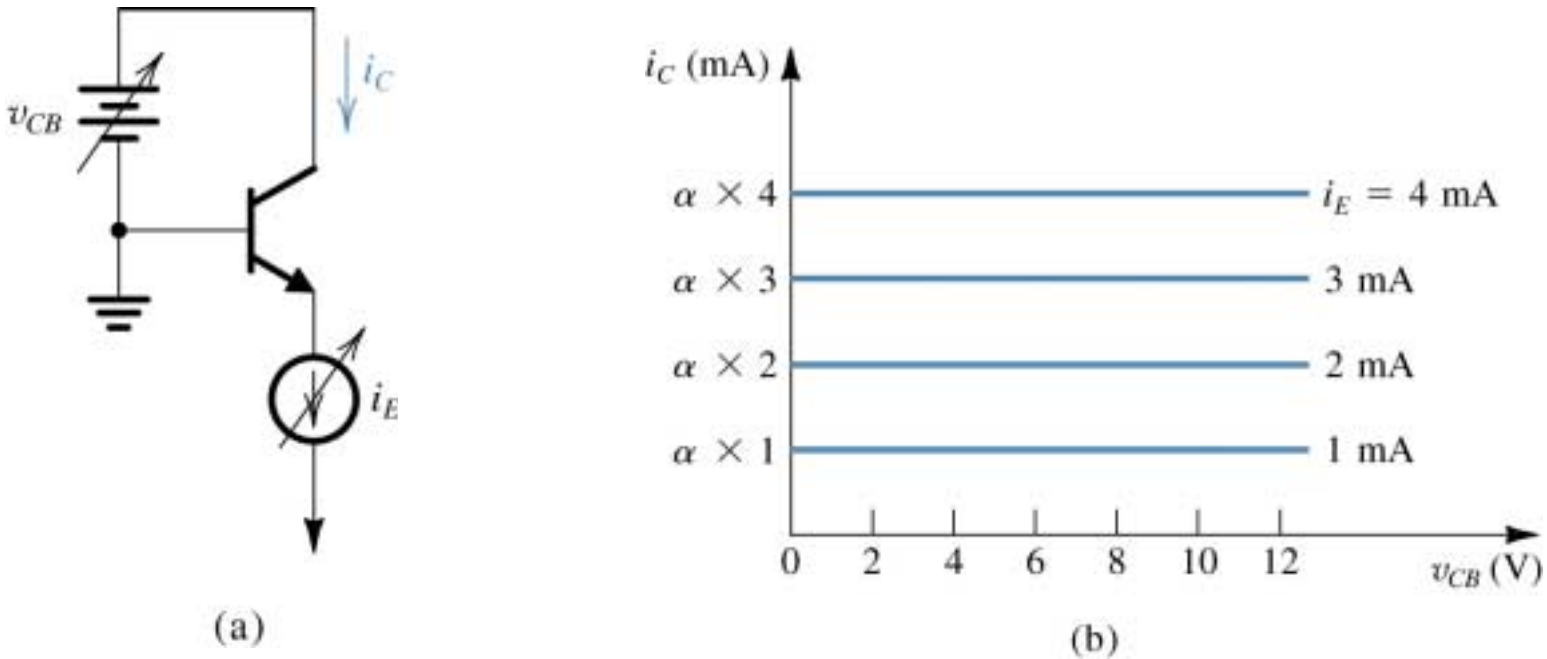
A simplified structure of the *pnp* transistor.



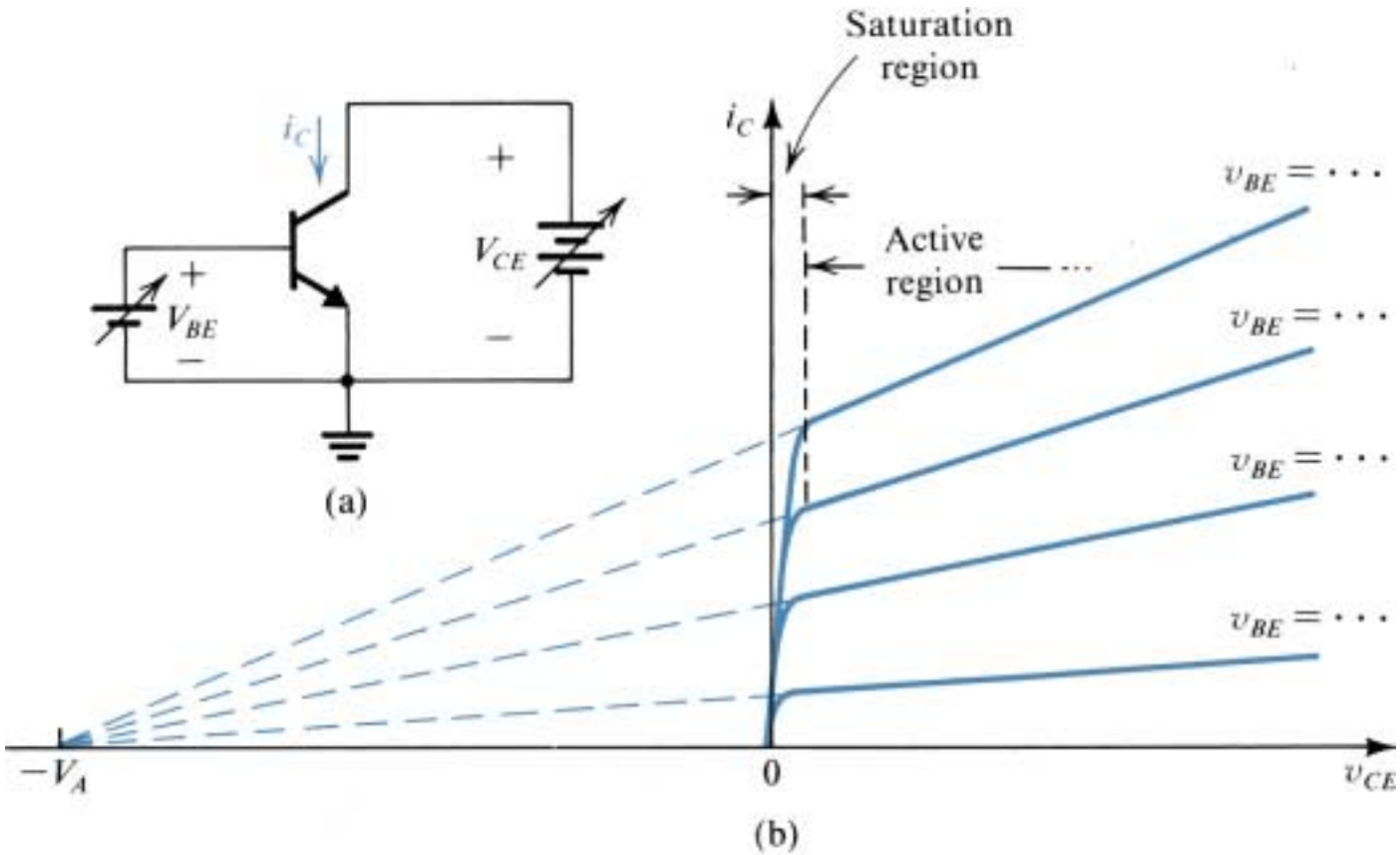
Current flow in an *npn* transistor biased to operate in the active mode, (Reverse current components due to drift of thermally generated minority carriers are not shown.)



Current flow in an pnp transistor biased to operate in the active mode.

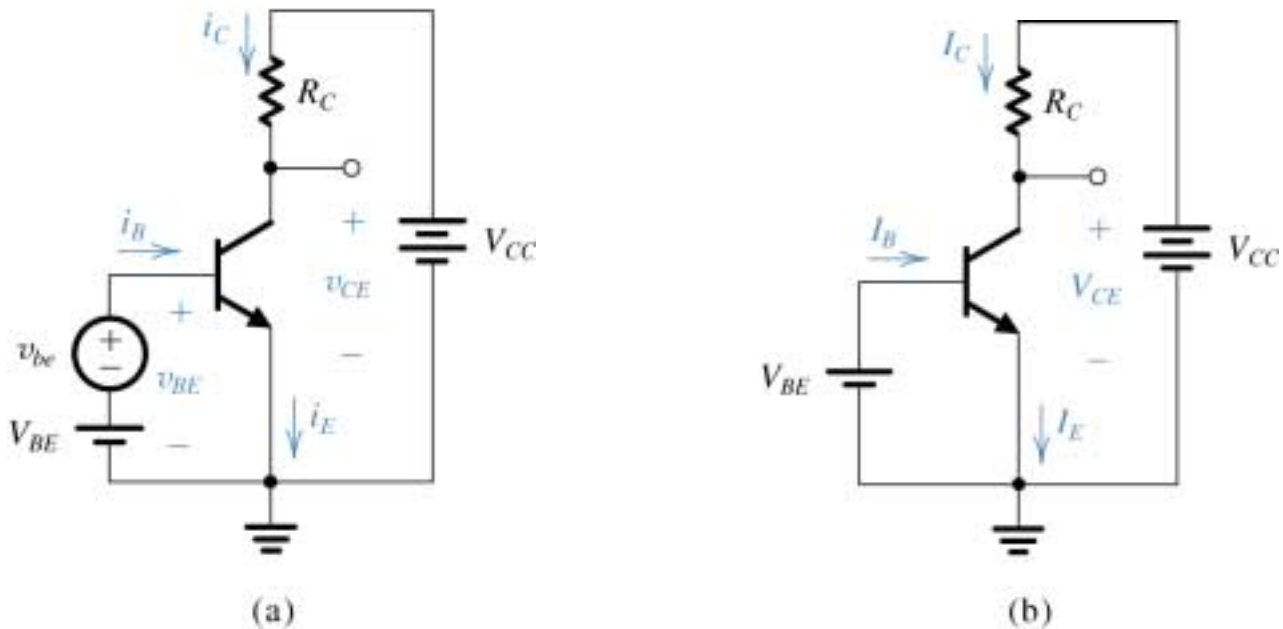


The i_C-v_{CB} characteristics for an npn transistor in the active mode.



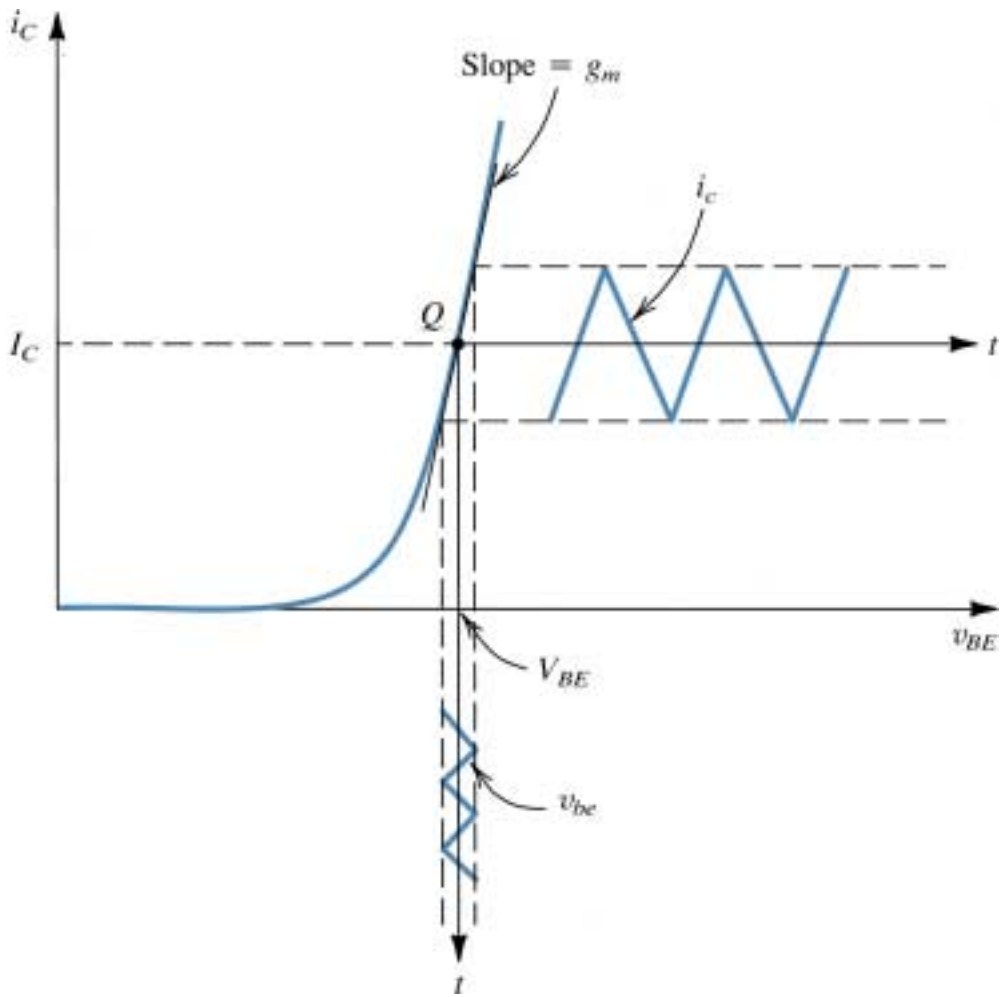
(a) Conceptual circuit for measuring the i_C-v_{CE} characteristics of the BJT.

(b) The i_C-v_{CE} characteristics of a practical BJT.

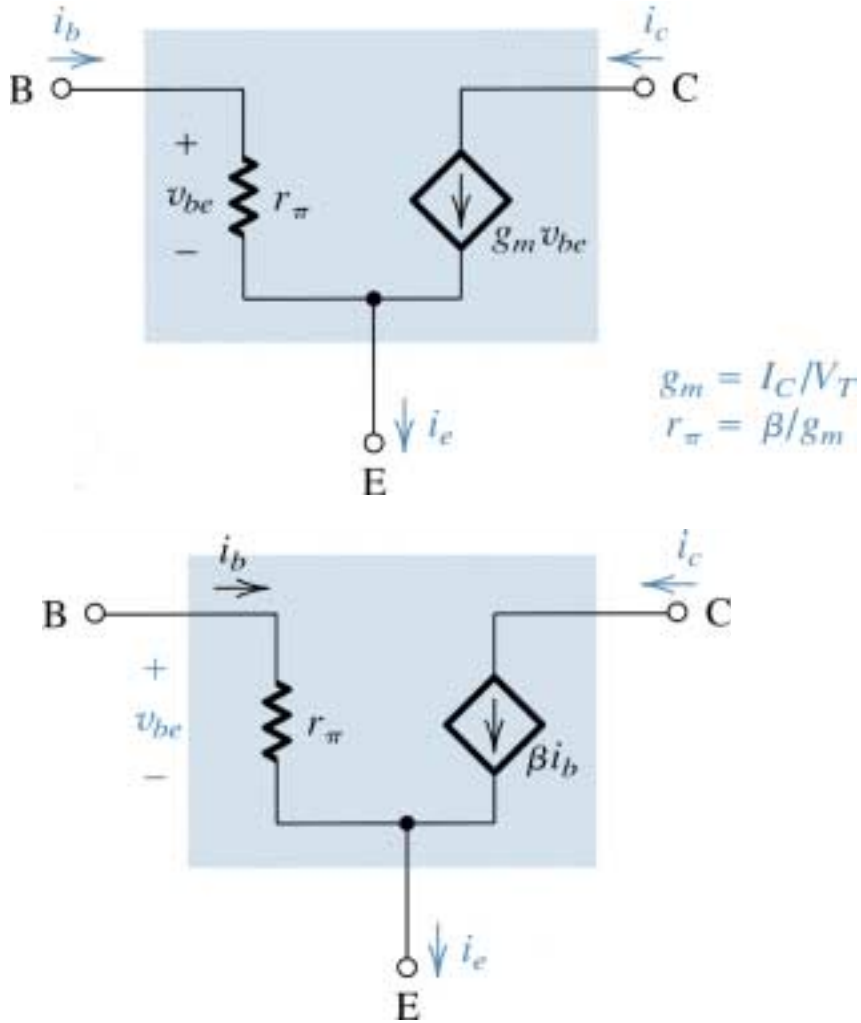


(a) Conceptual circuit to illustrate the operation of the transistor of an amplifier.

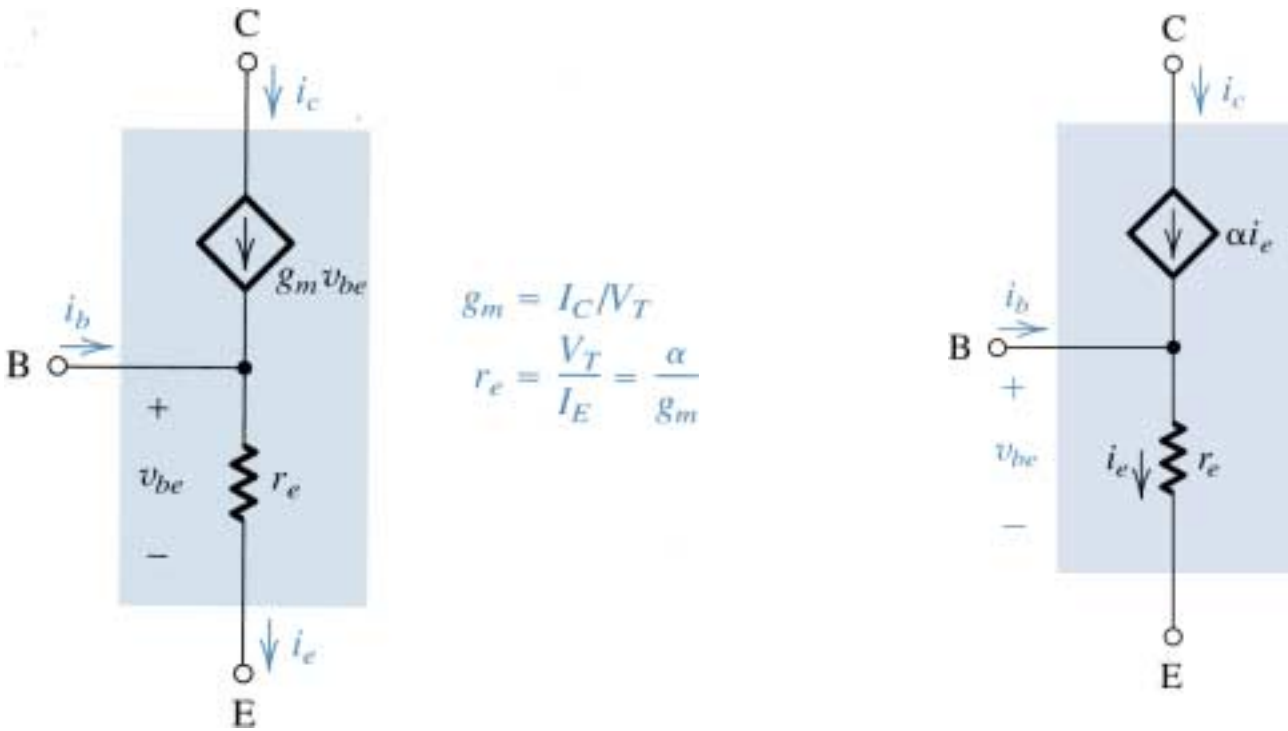
(b) The circuit of (a) with the signal source v_{be} eliminated for dc (bias) analysis.



Linear operation of the transistor under the small-signal condition: A small signal v_{be} with a triangular waveform is superimpose din the dc voltage V_{BE}. It gives rise to a collector signal current i_c, also of triangular waveform, superimposed on the dc current I_C. $I_c = g_m v_{be}$, where g_m is the slope of the i_c - v_{BE} curve at the bias point Q.

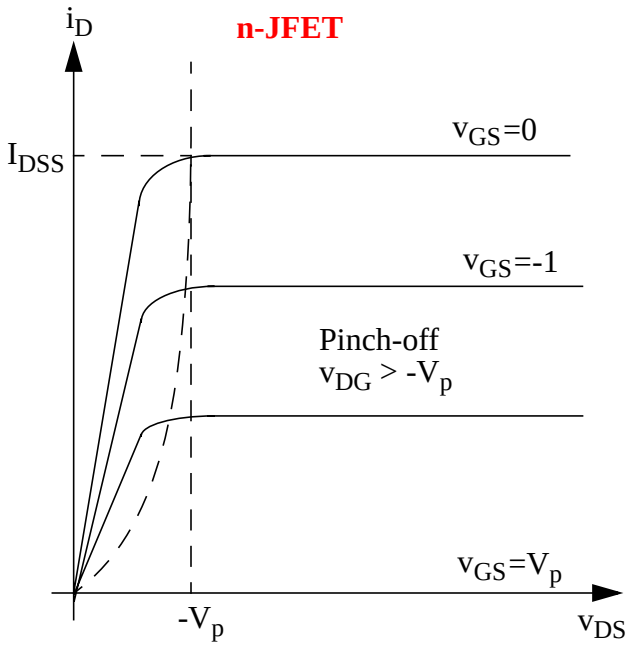


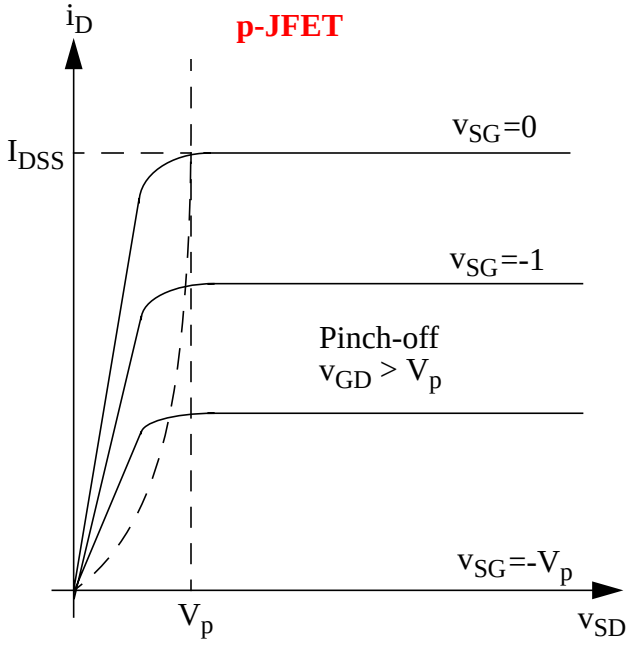
Two slightly different versions of the simplified hybrid-Π model for the small-signal operation of the BJT. The equivalent circuit in **(a)** represents the BJT as a voltage-controlled current source (a transconductance amplifier) and that in **(b)** represents the BJT as a current-controlled current source (a current amplifier).



Two slightly different versions of what is known as the *T model* of the BJT. The circuit in **(a)** is a voltage-controlled current source representation and that in **(b)** is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_Π featured in the hybrid-π model.

Junction Field-Effect Transistors





Junction Field-Effect Transistors

Triod (VCR) Region

$$i_D = I_{DSS}\left[2\left(1-\frac{v_{GS}}{V_p}\right)\left(\frac{v_{DS}}{-V_p}\right)-\left(\frac{v_{DS}}{V_p}\right)^2\right]$$

$$r_{DS} = \left.\frac{v_{DS}}{i_D}\right]_{v_{DS}\,=\,small} = \left[\frac{2I_{DSS}}{-V_p}\left(1-\frac{v_{GS}}{V_p}\right)\right]^{-1}$$

Boundary

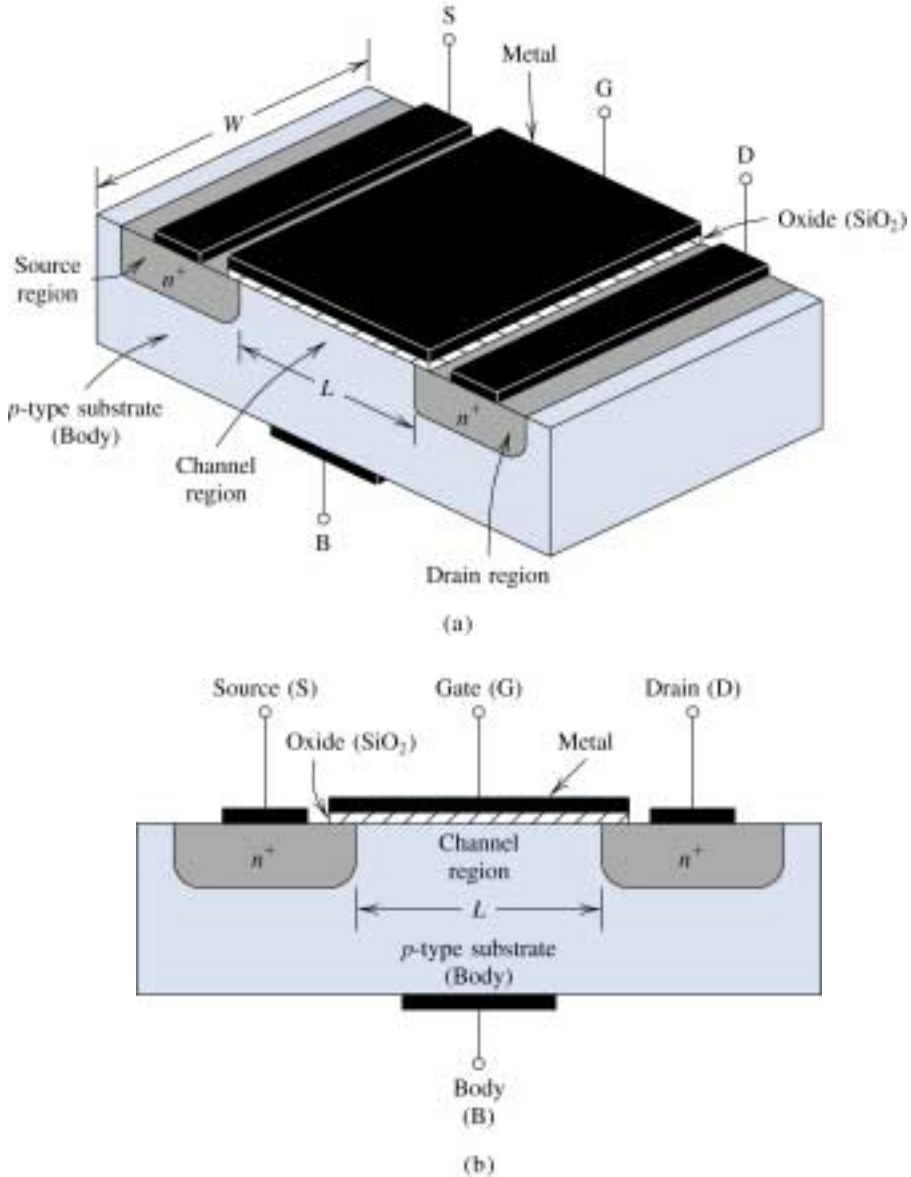
$$v_{DG} = -V_p$$

$$i_D = I_{DSS}\left(\frac{v_{DS}}{V_p}\right)^2$$

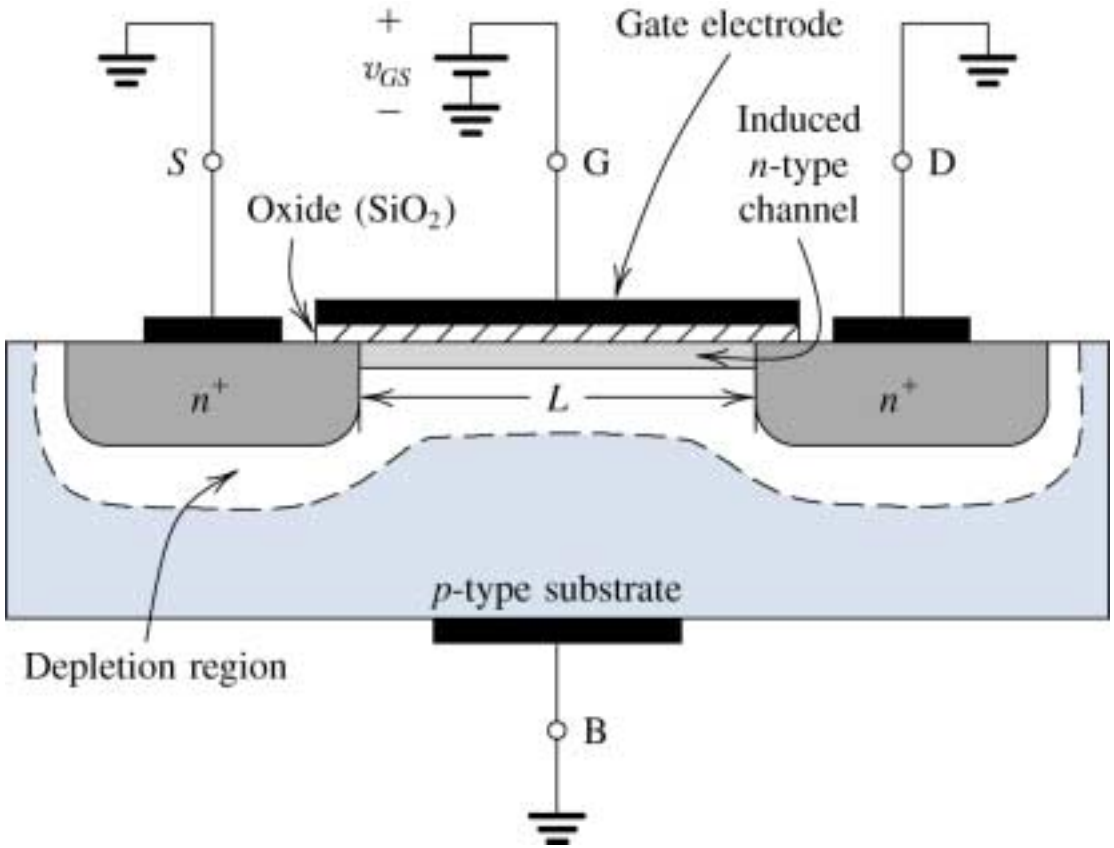
Pinch-Off Region

$$i_D = I_{DSS}\left(1-\frac{v_{GS}}{V_p}\right)^2$$

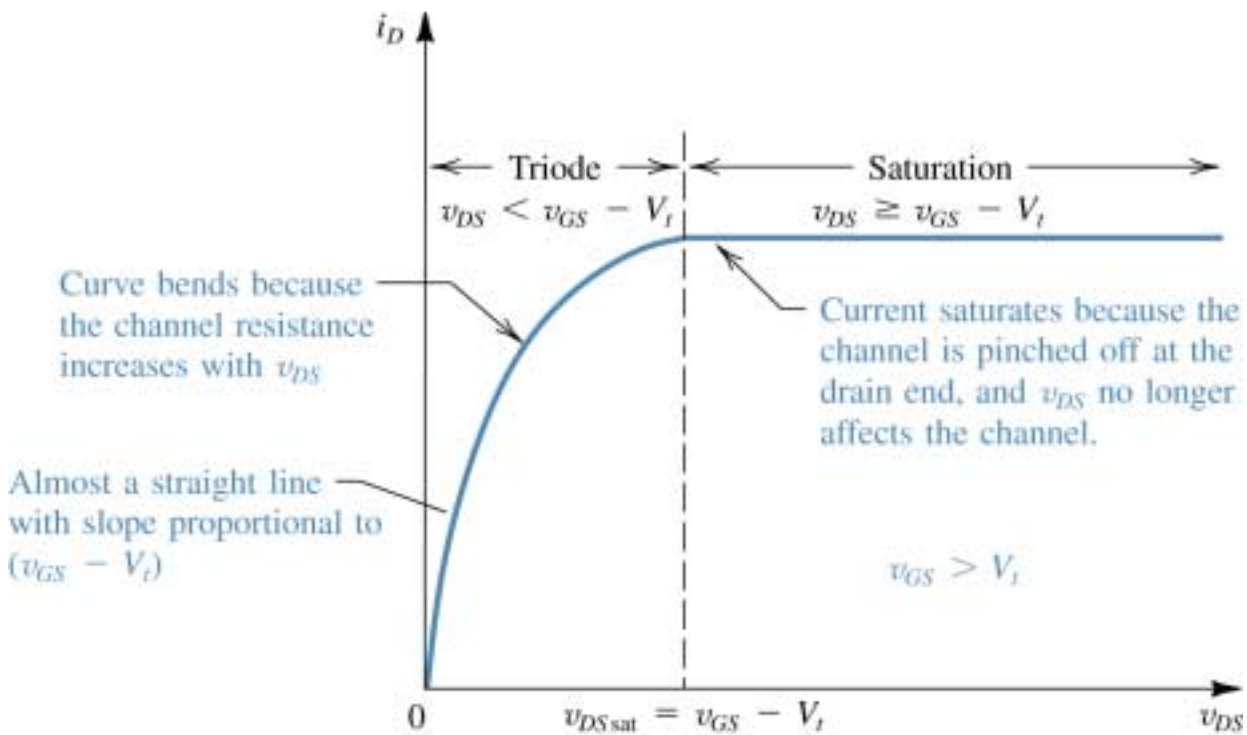
MOSFETs



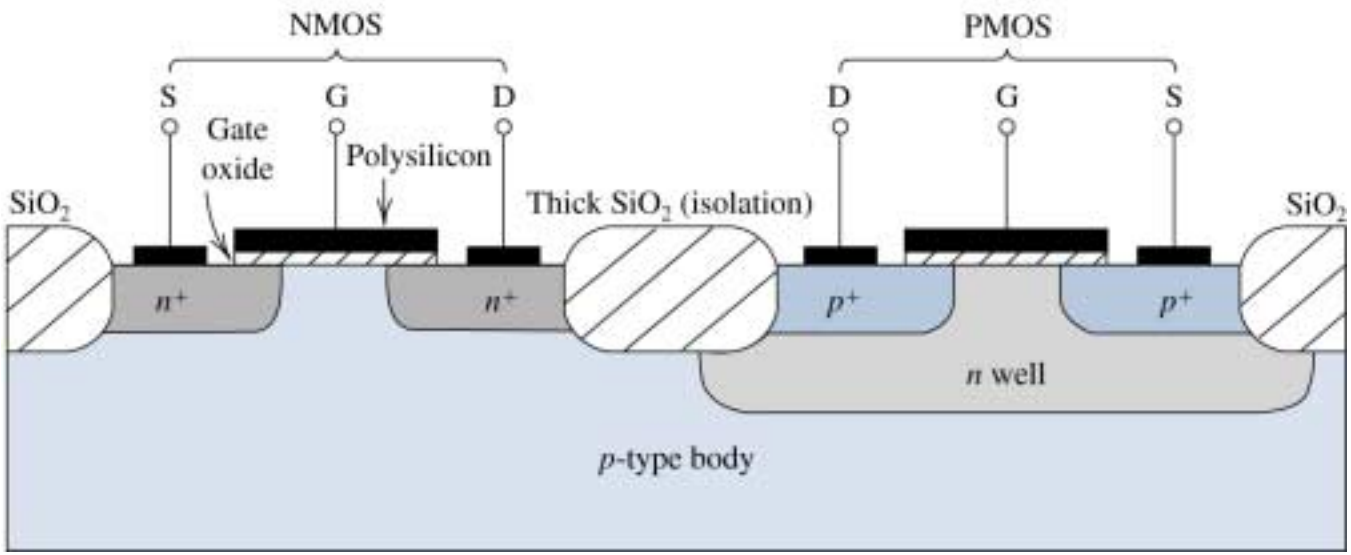
Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically L = 1 to 10 μm, W = 2 to 500 μm, and the thickness of the oxide layer is in the range of 0.02 to 0.1 μm.



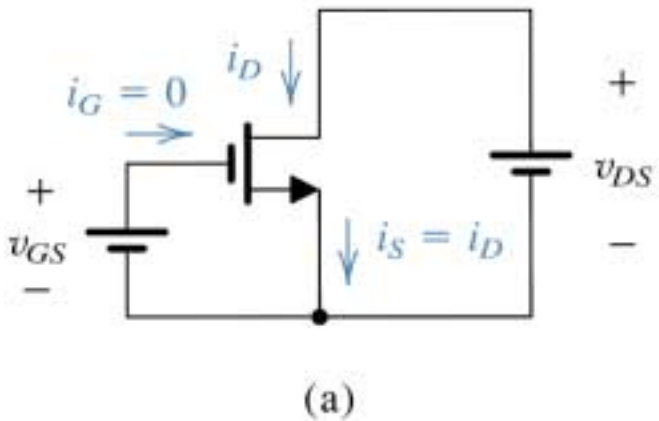
The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

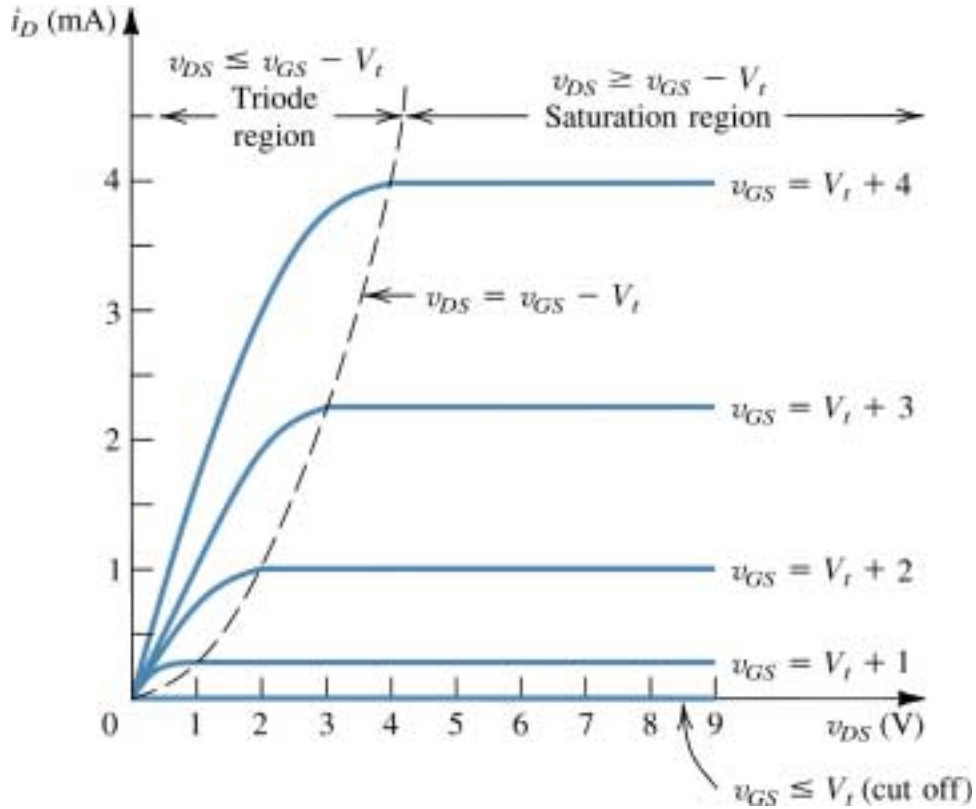


The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

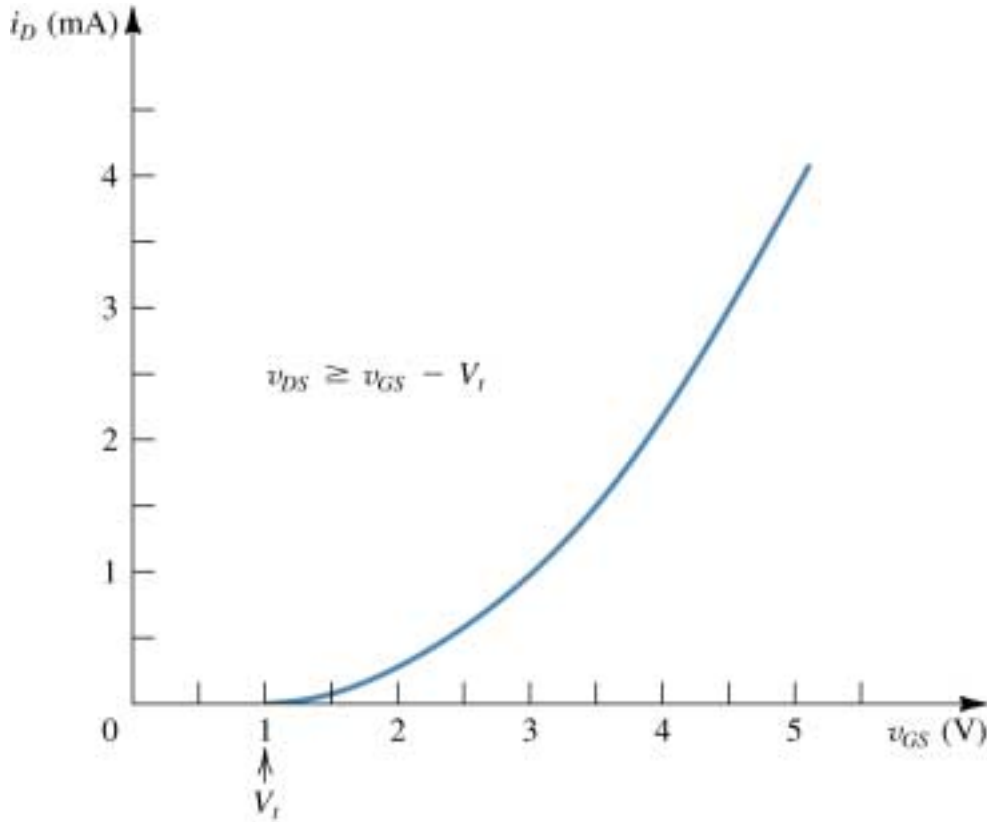


Cross section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well.

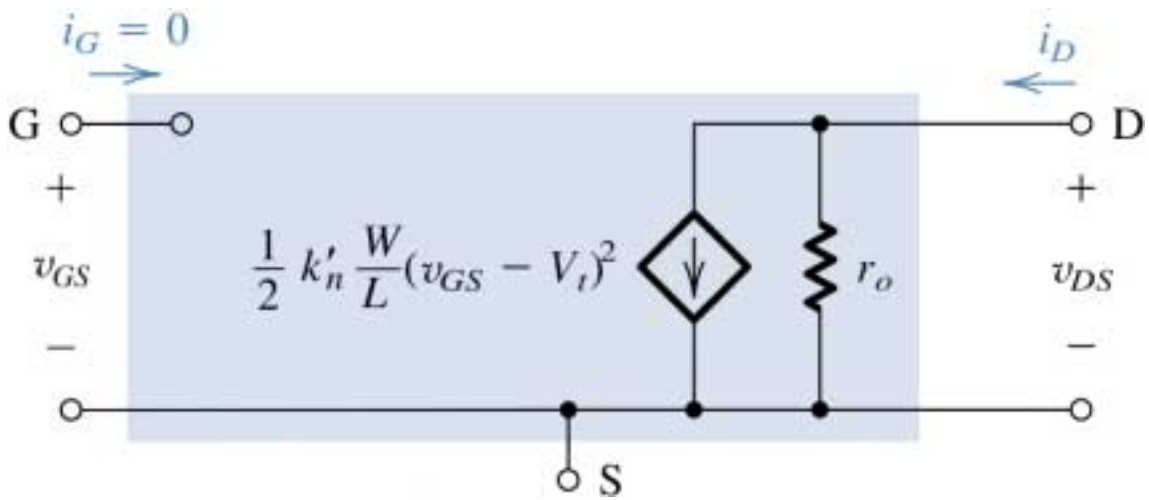




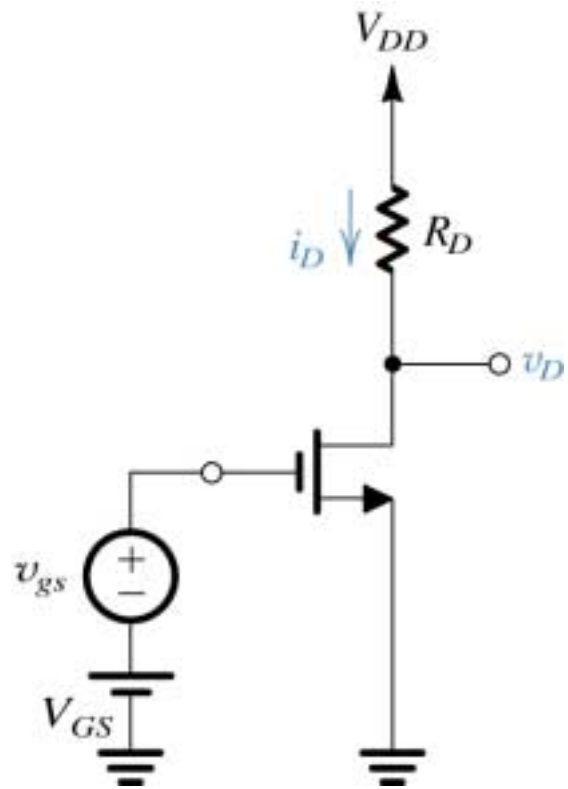
(a) An n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D - v_{DS} characteristics for a device with V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2.



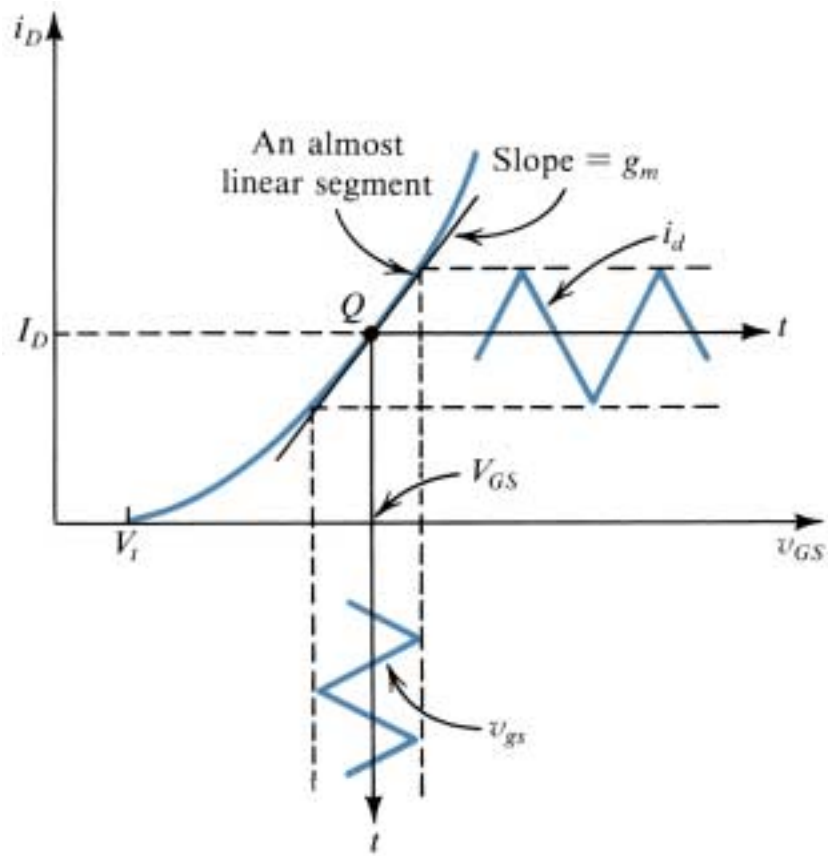
The i_D - v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2).



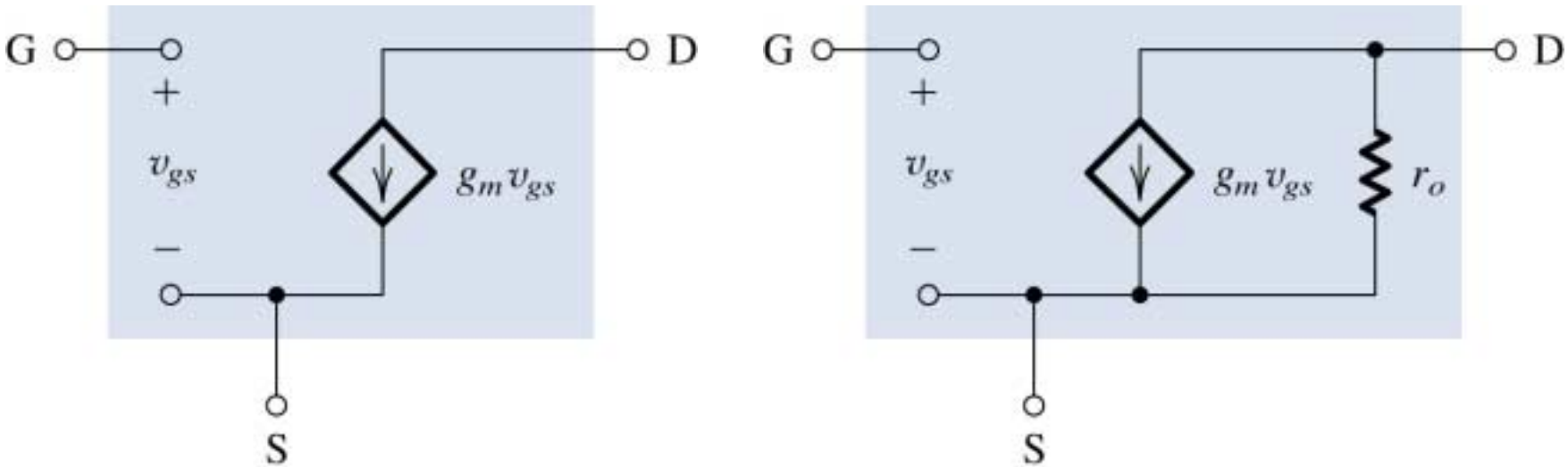
Large-signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by $r_o \cong V_A/I_D$.



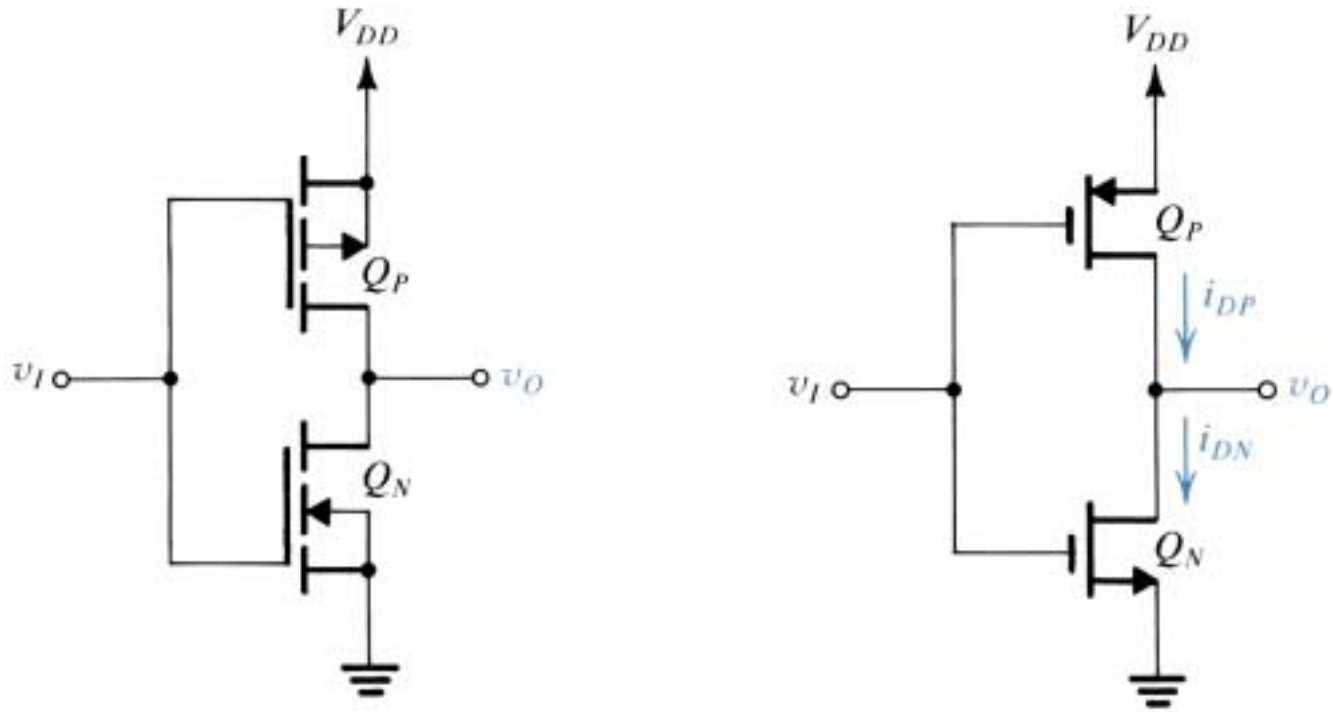
Conceptual circuit utilized to study the operation of the MOSFET as an amplifier.



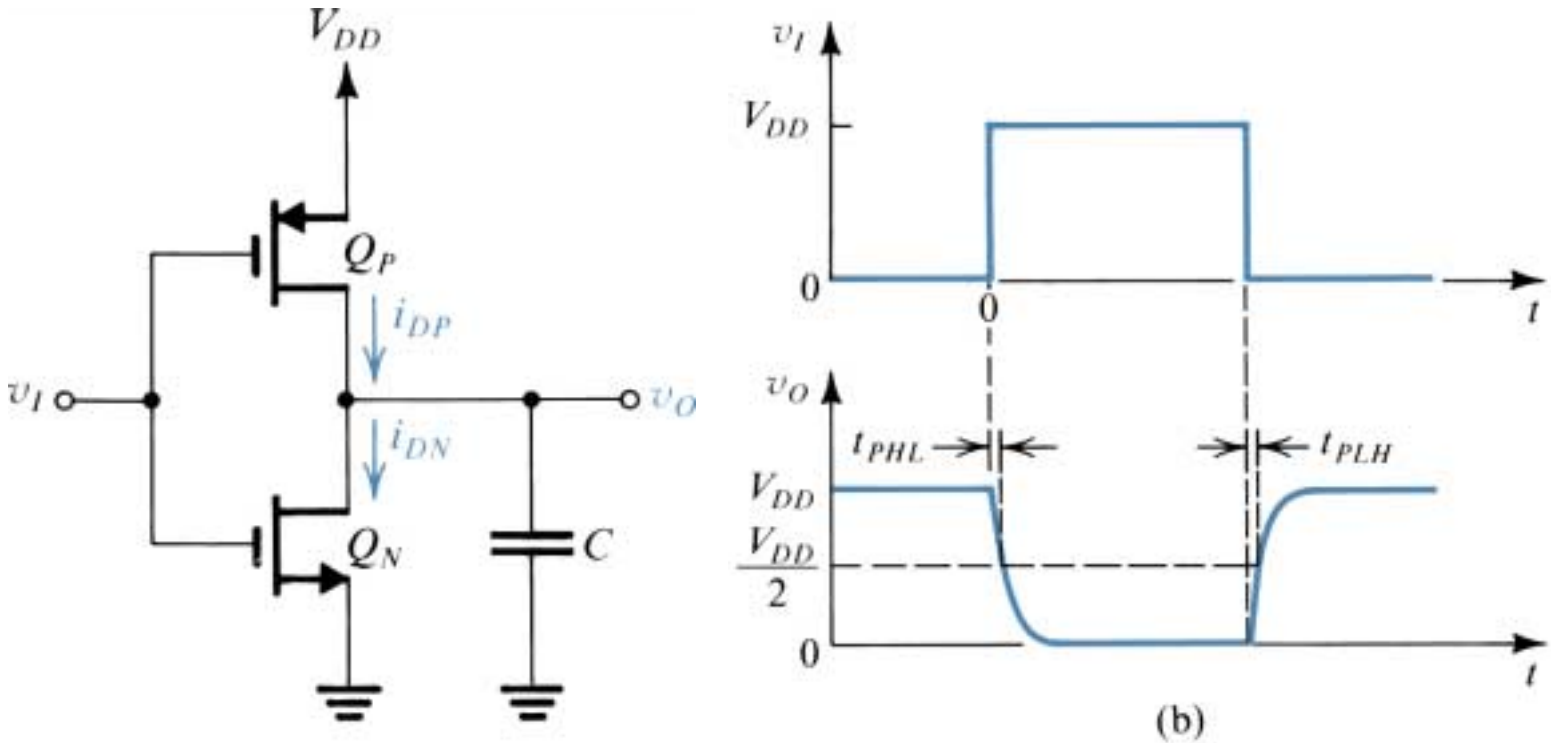
Small-signal operation of the enhancement MOSFET amplifier.



Small-signal models for the MOSFET: **(a)** neglecting the dependence of i_D on v_{DS} in saturation (channel-length modulation effect); and **(b)** including the effect of channel-length modulation modeled by output resistance $r_o = |V_A|/I_D$.



(a) The CMOS inverter. (b) Simplified circuit schematic for the inverter.



Dynamic operation of a capacitively loaded CMOS inverter: (a) circuit; (b) input and output waveforms.