**Circuit Layout Techniques And Tips (Part III of VI)**

*by Bonnie C. Baker and Ezana Haile, Microchip Technology Inc.*

The major classes of parasitic generated by the PC board layout come in the form of resistors, capacitors and inductors. For instance, PCB resistors are formed as a result of traces from component to component, unintentional capacitors can be built into the board with traces, soldering pads and parallel traces, and circumstances that surround where inductors are built come in the form of loop inductance, mutual inductance and vias. All of these parasitics stand a chance of interfering with the effectiveness of your circuit as you transition from the circuit diagram to the actual PCB. This article quantifies the most troublesome class of board parasitics, the board capacitor, and gives an example of where the effects on circuit performance can be clearly seen.

**Feeling the Pain of Those Unnecessary Capacitors**

In Part II of this series we discussed how capacitors could inadvertently be built into your board and, quickly reviewing this concept, most layout capacitors are built by placing two parallel traces close together. The value of this type of capacitor can be calculated using the formulae shown in Fig. 1 (from Fig. 5 in Part II of this series.)

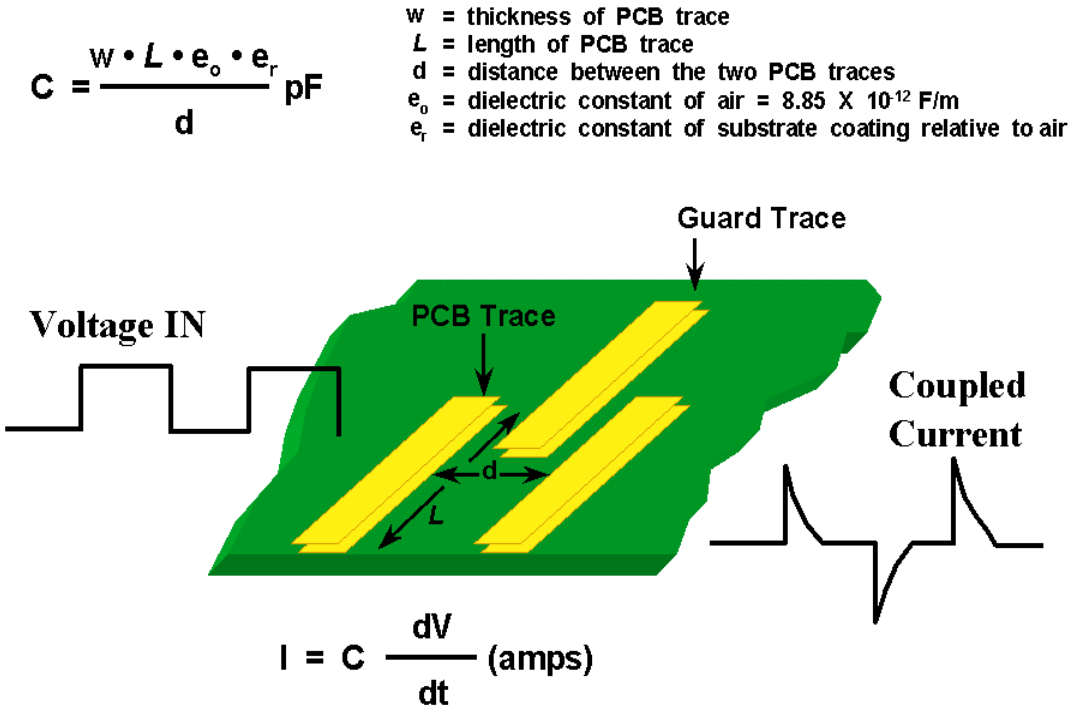


**Fig. 1: Capacitors can easily be fabricated into a PCB by laying out two traces in close proximity. With this type of capacitor, fast voltage changes on one trace can initiate a current signal in the other trace**

This type of capacitor can cause problems in mixed signal circuits where sensitive, high impedance analog traces are in close proximity to digital traces. For example, the circuit in Fig. 2 has the potential to have this type of problem.

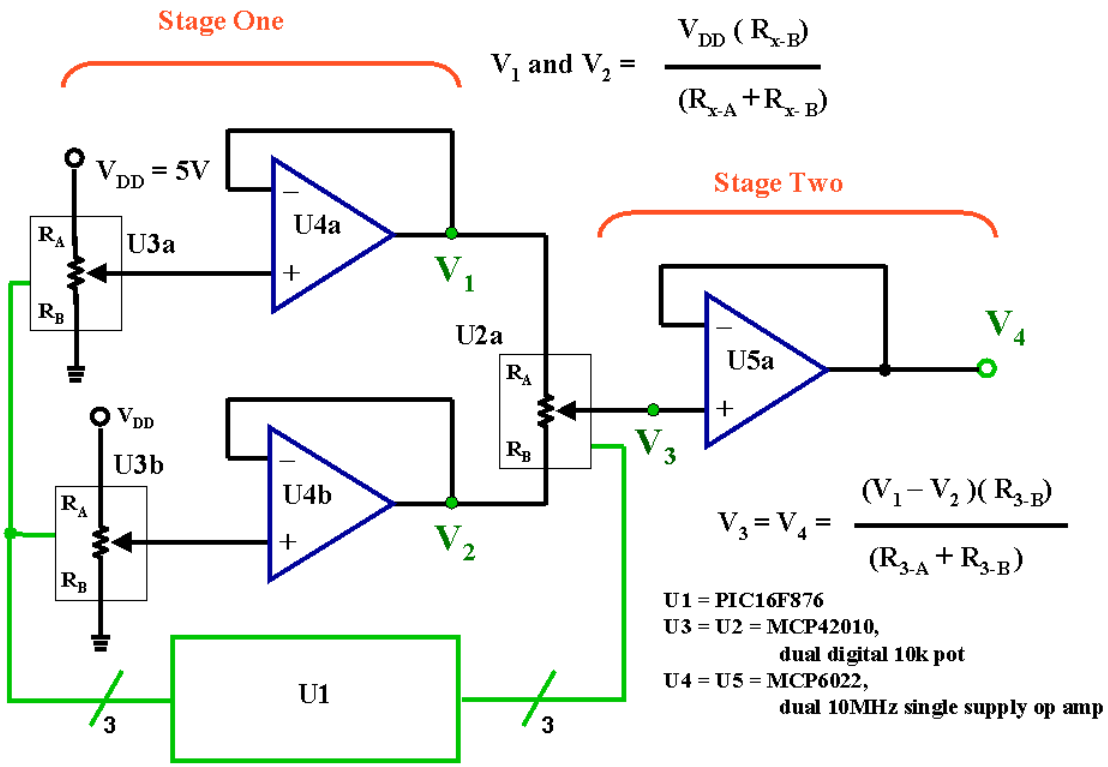


**Fig. 2: A 16-bit DAC can be built using three 8-bit digital potentiometers and three amplifiers to provide 65,536 different output voltages. If $V_{DD}$ is 5V in this system the resolution or LSB size of this DAC is 76.3µV**

To quickly explain the circuit operation in Fig. 2, a 16-bit DAC is built using three 8-bit digital potentiometers and three CMOS operational amplifiers. To the left side of this figure, two digital potentiometers ($U3_a$ and $U3_b$) span across $V_{DD}$ to ground with the wiper output connected to the non-inverting input of two amplifiers ($U4_a$ and $U4_b$). The digital potentiometers, $U_2$ and $U_3$ are programmed using an SPI interface between the microcontroller, $U_1$. In this configuration, each digital potentiometer is configured to operate as an 8-bit multiplying DAC. If $V_{DD}$ is equal to 5 V the LSB size of these DACs is equal to 19. 61 mV.

The wipers of each of these two digital potentiometers are connected to the non-inverting inputs of two buffer-configured operational amplifiers. In this configuration the inputs to the amplifiers are high impedance, which isolates the digital potentiometers from the rest of the circuit. These two amplifiers are also configured so that output swing restrictions on the amplifiers in the second stage aren't violated.

To have this circuit perform as a 16-bit DAC ($U2_a$), a third digital potentiometer spans across the output of these two amplifiers, $U4_a$ and $U4_b$. The programmed setting of U3a and U3b sets the voltage across the digital potentiometer. Again, if $V_{DD}$ is 5V it is possible to program the output of $U3_a$ and $U3_b$ 19.61 mV apart. With this size of voltage across the third 8-bit digital potentiometer, $R_3$, the LSB size of this circuit from left to right is 76.3 µV. The critical device specifications that will give optimum performance with this circuit are given in Table 1.

| Device | Specification | | Purpose |
|---|---|---|---|
| Digital Potentiometers (MCP42010) | Number of bits | 8-bits | Determines the overall LSB size and resolution of the circuit. |
| | Nominal resistance (resistive element) | 10 kΩ (typ) | The lower this resistance is the lower the noise contribution will be to the overall circuit. The trade off is that the current consumption of the circuit is high with these lower resistances. |
| | DNL | ±1LSB (max) | Good Differential Non-Linearity is needed to insure no missing codes occur in this circuit which allows for a possible 16-bit operation. |
| | Voltage Noise Density (for half of the resistive element) | 9 nV/√Hz @ 1 kHz (typ) | If the noise contribution of these devices is too high it will take away from the ability to get 16-bit noise free performance. Selecting lower resistive elements can reduce the digital potentiometer noise. |
| Operational Amplifiers (MCP6022) | Input Bias Current, $I_B$ | 1 pA @ 25 °C (max) | Higher $I_B$ will cause a dc error across the potentiometer. CMOS amplifiers were chosen for this circuit for that reason. |
| | Input Offset Voltage | 500 µV (max) | A difference in amplifier offset error between $A_1$ and $A_2$ could compromise the DNL of the overall system. |
| | Voltage Noise Density | 8.7 nV/√Hz @10 kHz (typ) | If the noise contribution of these devices is too high it will take away from the ability to get 16-bit accurate performance. Selecting lower noise amplifiers can reduce amplifier noise. |

**Table 1: From the long list of specifications that each of the devices have, there are a handful that make this circuit more successful when it is used to provide dc reference voltages or arbitrary wave forms**

This circuit can be used in two basic modes of operation. The first would be if you wanted a programmable, adjustable, dc reference where the digital portion of the circuit is only used occasionally and certainly not during normal operation. The second would be as an arbitrary wave generator when the digital portion of the circuit is an intimate part of the circuit operation and the risk of capacitive coupling may occur.

The first pass layout of the circuit in Fig. 2 is shown in Fig. 3. This circuit was quickly designed in our lab without attention to detail. The consequences of placing digital traces next to high impedance analog lines were overlooked in the layout review. This speaks strongly to doing it right the first time, but is to our benefit in this article to illustrate how to identify the problems and make significant improvements.

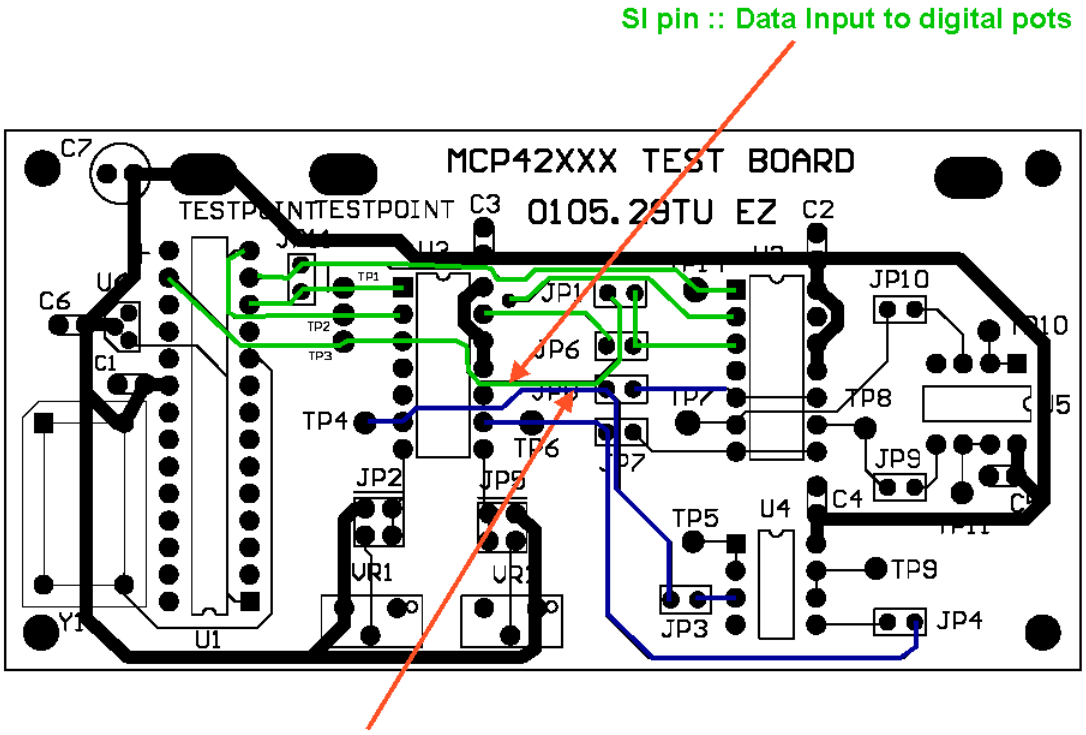


**Fig. 3: This is the first attempt at layout for the circuit in Fig. 2. It can be seen that a critical high impedance analog line is very close to a digital trace. This configuration produces inconsistent noise on the analog line because the data input code on that particular digital trace changes, dependent on the programming requirements for the digital potentiometer**

Taking a look at the color-coding in this layout it is obvious where a potential problem is. The analog trace (blue) that is pointed out goes from the wiper of U3a to the high impedance amplifier input of U4a. The digital trace (green) that is pointed out carries the digital word that programs the digital potentiometer settings.

On the bench, it is found that the digital signal on the green trace is coupled into the sensitive blue trace. This is illustrated in Fig. 4.

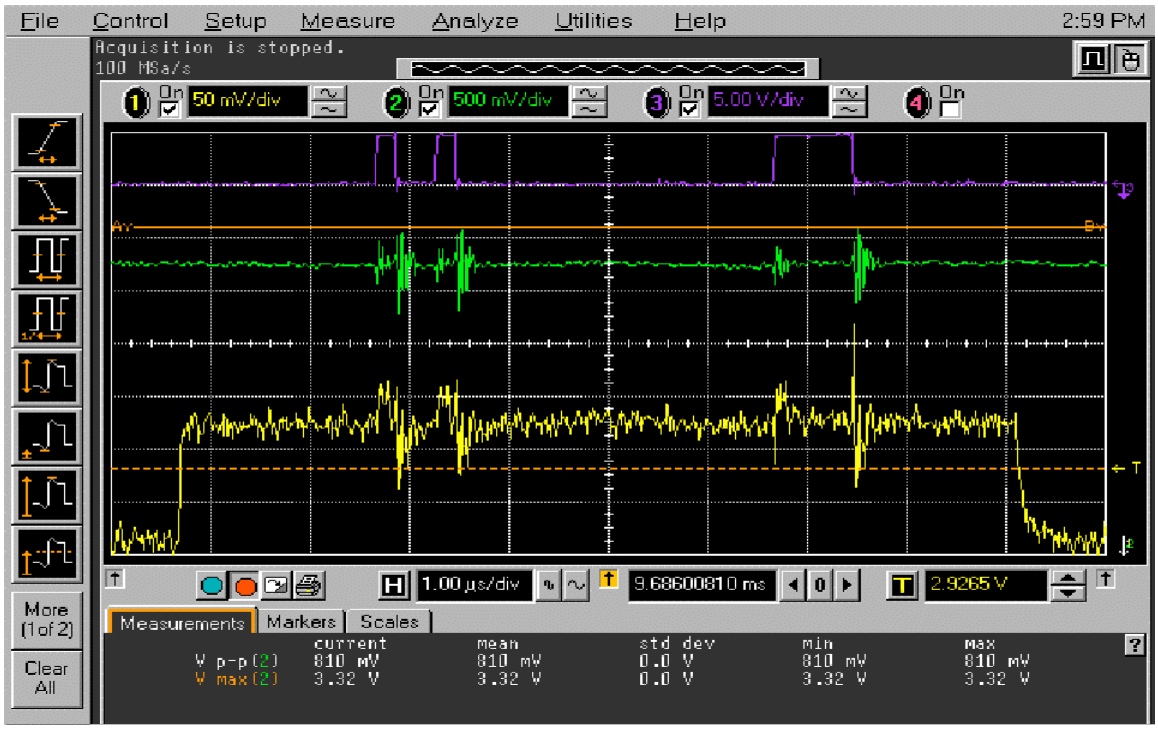


**Fig. 4: In this scope photo, the upper trace was taken at JP1 (digital word to the digital potentiometers), the middle trace on JP5 (noise on the adjacent analog trace) and the lower yellow trace is at TP10 (noise at the output of the 16-bit DAC)**

The digital signal that is programming the potentiometers in the system has transmitted from trace-to-trace onto an analog line that is being held at a dc voltage. This noise propagates through the analog portion of the circuit all the way out to the third digital potentiometer (U5a) which is toggling between two output states.

What is the solution to this problem? Basically we separated the traces.

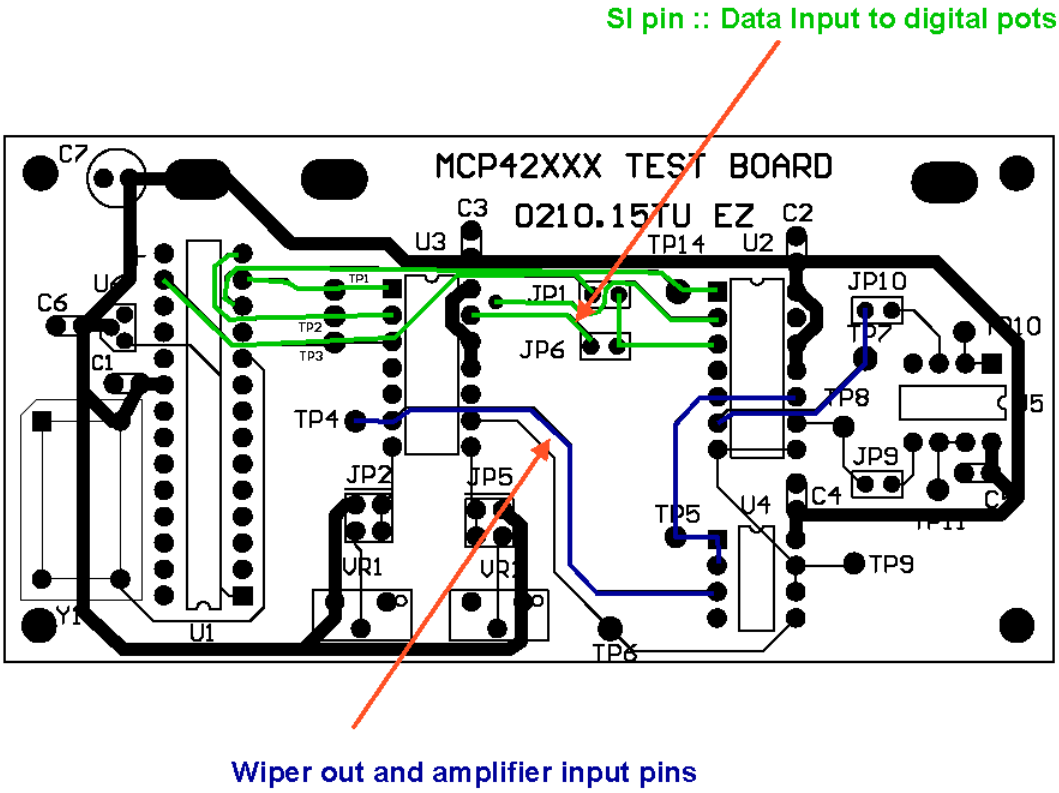


**Fig. 5: With this new layout the analog and digital lines have been separated**

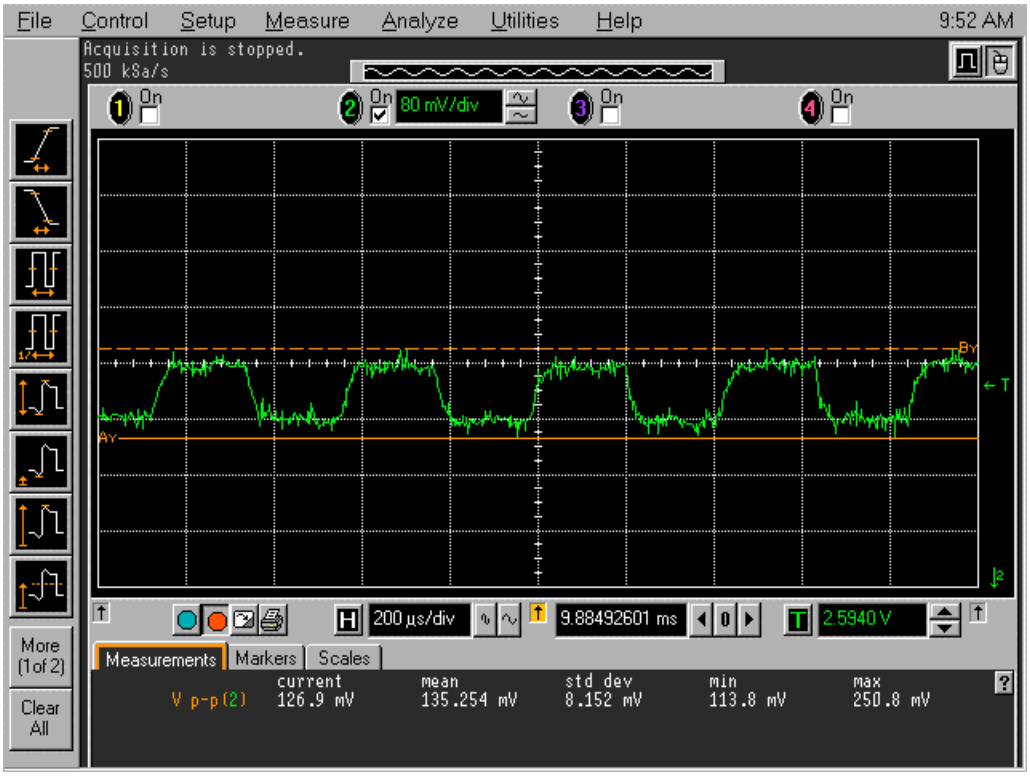


**Fig. 6: With the new layout a single code transition shows no digital noise**

The results of the layout change are shown in Fig. 6. With the analog and digital traces carefully kept apart this circuit becomes a very clean 16-bit DAC. A single code transition of the third digital potentiometer 76.29 µV is shown with the green trace. You may notice that the oscilloscope scale is 80 mV/div and that the amplitude of this code change is shown to be approximately 80 mV. In the lab, we were forced by the equipment to gain the output of the 16-bit DAC by 1000x.

**Conclusion**

Once again, when the digital and analog domains meet careful layout is critical if you intend to have a successful final PCB implementation. In particular active digital traces close to high impedance analog traces will cause serious coupling noise that can only be avoided with distance between traces.

as published in...
analog ZONE