

Circuit Layout Techniques And Tips (Part V of VI)

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The Trouble With Troubleshooting Your Layout Without The Right Tools

When you're trying to solve a signal integrity problem the best of all worlds is to have more than one tool to examine the behavior of a system. If there is an ADC in the signal path there are three fundamental issues that can easily be examined when assessing the circuit's performance. All three of these methods evaluate the conversion process, as well as its interaction with the layout and other portions of the circuit. The three areas of concern encompass the use of frequency-analysis (FFT), time-analysis, and dc-analysis techniques. This part will explore the use of these tools to identify the source of problems as they relate to the layout implementation of circuits: How you decide what to look for, where to look, how to verify problems through testing, and how to solve the problems.

This is the circuit (Fig. 1) that was built and used in the discussion that follows.

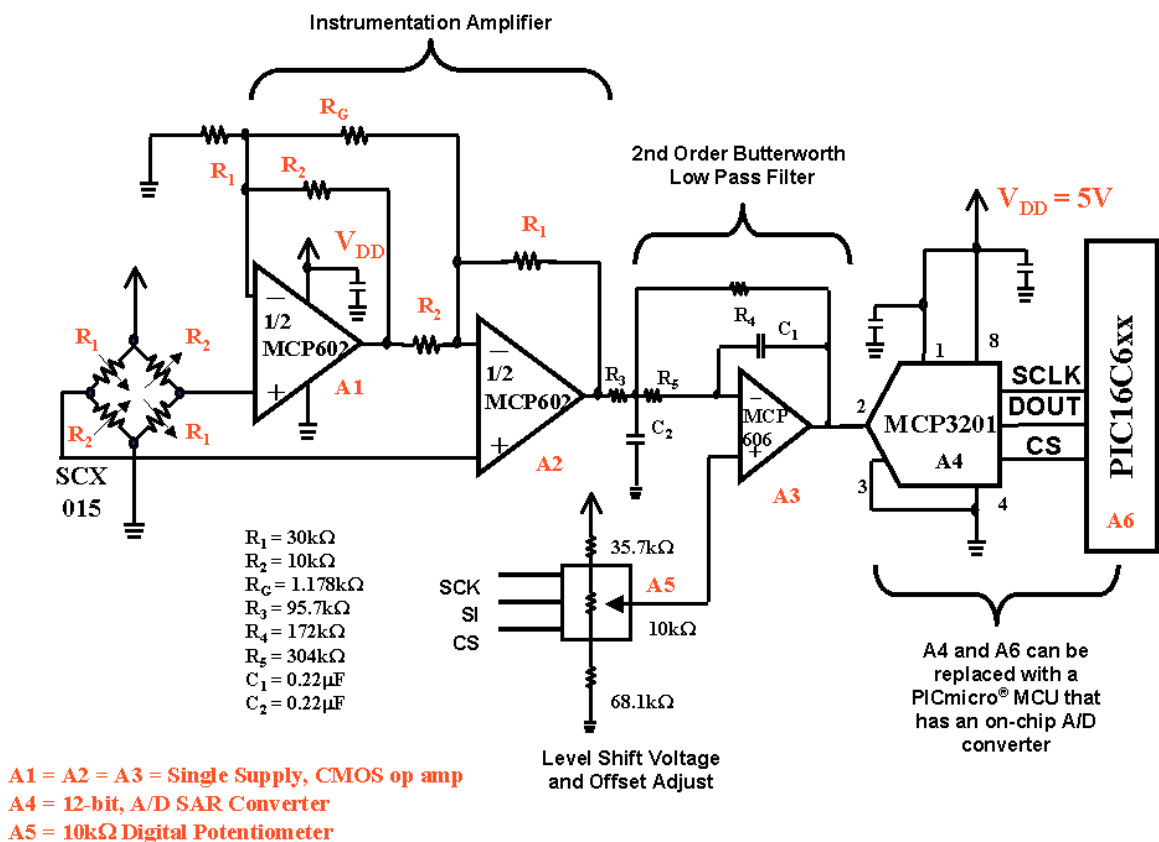


Fig. 1: The Instrumentation Amplifier (A1/A2) Gains The Voltage At The Output Of The SCX015 Pressure Sensor And The Following Low-Pass Filter (A3) Eliminates Aliased Noise From The 12-bit ADC Conversion

Power Supply Noise

A common source of interference in circuits is from the power supply, typically injected through the power supply pins of the active devices. For instance, a time-based plot of the output of the ADC in Fig. 1 is shown in Fig. 2, where the sample speed was 40 ksample/s and 4096 samples were taken.

In this case the instrumentation amplifier, voltage reference and ADC do not have bypass capacitors installed. Additionally, the inputs to the circuit are both referenced to a low noise dc voltage source of 2.5V.

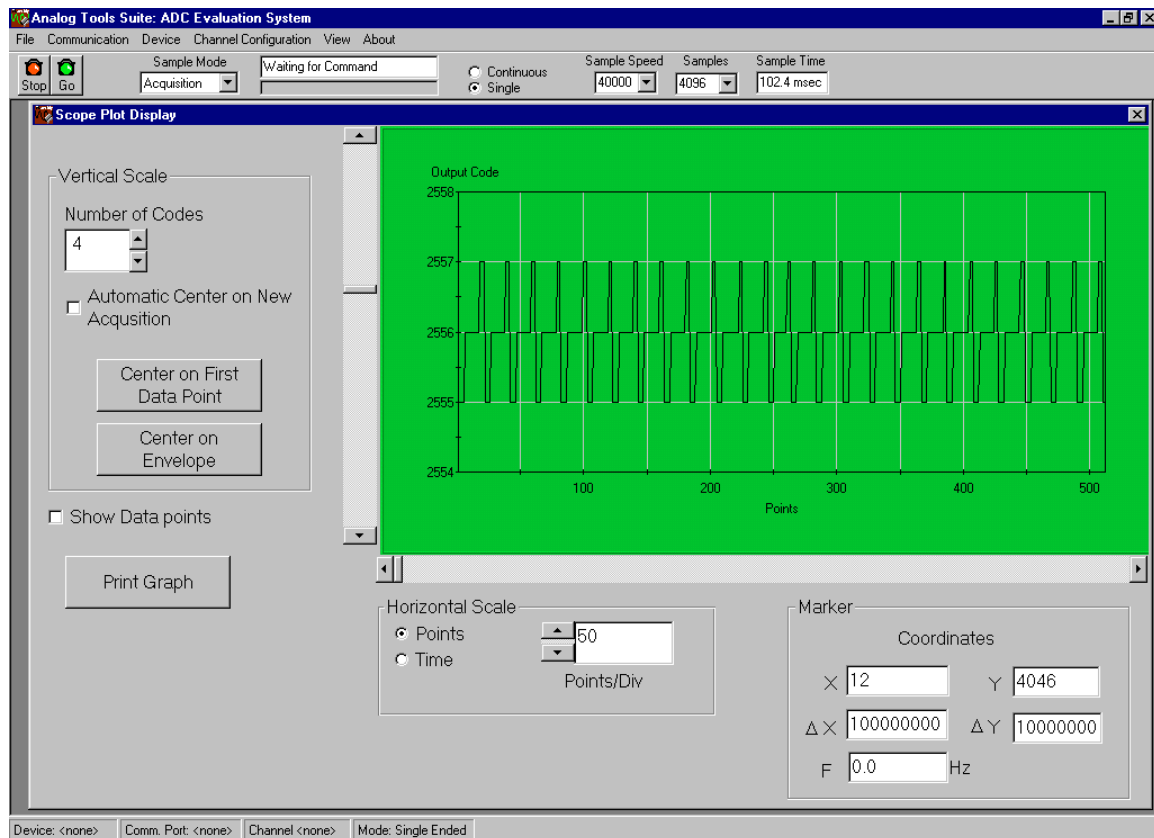


Fig. 2: The Time Domain Representation Of This Data From The MCP3201 (12-bit ADC) Produces An Interesting Periodic Signal - Traced Back To The Power Supply

Further investigations into the circuit show that the source of the noise seen on the time plot comes from the switching power supply. An inductive choke is added to the circuit along with bypass capacitors - one 10 μF is positioned at the power supply and three 0.1 μF capacitors are placed as close to the supply pins of the active elements as possible. Now the generation of a new time plot seems to produce a solid dc output and this is verified with the histogram results (see Fig. 3.) The data show that these changes eliminated the noise source from the signal path of the circuit.

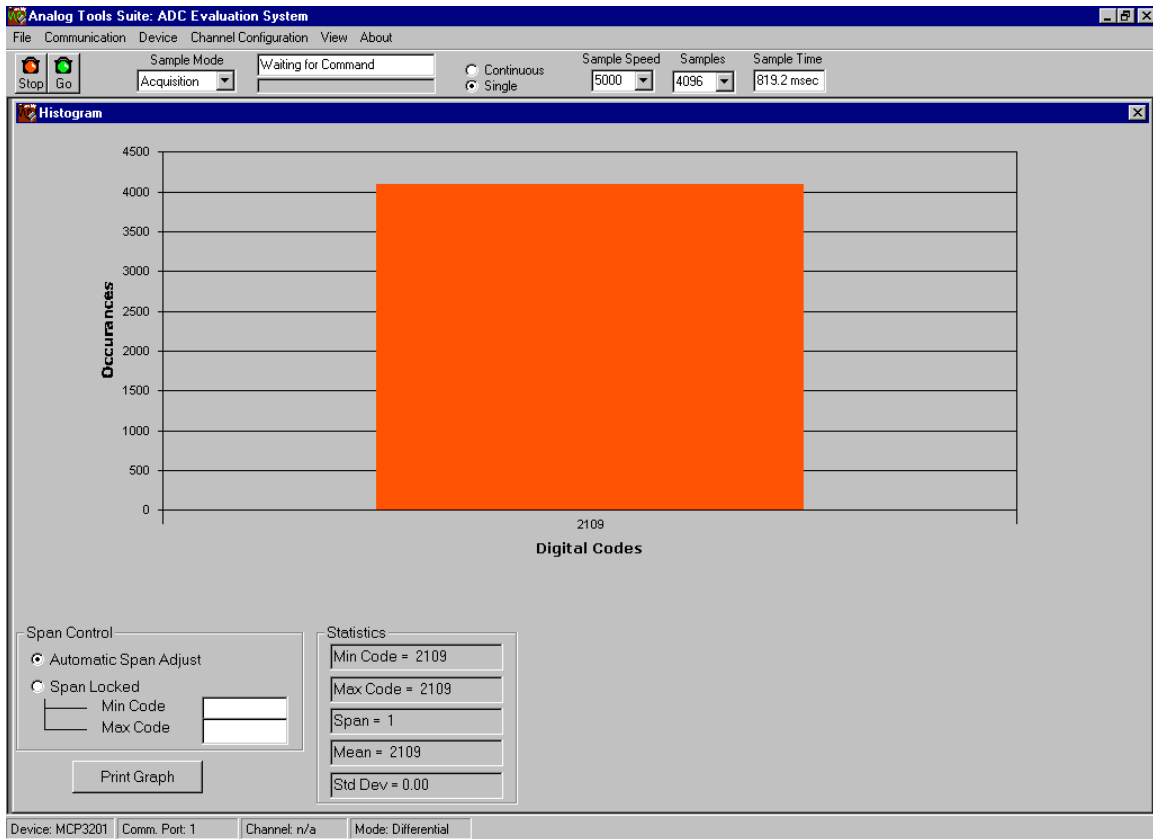


Fig. 3: With Power Supply Noise Sufficiently Reduced, Output Code Of The MCP3201 Is Consistently 2109

Interfering External Clocks

Another source of systematic noise can come from clock sources or digital switching in the circuit. If this type of noise is correlated with the conversion process, it won't appear as interference in the conversion, but if it is not correlated it can easily be found with FFT analysis.

An example of clocking signal interference is shown in the FFT plot of Fig. 4. With this plot the circuit shown in Fig. 1 is used with the by-pass capacitors installed. The spurs seen in the FFT plot (Fig. 4) are generated by a 19.84 MHz clock signal on the board. In this instance layout has been done with little regard for trace-to-trace coupling. Negligence to this detail appears in the FFT plot.

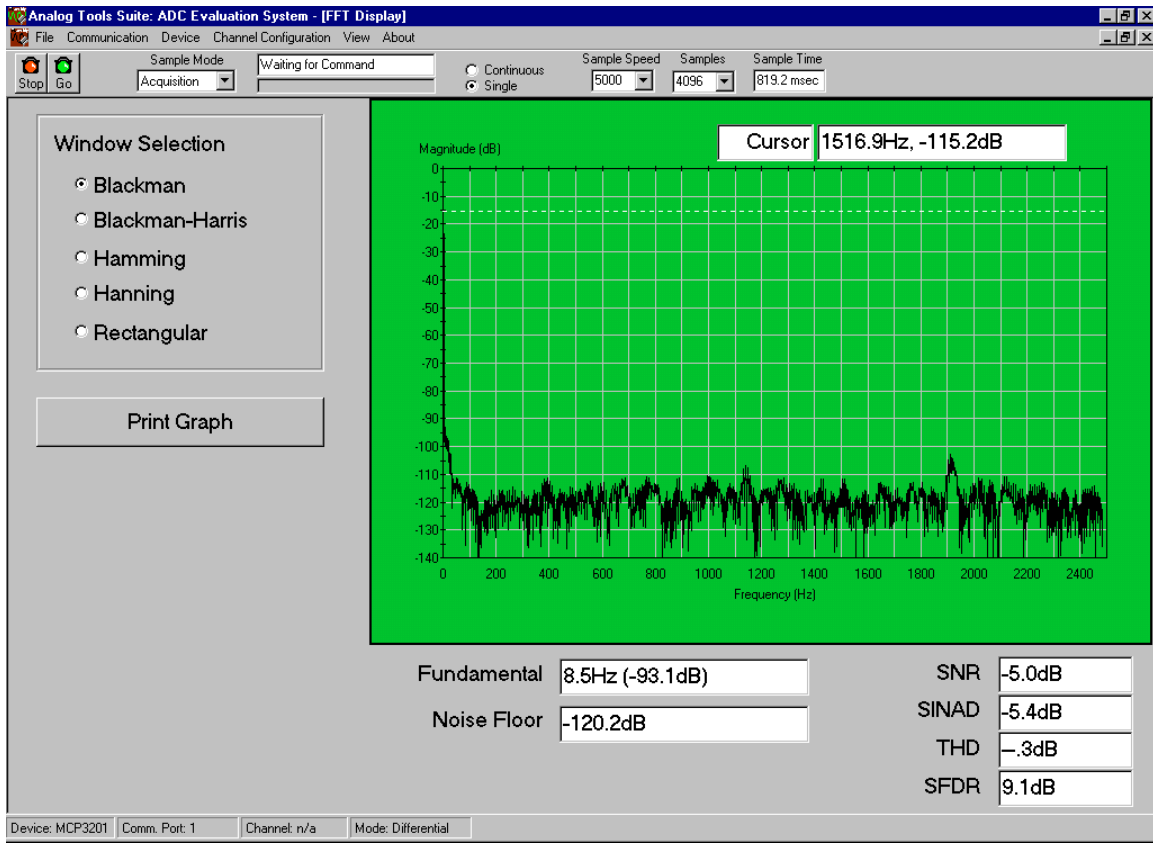


Fig. 4: Digital noise Coupled Into Analog Traces Is Sometimes Misunderstood As Broadband Noise But An FFT Plot Easily Pulls Out This So-Called “Noise” Into An Identifiable Frequency

This problem can be solved by changing the layout to keep high-impedance analog traces away from digital-switching traces, or implementing an anti-aliasing filter in the analog signal path prior to the ADC. Random trace-to-trace coupling is somewhat more difficult to find. In these instances, time domain analysis can be more productive.

Improper Use of Amplifiers

Returning to the circuit (Fig. 1) a 1 kHz ac signal is injected at the positive input to the instrumentation amplifier. (This signal would not be characteristic of this pressure sensing, however this example is used to illustrate the influence of devices in the analog signal path.

The performance of this circuit with the above conditions is shown in the FFT plot of Fig. 5. It should be noted that the fundamental seems to be distorted and there are numerous harmonics with the same distortion. Overdriving the amplifier slightly into the rails causes the distortion and the solution to this problem is to lower the amplifier gain.

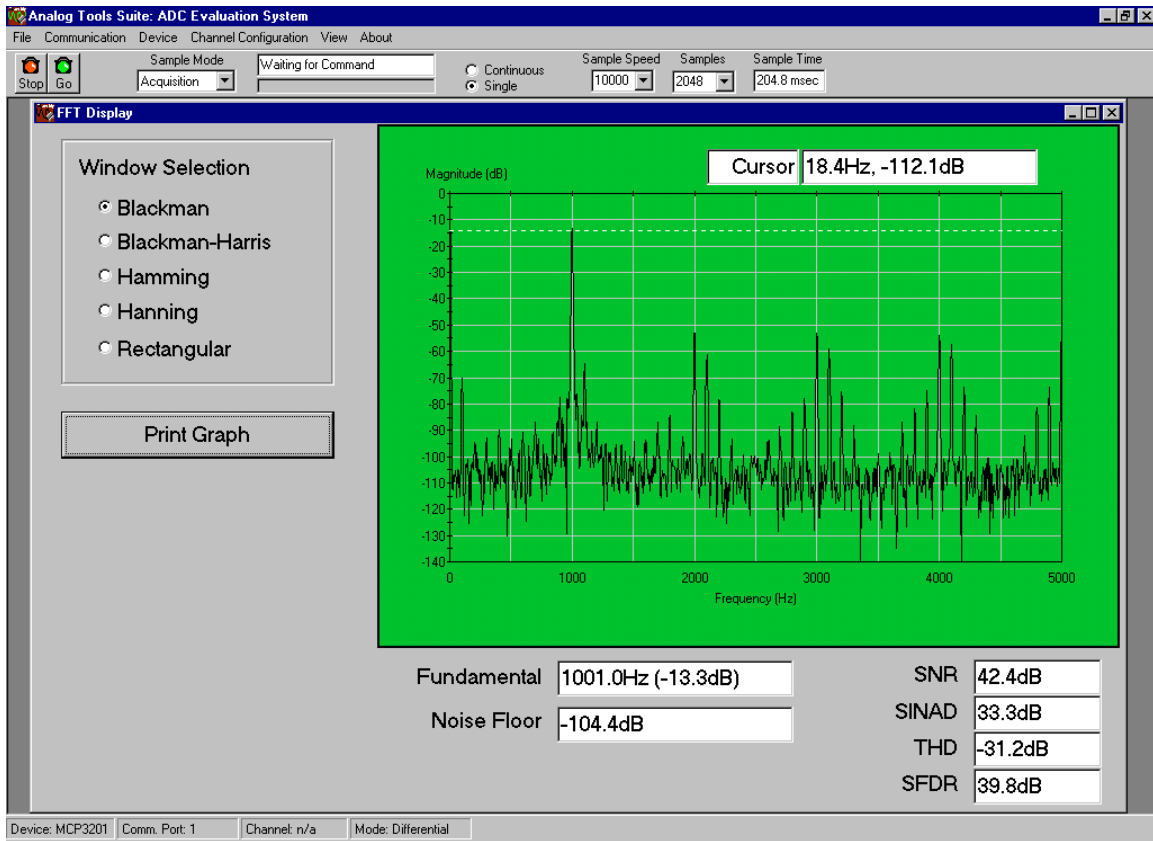


Fig. 5: Slightly Overdriving An Amplifier Can Generate Distortion In The Signal Which An FFT Plot Quickly Points Out

Conclusion

Solving signal integrity problems can take a great deal of time particularly if you don't have the tools to tackle the tough issues. The three best analysis tools to have in your arsenal are frequency-analysis (FFT), time-analysis (scope photo) and dc-analysis (histogram) tools. We used all of these tools to identify the power supply noise, external clock noise, and overdriven amplifier distortion.

