**Circuit Layout Techniques And Tips (Part VI of VI)**
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## Layout Tricks For A 12-Bit Sensing System

When I started writing this article I thought a "cookbook" approach would be appropriate when describing the implementation of a good 12-bit layout. My assumption behind this type of approach was that a reference design could be provided, which would make the layout implementation easy. But I struggled with this topic long enough to find that this notion was fairly unrealistic.

Because of the complexity of this problem, I am going to provide basic guidelines ending with a review of issues to be aware of while implementing your layout design. Throughout this discussion I will offer examples of good and bad layout implementations. I am doing this in the spirit of discussing concepts and not with the intent of recommending one layout as the only one to use.

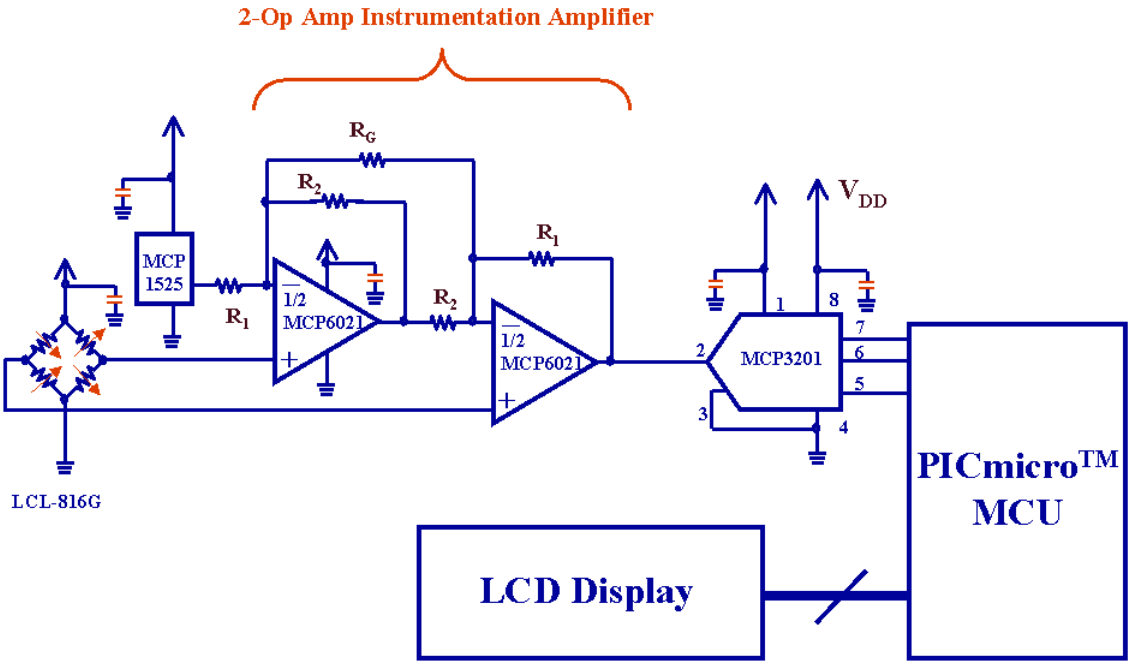


**Fig. 1: Signals From The Sensor Are Gained By An Instrumentation Amplifier, Filtered, Digitized (12-bit ADC, MCP3201) With Results Displayed On The LCD**

The application circuit that I'm going to use is a load-cell circuit that accurately measures the weight applied to the sensor, then displays the results on an LCD screen. The circuit diagram for this system is shown in Fig. 1.

The load cell that I used can be purchased from Omega (LCL-816G.) My sensor model for the LCL-816G is a four-element resistive bridge that requires voltage excitation. With a 5-V excitation voltage applied to the high side of the sensor the full-scale output swing is a ±10 mV differential signal with a 32 ounce maximum excitation. This small differential signal is gained by a two-op amp instrumentation amplifier. I chose a 12-bit converter to match the required precision of this circuit and once the converter digitizes the voltage presented at its input the digital code is sent to a microcontroller using the converter's SPI port.

The microcontroller then uses a look-up table to convert the digital signal from the ADC into weight. Linearization and calibration activities can be implemented with controller code at this point if need be. Once this is done the results are sent to the LCD. As a final step, I wrote the firmware for the controller and now the design is ready to go to board layout.

## One Major Step Towards Disaster

As I look at this complete circuit diagram I am tempted to use an auto router tool in my layout software. This is my first mistake. I have found that when I use this type of tool I often will go back and make significant changes to the layout. If the tool is capable of implementing layout restrictions, I may have a fighting chance. If my auto-routing tool does not have a restriction option, the best approach is to not use it at all.

## General Layout Guidelines

*Device Placement*

Now that I am working on this layout manually my first step is to place the devices on the board. This critical step is to effectively keep track of they noise-sensitive devices and their enemy, the noise-creator devices. There are two guidelines that I use:

1. Separate the circuit devices into two categories: High speed (>40 MHz) and low speed. When you can place the higher-speed devices closer to the board connector / power supply.
2. Separate the above categories into three sub-categories: Pure digital, pure analog, and mixed signal. With this delineation, place the digital devices closer to the board connector/power supply.

The board layout strategy should map the diagram shown in Fig. 2. Notice Fig. 2.a with the relationship between high speed vs. slower speeds and the board connector/power supply. In Fig. 2.b the digital and analog circuit is shown as being separate from the digital devices, which are closest to the board connector/power supply. The pure analog devices are furthest away from the digital devices to ensure that switching noise is not coupled into the analog signal path. The layout treatment of the ADC is discussed in detail in part 4 ("Layout Techniques to use as the ADC Accuracy and Resolution Increase") of this 6 part series.

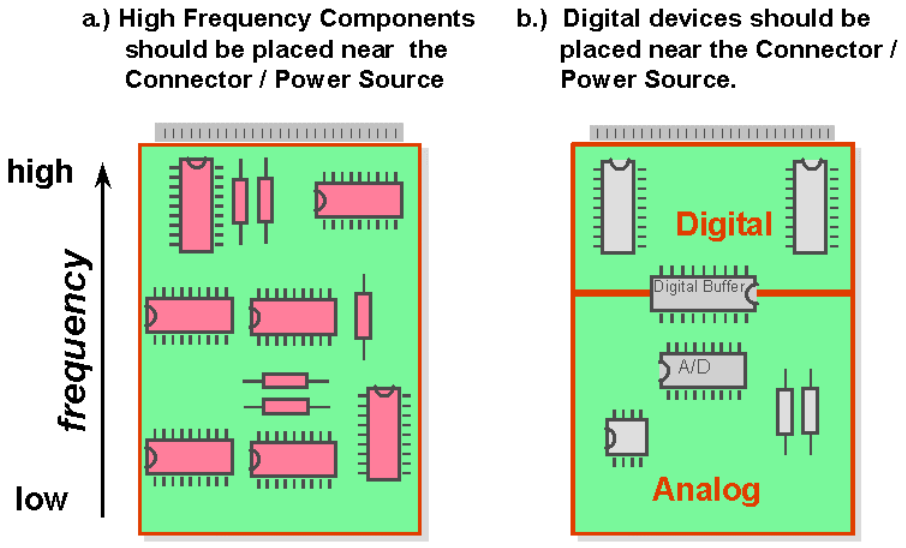


**Fig. 2: Placement Of Active Components On A PCB Is Critical In Precision 12-bit+ Circuits With Higher-Frequency (a) & Digital (b) Devices Closest To The Connector**

*Ground And Power Supply Strategy*

Once I determine the general location of the devices my ground planes and power planes are defined. My strategy of the implementation of these planes is a bit tricky.

First of all, it is dangerous for me not to use a ground plane in a PCB implementation. This is true particularly in analog and/or mixed-signal designs. One issue is that ground noise problems are more difficult to deal with than power supply noise problems because analog signals are referenced to ground. For instance, in the circuit shown in Fig. 1 the ADC's inverting input pin (MCP3201) is connected to ground. Secondly, the ground plane also serves as a shield against emitted noise. Both of these problems are easy to resolve with a ground plane and nearly impossible to overcome if there is no ground plane.

However, with my small design I assume that I won't need a ground plane. A ground plane-less layout implementation of the circuit in Fig. 1 is shown in Fig. 3.

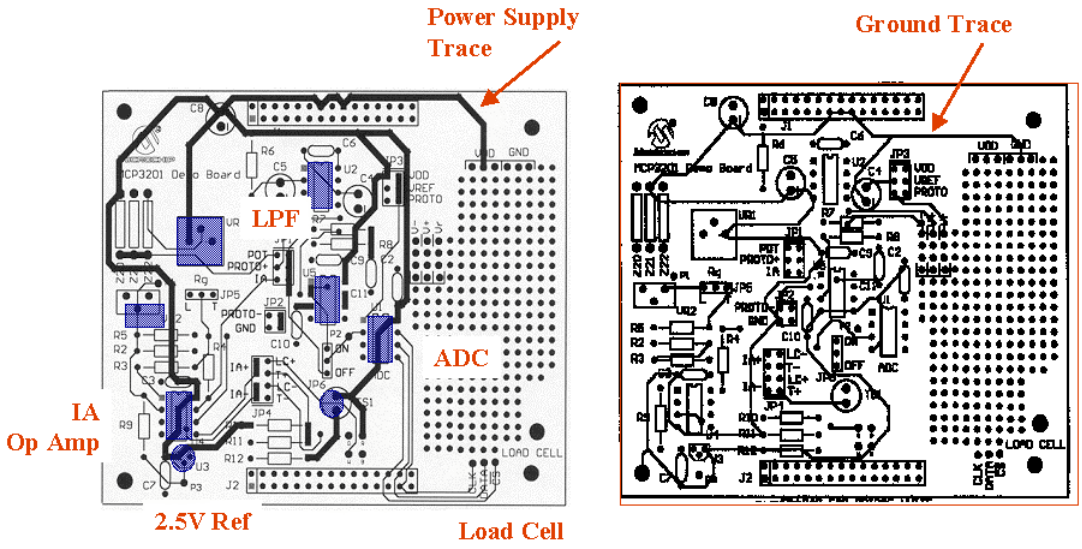


**Fig. 3: Layout Of Layers Of The Circuit With No Ground Or Power Plane. Power Traces Are Considerably Wider Than Signal Traces To reduce Inductance**

Does my "no ground plane is required" theory play out? The proof is in the pudding, or data. In Fig. 4 4096 samples were taken from the ADC and logged. No excitation was applied to the sensor when this data are taken. With this circuit layout the controller is dedicated to interfacing with the converter and sending the converter's results to the LCD.

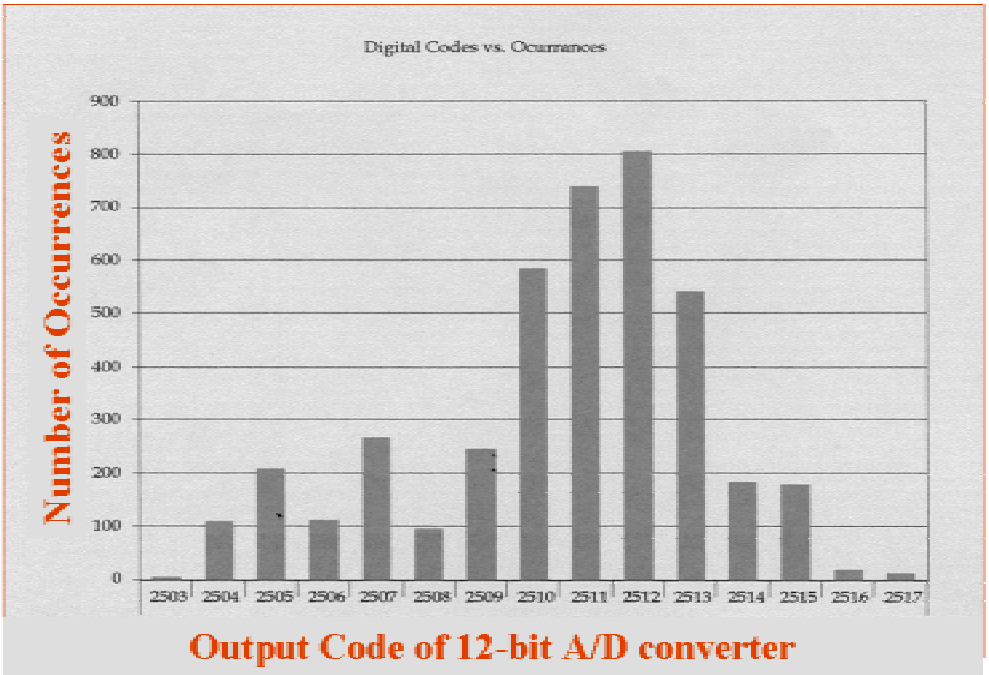


**Fig. 4: A Histogram Of 4096 Samples From The Output Of The ADC In The Fig. 3 PCB Layout. The Code Of The Noise From The Circuit Is 15 Codes Wide**

Fig. 5 shows the same device layout shown in Fig. 3 but a ground plane on the bottom layer is added. The ground plane (Fig. 5.b) has a few breaks due to signal. These breaks should be kept to a minimum. Current return paths should not be “pinched” as a consequence of these traces restricting the easy flow of current from the device to the power connector. The histogram for the ADC converter output is shown in Fig. 6 and compared to Fig. 4 the output codes are much tighter. The same active devices were used for both tests while the passive devices were different causing a slight offset difference.

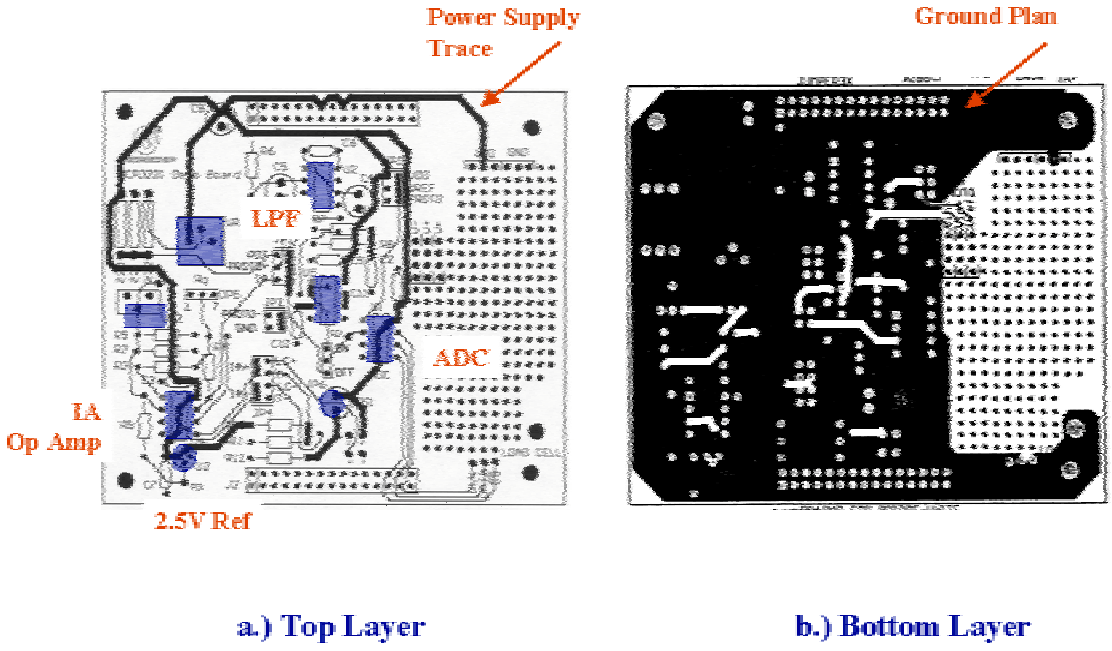


**Fig. 5: Layout Of The Layers Of The Circuit WITH A Ground Plane**

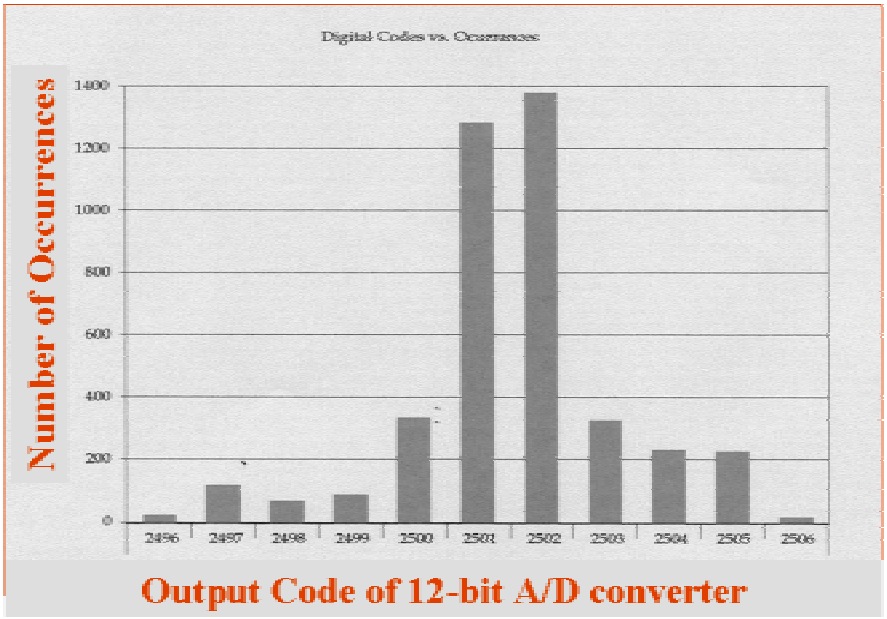


**Fig. 6: Histogram Of 4096 Samples From The Output Of The ADC On The PCB With The Fig. 5 Ground Plane. The Noise Is Now 11 Codes Wide**

It is clear from my data that a ground plane does have an effect on the circuit noise. Without a ground plane the width of the noise was ~15 codes and when I added one I improved the performance by almost 1.5X or 15/11. It should be noted that my test set up was in the lab where EMI interference is relatively low.

The cause of the noise can be attributed to op amp noise and the absence of an anti-aliasing filter. If my circuit has a "minimum" amount of digital circuitry on board, a single ground plane and a single power plane may be appropriate. My qualifier "minimum" is defined by the board designer. The danger of connecting the digital and analog ground planes together is that my analog circuitry can pick-up the noise on the supply pins and couple it into the signal path. In either case analog and digital grounds and power supplies should be connected together at one or more points in the circuit to ensure that my power supply, and the input and output ratings of all of the devices are not violated.

The inclusion of a power plane in a 12-bit system is not as critical as the required ground plane. Although a power plane can solve many problems power noise can be reduced by making the power traces two or three times wider than other traces on the board and by using by-pass capacitors effectively.

*Signal Traces*

My signal traces on the board (both digital and analog) should be as short as possible. This basic guideline will minimize the opportunities for extraneous signals to couple into the signal path. One area to be particularly cautious of is with the input terminals of analog devices where the impedance is normally higher than the output or power supply pins. As an example, the voltage reference input pin to the ADC is most sensitive while a conversion is occurring. With the type of 12-bit converter I have in Fig. 1 my input terminals (IN+ and IN–) are also sensitive to injected noise. Another potential for noise injection into my signal path is the input terminals of an operational amplifier. These terminals have typically $10^9$ to $10^{13}$ Ω input impedance.

My high impedance input terminals are sensitive to injected currents which can occur if the trace from a high-impedance input is next to a trace that has fast-changing voltages, such as a digital or clock signal. When a high-impedance trace is in close proximity to a trace with these types of voltage changes, charge is capacitively coupled into the high-impedance trace.

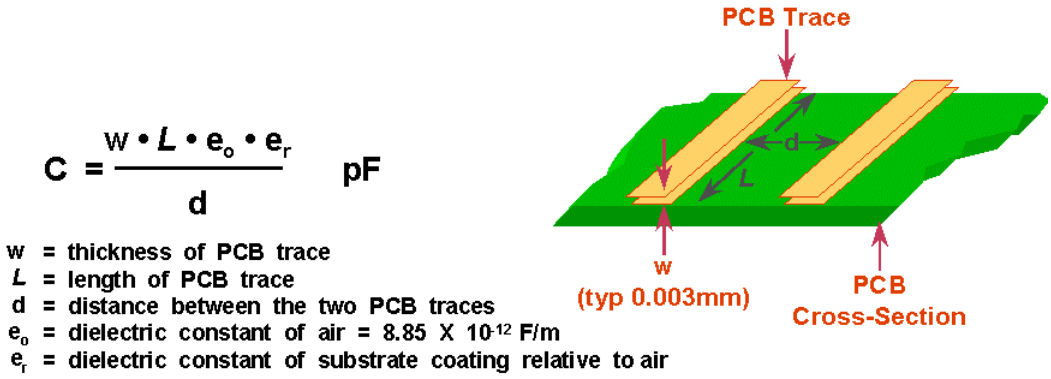


**Fig. 7: Capacitance Can Form With Traces In Close Proximity, Coupling Signals**

The relationship between two traces is shown in Fig. 7. In this diagram the value of the capacitance between two traces is primarily dependent on the distance (d) between the

traces and the distance that the two traces are in parallel (L). From this model, the amount of current generated into the high impedance trace is equal to:

$I = C\,\delta V/\delta t$

where,

*I* equals the current that appears on the high impedance trace
C equals the value of capacitance between the two PCB traces
$\delta V$ equals the change in voltage of the trace that is switching, and
$\delta t$ equals the amount of time that the voltage change took to get from one level to the next

## DID I SAY BY-PASS AND USE AN ANTIL-ALIASING FILTER?

Although this article is about layout practices, I thought it would be a good idea to cover some of the basics in circuit design. A good rule concerning by-pass capacitors is to always include them in the circuit. If they are not included the power supply noise may very well eliminate any chance for 12-bit precision.

### *By-Pass Capacitors*

By-pass capacitors belong in two locations on the board: One at the power supply (10 μF to 100 μF or both) and one for every active device (digital and analog), with the value depending on the functionality. For parts operating at 1 MHz, or less, 1 μF will reduce injected noise dramatically. If operation is above about 10 MHz a 0.1 μF capacitor is probably appropriate. In between these two frequencies, both or either one could be used. Refer to the manufacturer's guidelines for specifics.

Every active device on the board requires a by-pass capacitor and it must be placed as close as possible to the power supply pin of the part (see Fig. 5.) If two by-pass capacitors are used the smaller one should be closest to the pin. Finally, the lead length of the by-pass capacitor should be as short as possible.

### *Anti-Aliasing Filters*

You will note that the circuit in Fig. 1 does not have an anti-aliasing filter. As the data shows, this oversight has caused noise problems in the circuit. When this board has a $4^{th}$ order, 10 Hz, anti-aliasing filter inserted between the output of the instrumentation amplifier and the input of the ADC the conversion response improves dramatically. This is shown in Fig. 8.

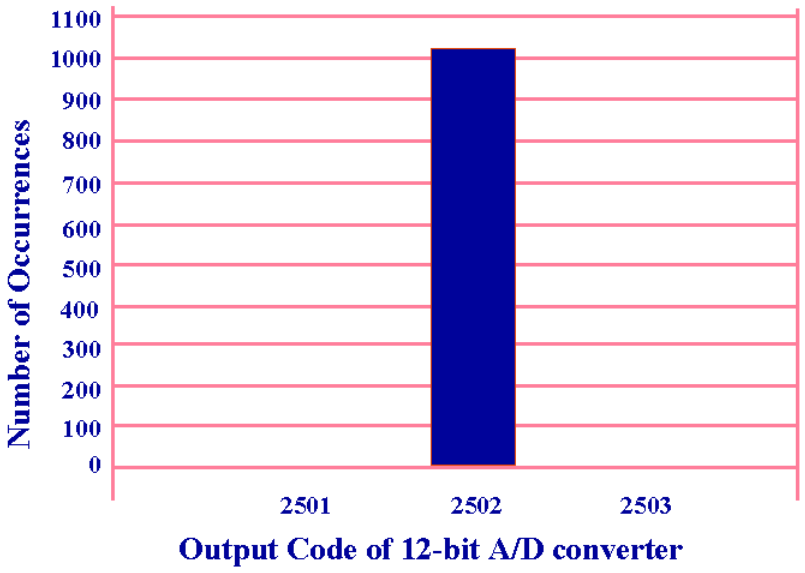


**Fig. 8: Conversion Results With A 4th Order Anti-Aliasing Filter And Ground Plane**

Analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. In particular this includes extraneous noise peaks. ADCs will convert the signal that is present on their input. This signal could include the sensor voltage signal or noise. The anti-aliasing filter removes the higher-frequency noise from the conversion process.

**PCB Design Check List**

Good 12-bit layout techniques are not difficult to master as long as you follow a few guidelines:

- Check device placement versus connectors. Make sure that high-speed devices and digital devices are closest to the connector
- Always have at least one ground plane in the circuit
- Make power traces wider than other traces on the board
- Review current return paths and look for possible noise sources on ground connects. This is done by determining the current density at all points of the ground plane and the amount of possible noise present
- By-pass all devices properly. Place the capacitors as close to the power pins of the device as possible
- Keep all traces as short as possible

- Follow all high-impedance traces looking for possible capacitive coupling problems from trace to trace
- Make sure your signals, in a mixed-signal circuit, are properly filtered