

Circuit Layout Techniques And Tips (Part II of VI)

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Could It Be Possible That Analog Layout Techniques Differ From Digital?

The increasing percentage of digital designers and layout experts in the engineering population reflects the direction our industry is headed. Although the emphasis on digital design is providing significant advances in end products, there is still, and will always be, a portion of circuit design that interfaces with the analog – or real world. There is some similarity in layout strategies between the two domains, but the differences can make an easy circuit layout design achieve less than optimum results. In this Part we will discuss the fundamental similarities and differences between analog and digital layouts with respect to bypass capacitors, power supply and ground layouts, voltage errors, and electromagnetic interference (EMI.)

The Similarities of Analog and Digital Layout Practices

Bypass or Decoupling Capacitors – In layouts, both analog and digital devices require these types of capacitor. In both cases the devices require a capacitor as close as possible to the power supply pin(s) with a common value being $0.1 \mu\text{F}$. A second capacitor in the system is required at the power supply source with a value of usually about $10 \mu\text{F}$.

The value of both these capacitors can vary ten times higher or lower, but for position (Fig. 1) both require short leads and must be as close to the device (with the $0.1 \mu\text{F}$ capacitor) or power supply source (with the $10 \mu\text{F}$ capacitor) as possible.

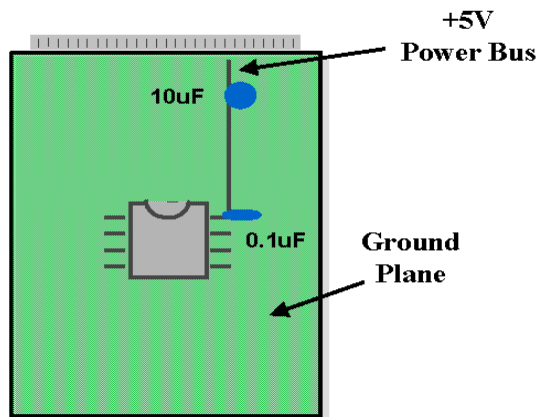


Fig. 1: In both analog and digital designs, bypass/decoupling should be as close to the device as possible. Power supply decoupling should be positioned where power enters the board. The capacitors should always have short leads.

Bypass (decoupling) capacitors' placements on the board are just common sense for both types of design, but interestingly enough, for differing reasons. In analog layouts, bypass capacitors generally serve the purpose of redirecting high-frequency signals that are on the power rail that would otherwise enter into the sensitive analog chip through the power pin. Generally speaking these high-frequency signals are higher than the analog device's capability to reject them. The possible consequences of not using bypass in your analog design are the addition of undue noise to the signal path and, worse yet, oscillation.

For digital devices, such as controllers and processors, decoupling capacitors are required for different reasons. One of the functions is to serve as a "mini" charge reservoir because in digital circuits a great deal of current is frequently required to execute the transitions of the changing gate states. Switching transient currents occur on chip, and throughout the circuit board, and having additional charge "on call" is advantageous. The consequences of not having enough charge locally to execute this switching action could result in a significant change in the voltage of the power rail. When the voltage change is too large, it will cause the digital signal level to go into the indeterminate state, more than likely resulting in erroneous operation of the state machines in the digital device. The switching current passing through the parasitic inductance of the circuit board traces would cause this change in voltage:

$$V = L\delta I/\delta t,$$

where, V = voltage change, L = board trace inductance, δI = change in current through the trace, and δt = the time it takes for the current to change.

So for multiple reasons, it is a good idea to bypass (or decouple) the power supply at the power supply and at the power supply pin of active devices.

The Power And Ground Should Be Routed Together

When power and ground traces are well matched with respect to location, the opportunities for EMI are lessened. If power and ground are not matched, system loops are designed into the layout and the possibility of seeing "noisy" results without explanation is possible. An example of a PCB designed with the power and ground traces not matched is shown in Fig. 2.

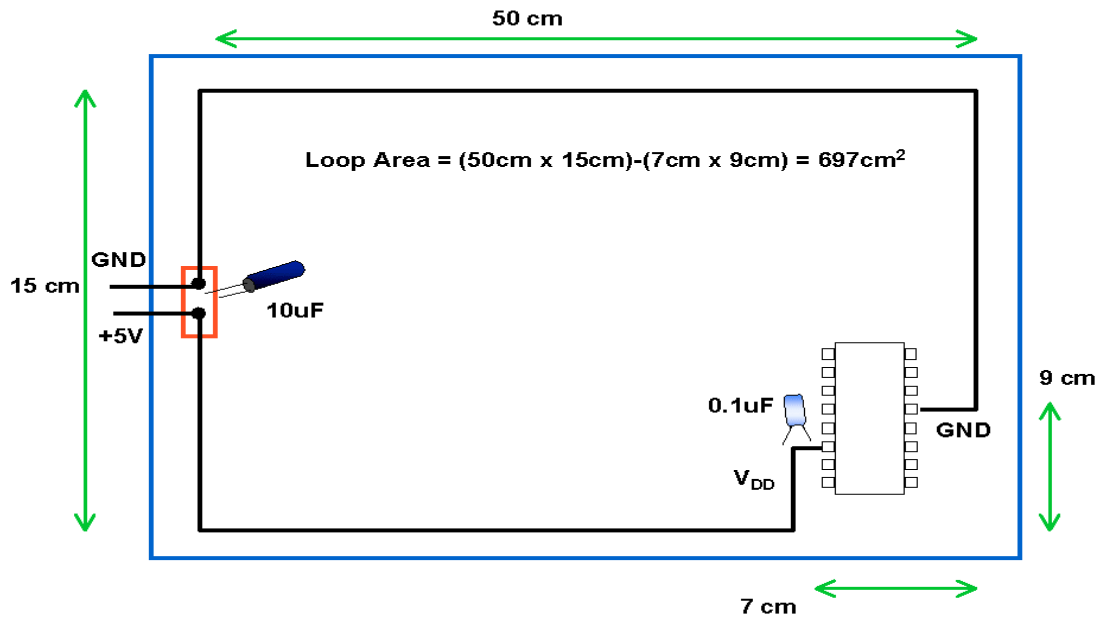


Fig. 2: The power and ground traces are laid out using different routes to the device on this board with the mismatch opening the opportunity for EMI.

The loop area designed into this board is 697 cm^2 ; the opportunity for induced voltages in the loop from radiated noise is decreased dramatically by the approach shown in Fig. 3.

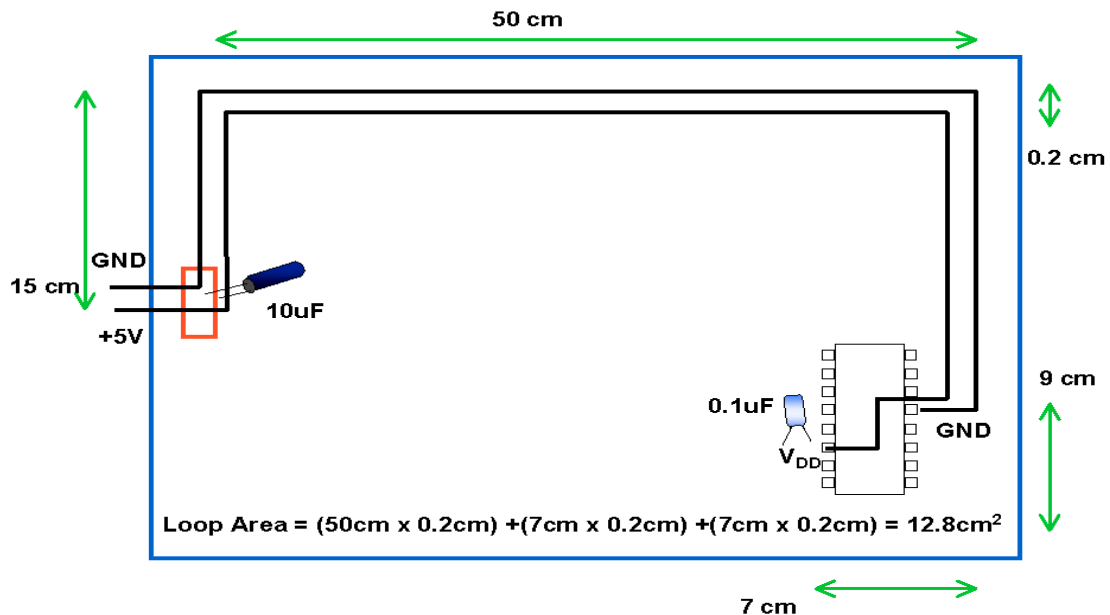


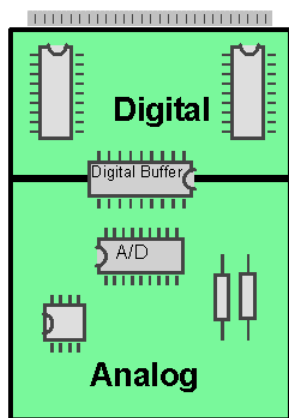
Fig. 3: In this one-layer board the power ground traces are laid next to each other on their way to the device. This is better matched than that in Fig. 2 lessening the EMI opportunity by $679/12.8$ or $\sim 54x$.

Where The Domains Differ

Ground Planes can be a Problem – The fundamentals of circuit board layout apply to analog as well as digital circuits. One fundamental rule of thumb is to use uninterrupted ground planes. This common practice reduces the effects of $\delta I/\delta t$ (changes in current with time) in digital circuits, which changes the potential of ground and noise being injected into the analog circuits. But when comparing digital and analog circuits, the layout techniques are essentially the same with one exception: That an added precaution be taken to keep digital signal lines and return paths in the ground plane as far away from the analog circuitry as possible by connecting the analog ground plane separately to the system ground connect, or by having the analog circuitry at the farthest side of the board, i.e. the end of the line. This is done to maintain signal paths that have a minimal amount of interference from external sources. The opposite is not true for digital circuitry which can tolerate a great deal of noise on the ground plane before problems start to appear.

Location of components – In every PCB design, noisy and quiet portions of the circuit should be separated as noted above. Generally speaking, digital circuitry is “rich” with noise and in turn less sensitive to it (because of the greater voltage noise margins.) In contrast the voltage noise margins of the analog circuitry are much smaller. Of the two domains, analog is most sensitive to switching noise and in the layout of a mixed-signal system, the two domains should be separated. This is graphically shown in Fig. 4.

a.) Separate the Digital and Analog Portions of the Circuit



b.) High Frequency Components should be placed near the Connectors

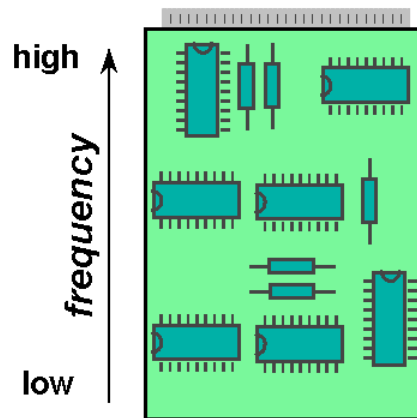


Fig. 4: If possible, (a) the digital and analog circuits should be separated to isolate digital switching from analog circuits: Additionally, (b) the high frequency should be separated from the low frequency keeping the former closer to the connectors.

Parasitics Designed into the PCB – There are two, fundamental, parasitic components that can be easily designed into a PCB to create problems: A capacitor and an inductor. A capacitor is designed simply by having two traces close to each other. This can be done by placing the two traces one on top of the other with two layers, or by placing them beside each other on the same layer (see Fig. 5.) In both configurations changes in voltage with time ($\delta V/\delta t$) on one trace could generate a current on a second one and if the second trace is high impedance, current created by the E-field will convert into a voltage.

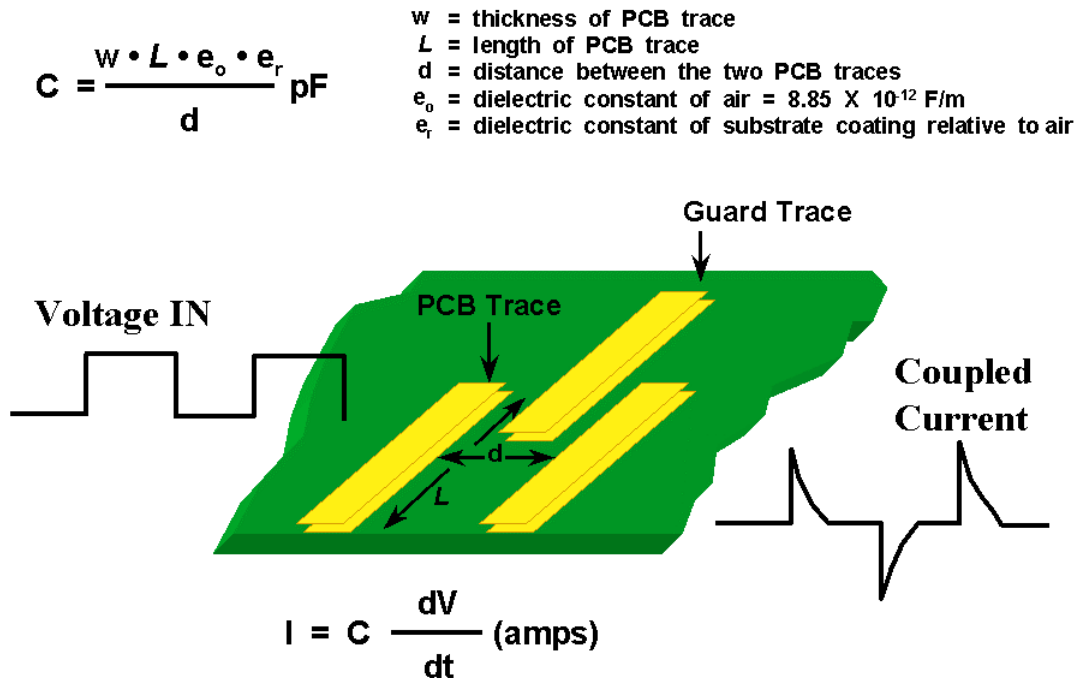


Fig. 5: Capacitors can be easily fabricated in a PCB by laying out traces in close proximity, with fast voltage changes on one trace initiating a current in the other.

Fast voltage transients are most typically found on the digital side of the mixed-signal design. If the traces that have these fast voltage transients are in close proximity to high-impedance analog traces; this type of error will be very disruptive to analog circuitry accuracy. Analog circuitry has two strikes against it in this environment: The noise margins are much lower than digital, and it is not unusual to have high-impedance traces.

This type of phenomenon can be easily minimized using one of two techniques: The most commonly-used is to change the dimensions between the traces as the capacitor equation suggests. The most effect dimension to change is the distance between the two offending traces – the variable, “d”, in the denominator of the capacitor equation. As “d” is increased, the capacitance will decrease. Another variable that can be changed is the length of the two traces. In this case if the length (“L”) is reduced the capacitance between the two traces will also be reduced.

Another technique used is to lay a ground trace between the two offending traces. Not only is the ground trace low impedance, but an additional trace like this will break up the E-fields that are causing the disturbance shown in Fig. 5.

The way that an inductor is designed into a board is similar to the construction of a capacitor, again, by placing two traces one on top of the other with two layers or by placing them beside each other on the same layer, as shown in Fig. 6. In both trace configurations, changes in current with time ($\delta I/\delta t$) on one could generate a voltage in the same trace due to its inductance and initiate a proportional current on the second trace due to mutual inductance. If the voltage change is high enough on the primary trace the disturbance can reduce the voltage margin of the digital circuitry enough to cause errors. This phenomena is not necessary reserved for digital circuits, but more common in that environment because of the larger, seemingly instantaneous switching currents.

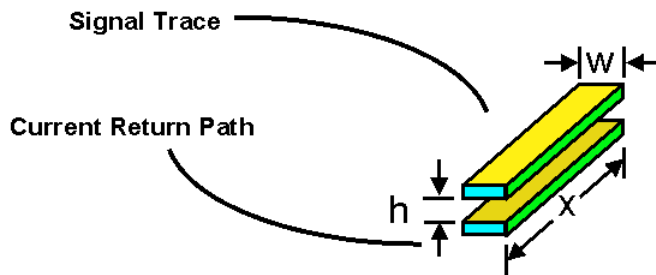
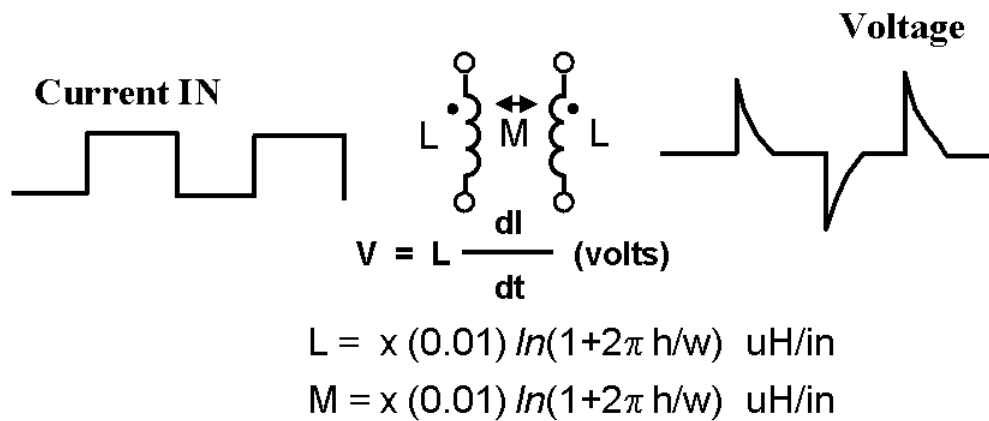


Fig. 6: If little attention is paid to the placement of traces, line inductance and mutual inductance can be created. This kind of parasitic element is most detrimental to the circuit operation where there are digital switching circuits.

To eliminate potential noise for EMI sources it is best to separate quiet analog lines and noisy I/O ports. Try to implement low-impedance power and ground networks, minimize inductance in conductors for digital circuits and minimize capacitive-coupling in analog circuits.

Conclusion

When the domains meet, careful layout is critical if a designer intends a successful final PCB implementation. Layout strategies are usually presented as rules of thumb because it is difficult to test the success of your final product in a lab environment. So, generally speaking, although there is some similarity in layout strategies between the digital and analog domains, the differences should be recognized and worked with. In this article we briefly talked about bypass capacitors, power supply and ground layout, voltage errors, and EMI because of PCB layout. For more information refer to:

[1] Henry W. Ott, *Noise Reduction Techniques in Electronic Systems*, 2nd ed., Wiley, 1998.

[2] Ralph Morrison, *Noise and Other Interfering Signals*, Wiley and Sons, 1992