

Operational Amplifiers Part I of VI What Does “Rail-to-Rail” Input Really Mean?

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Some single-supply operational amplifier advertisements claim rail-to-rail input operation capability. These claims are usually true, but there are a few compromises that have been made to achieve this type of performance. But if you are aware of the amplifier characteristics there are configurations that will minimize the effects of these compromises.

The input stage of amplifiers has changed dramatically from the time when two power-supply voltages were required. It was not long ago where amplifiers required ± 15 V power-supply voltages as a norm. With single-supply amplifiers the voltage of the supply has gone down dramatically and the negative-supply voltage is now ground. Typically, single-supply amplifiers are required to operate using a 5 V-supply voltage, but battery-operated applications are driving that voltage down even further.

Along with this reduction of power-supply voltages, the requirements on input range of the amplifier have changed. With dual-supply devices is it not unusual to have input common-mode swings that are a few volts from both supply rails. With a ± 15 V amplifier this means that the input range is 87% of the supply voltage. With single-supply amplifiers the input swings are required to be rail-to-rail or at least as high a percentage of the supply voltage as possible. You might ask why these amplifier ranges have improved from their predecessors? In the analog domain the noise margins do not go down with power-supply voltage. Consequently, every time the amplifier power supply is decreased, the relative input ranges must be increased.

R-R Input Performance Comes with Compromises

The input voltage range is more a function of the input circuit topology than the silicon process. The input devices of the amplifier can be CMOS, Bipolar, or JFET (Junction Field-Effect Transistor). However, there are three basic topologies: pMOS (p-channel Metal-Oxide Semiconductor) differential input pair; nMOS (n-channel Metal-Oxide Semiconductor) differential input pair; and pMOS/nMOS composite differential input pair. These are used to design the input stage of single-supply, voltage-feedback amplifiers. These topologies are shown (see Fig. 1) with a CMOS input stage. In Fig. 1a, pMOS transistors (Q_1 and Q_2) are used for the first device at the input terminals. With this particular topology, the gate of both transistors can go 0.2 V to 0.3 V below the negative power-supply voltage before the devices leave their active region. However, the input terminal cannot go any higher than several hundred millivolts below the positive power-supply voltage before the input devices are pulled out of their linear region. An amplifier designed with a pMOS input stage will typically have an input range from $V_{SS} - 0.2$ V to $V_{DD} - 1.2$ V.

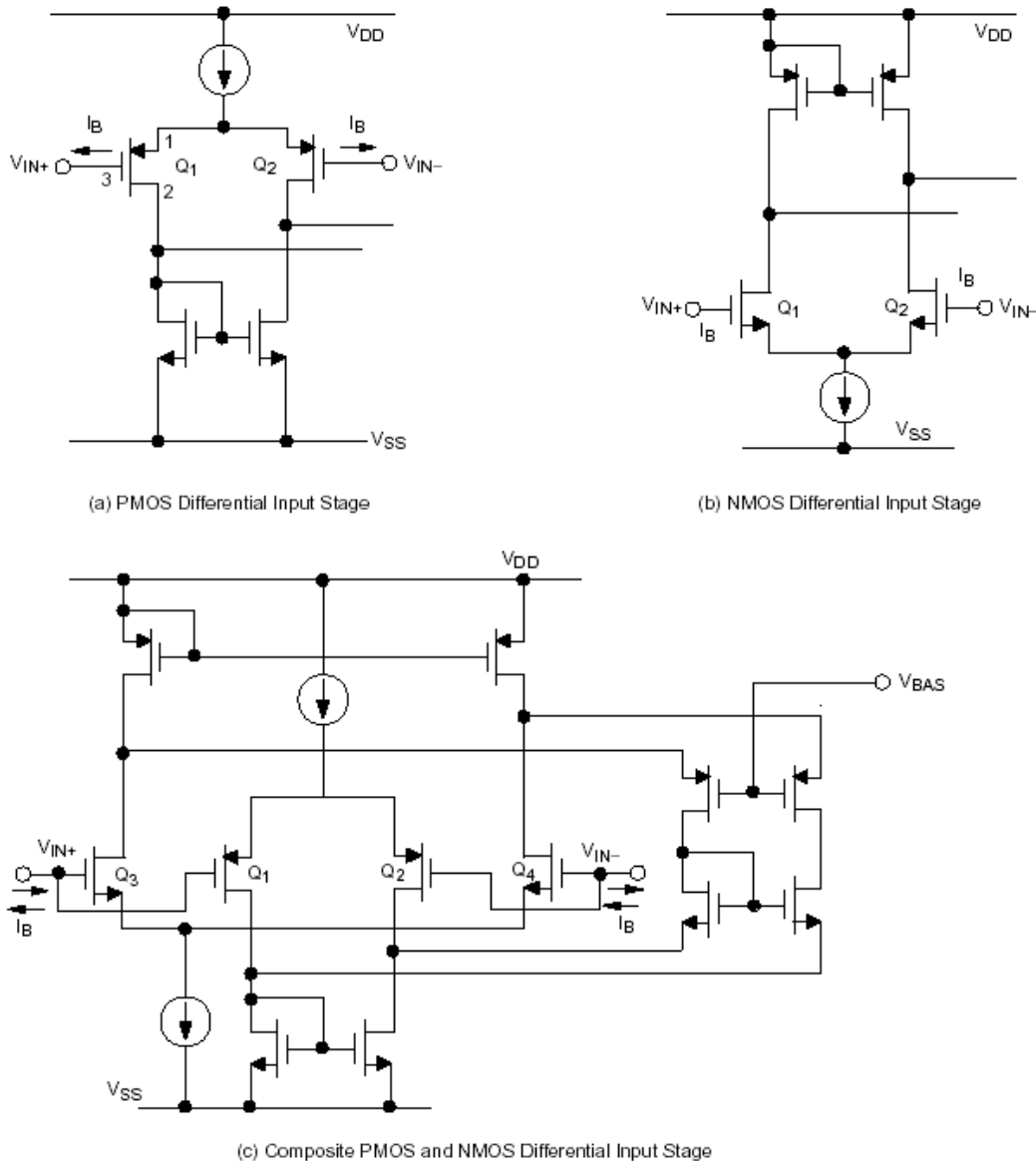


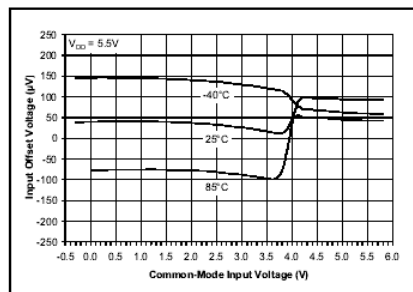
Fig. 1: Input voltage range of an amplifier is dependent on the topology of the input stage. The input stage can be a pMOS (a) differential pair allowing the input to swing below the negative rail, or an nMOS differential pair (b) where the inputs can swing above the positive rail. A composite input stage (c) uses both pMOS and nMOS differential pairs so the input-voltage range can extend from above the positive rail to below the negative rail

If the amplifier is designed with nMOS input transistors (Fig. 1b) the input range is restricted near the negative power-supply voltage. In this case, the input terminals can be taken to a few tenths of a volt above the positive-supply rail, but only to 1.2 V above the negative-supply rail. If an amplifier-input stage uses pMOS and nMOS transistors, it is configured as a composite stage (Fig. 1c). With this topology the amplifier effectively combines the advantages of the pMOS and nMOS transistors for true rail-to-rail input operation. When the input terminals of the amplifier are driven towards the negative rail,

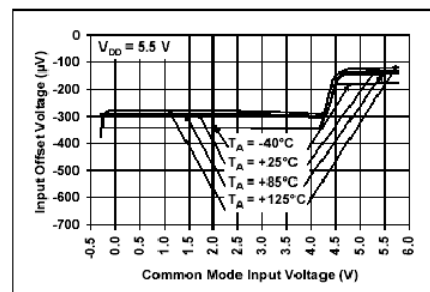
the pMOS transistors are turned completely on and the nMOS transistors are completely off. Conversely, when the input terminals are driven to the positive rail, the nMOS transistors are on while the pMOS transistors are off.

The basic topologies in Fig. 1 can be used with FET (field effect transistor) input or bipolar-input amplifiers. In the case of FET input amplifiers, the offset errors between the pFET (p-channel field effect transistor) and nFET (n-channel field effect transistor) are consistent with the CMOS errors with the circuit in Fig. 1c. With bipolar input stages, input-offset voltage variations are still a problem and input bias current is an additional error that is introduced. The nanoampere base current of an npn transistor comes out of the device, while the nanoampere base current of a pnp transistor goes into the device.

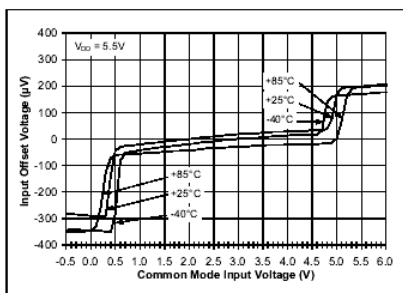
Although this style of input stage has rail-to-rail operation there are performance compromises: it will have wide variations in offset voltage. In the region near ground the offset error of the pMOS portion of the input stage is dominant and in the region near the positive supply, the offset error is dominated by the nMOS transistor pair. With this topology, the offset error can change dramatically in magnitude and sign as the common-mode voltage of the amplifier inputs extend over its entire range (see Fig. 2).



A.) 10MHz, CMOS, precision op amp (MCP6021)



B.) 1MHz, low cost, CMOS op amp (MCP6001)



C.) 14kHz, ultra low power, CMOS op amp (MCP6041)

Fig. 2: Input offset voltage vs. common-mode voltage of three different CMOS operational amplifiers over temperature with a single-supply of 5.5 V -- all three amplifiers have rail-to-rail input swing capability

The performance of three different CMOS amplifiers is shown in Fig. 2. The input stage topology for all three of these amplifiers is a composite nMOS and pMOS differential input stage (Fig. 1c, again). The amplifier in Fig. 2a is a high-speed, precision 10 MHz device. At lower input voltages the pMOS portion of the input stage is in operation with the nMOS portion turned off. At approximately 4.0 V the nMOS portion of the input stage starts to turn on and takeover the operation of the input stage.

The amplifier in Fig. 2b is a 1MHz device. It has the same input stage topology, but the nMOS portion of the input stage starts to take over at a slightly higher voltage, 4.4 V.

Finally, the amplifier in Fig. 2c has two transitions that occur as the common-mode input voltage is increased. At very low common-mode voltages the pMOS portion of the input stage is fully operational while the nMOS portion is turned off. As the common-mode input voltage increases, the nMOS section of the circuit quickly turns on. From approximately 0.5 V to 4.6 V both sections, pMOS and nMOS are operating. When the input voltage reaches approximately 4.75 V, the pMOS stage begins to shut down leaving the nMOS stage fully operational.

Each of the two input pins of the amplifier has voltage swing restrictions. In the device product data sheet, the input voltage restrictions are clearly defined in one of two ways: Most commonly the input voltage range, V_{IN} , is specified as a separate line item in the table. This specification can be defined as a condition for the CMRR (Common-Mode Rejection Ratio) specification, input common-mode voltage range, V_{CM} . The more conservative specification of the two is where the input-voltage range is called out as a CMRR test condition because the CMRR test validates the input voltage range with a second specification.

Application Challenge

The input voltage range restrictions and compromises become critical in a subset of amplifier circuit applications. For instance, if an amplifier is configured as a voltage-follower, it will most likely exhibit limitations in linearity due the input-stage topologies. This type of circuit is shown in Fig. 3a, along with a current monitor circuit in Fig. 3b. A buffer circuit configuration (Fig. 3a, again), requires rail-to-rail operation of the amplifier at its inputs as well as its outputs. The high-side current monitor circuit (Fig. 3b, again) uses an amplifier that must have an input-voltage range up to the positive rail. This circuit design senses the amount of current that is coming from the power supply. When the current exceeds 2 A, the non-inverting input of the amplifier falls below the inverting input. As a result the output goes low turning off the JFET, pulling the drain of the JFET low. This action brings the monitor output low.

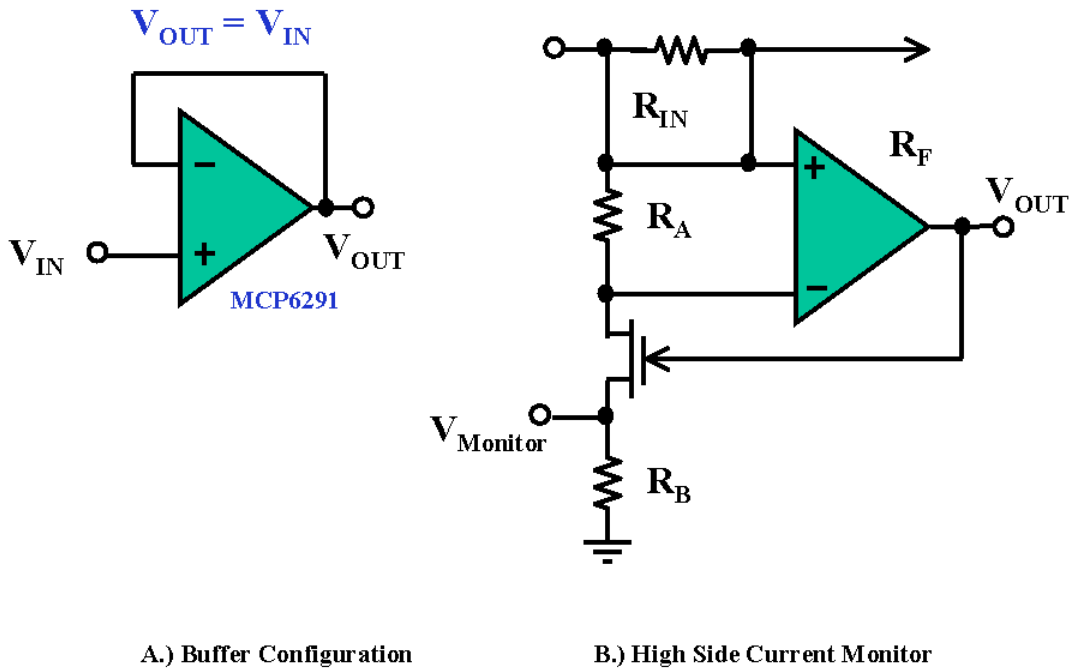


Fig. 3: Used as a buffer (A), the input devices of the operational amplifier may limit the input range of the buffer; used in a high-power supply-sense circuit (B), the input stage must be able to extend to the positive rail

These two applications present special requirements on the amplifier where rail-to-rail input operation is required. Most typically, an amplifier is designed with a closed-loop gain greater than one. In this instance the output-stage restrictions will limit the linear performance of the amplifier before the input stage will.

What Does Input Rail-to-Rail Really Mean?

If an advertisement that claims rail-to-rail input operation for an operational amplifier catches your attention, make sure you look deeper before using the product for your application. Rail-to-rail input specification claims are true, but the performance of the offset voltage could have an effect on your application circuit.

