ECOSat Communications Subsystem: RF Division Final Report

by

Kris Dolberg, and Jarrah Bergeron
kristofor.d@gmail.com, jarrahb1@uvic.ca
http://csdc.uvic.ca/RFcomms.php
Supervisor: Peter Driessen
Group: # 11
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Chapter 1 Goals

The RF subsection of the communications team was required to design a receiver (down-converter) and transmitter (up-converter) board to allow for the incoming and outgoing signals to be filtered and up-converted or down-converted to and from an intermediate frequency as the signal can only be processing in the baseband. The baseband signals are modulated or demodulated by the on-board digital signal processors in the modem which is separate but connected to our boards. The overarching goal was to build boards which satisfactorily do the up-conversion and down-conversion functions.

The secondary goals are the following. First, the board designs had to be completed, including part selection, board layout, part and PCB ordered. Second, the boards had to be built and work properly. And at last, the boards had to be characterized as to make sure they performed as needed.

Chapter 2. Project Overview

The goal of the ECOSat project as a whole is to design and construct a working cubesat with a payload capable of performing a series of experiments with diamagnetic materials and a communication system capable of performing the necessary tasks including the following. The first important task that the communication system performs is the relaying of telemetry data. Experiments in the diamagnetic payload will generate data about the results of the experiments. This data needs to be returned to earth so that they can be processed. The ECOSat communication system is also to be used as an amateur radio repeater. Signals broadcasted by amateur radio operators will be relayed forward by the ECOSat communications system. The communication system is also to be used as an experimental research platform for different software defined radio (SDR) modulation schemes. This research is the brainchild of UVic Ph.D. student Gorkem Cipli. Lastly, the communication system may also be used for delivering firmware updates to the satellite. These would be written on the ground and transmitted to the satellite.

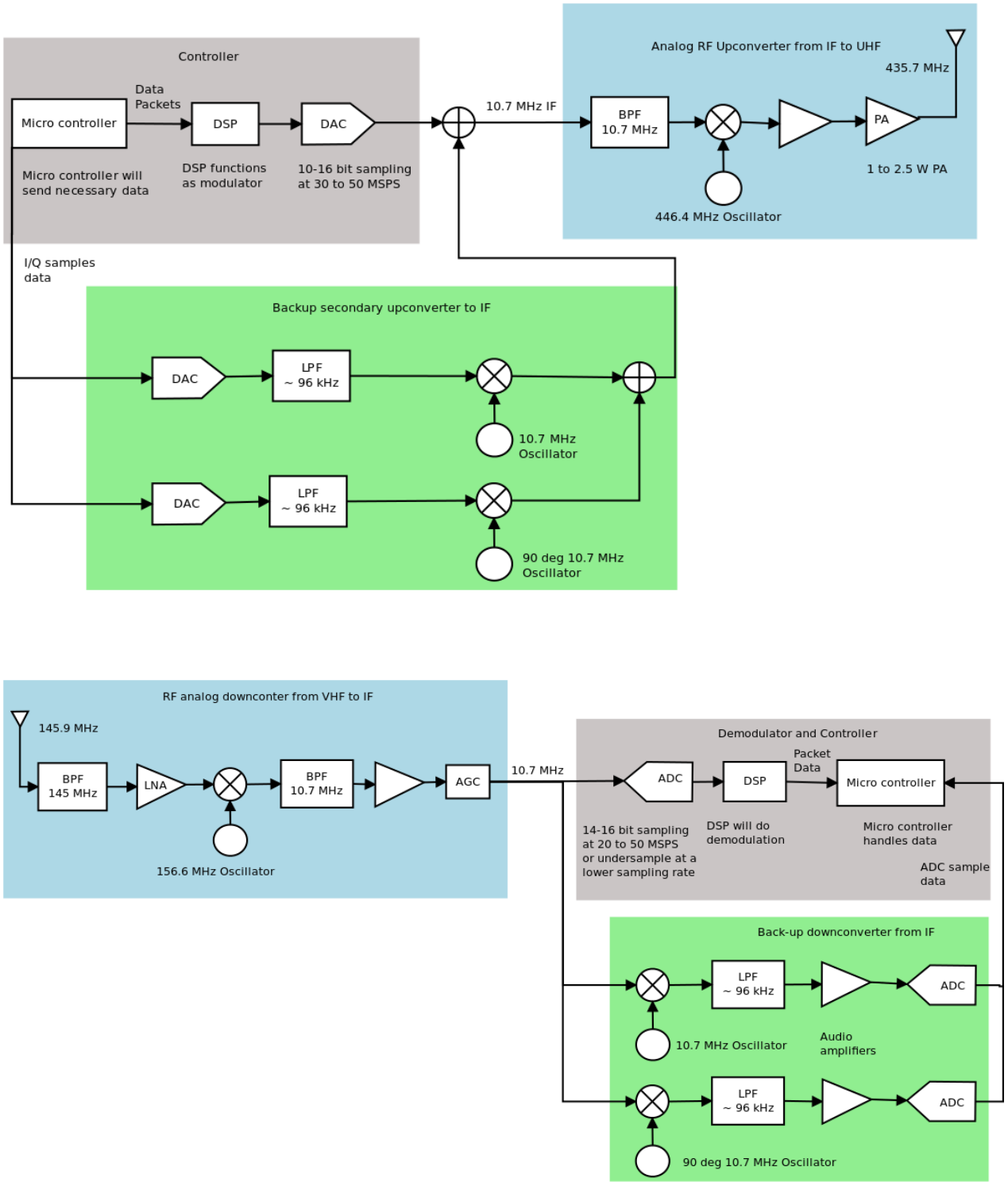
The radio-frequency (RF) boards at the center of our project are critical to the communications system as they provide a path for the signals to be converted to and from the transmission frequencies needed to propagate through space. Signals are demodulated and modulated in the baseband by a digital signal processor as RF frequencies are simply too high to be synthesized directly. Therefore, the baseband signal is first sent/received on an intermediate frequency of 10.7 MHz by the processor and then these signals come and go from our RF boards.

Chapter 3. Detailed Project Description

From our project proposal:

The University of Victoria ECOSat team is competing with 11 other Canadian universities in Geocentrix's Canadian Satellite Design Competition. The nanosatellite to be designed is 3U in size (approximately 10 by 10 by 30 cm) and must execute two missions, one of which must be scientific in nature. One of ECOSat satellite's missions will be to measure diamagnetic properties of pyrolytic graphite which will help with materials research for future space applications such as propulsion mechanisms. The second mission will be an OSCAR (Orbiting Satellite Carrying Amateur Radio) which will relay amateur operator messages around the world. The competition has been going for almost two years and is currently in its last stage with the final hardware delivery deadline in mid-September. Each of the satellite's subsystems is in the process of being built which includes the communications subsystem.

The communications subsystem is a large part of the satellite as it not only must receive commands from the ground and send back telemetry and status data but is also at the heart of the OSCAR which the satellite will be carrying. The communications system will be based on software-defined radio (SDR) which allows the flexibility of modulating and demodulation of signals in software. However, the very-high (VHF) and ultra-high frequency (UHF) signals cannot be synthesized directly from the processor as such tasks would be too computationally hungry. Instead, as with the vast majority of radios, the signals are first synthesized in baseband at low frequencies and then up-converted to the final transmit frequency or down-converted received signals back down to baseband. To accomplish this task, radio frequency grade analog circuits are used. A block diagram of the current communications design is shown below, first the transmitter and then receiver.



The proposed project is to complete both the up-converter and down-converter RF analog boards shown above in blue in the transmitter and receiver block diagram, respectively. Completion includes finishing the design, building and then testing the boards.

As this project is an ongoing venture, a preliminary schematic and board layout has already been produced for both the up-converter and down-converter boards. The tasks to be completed include:

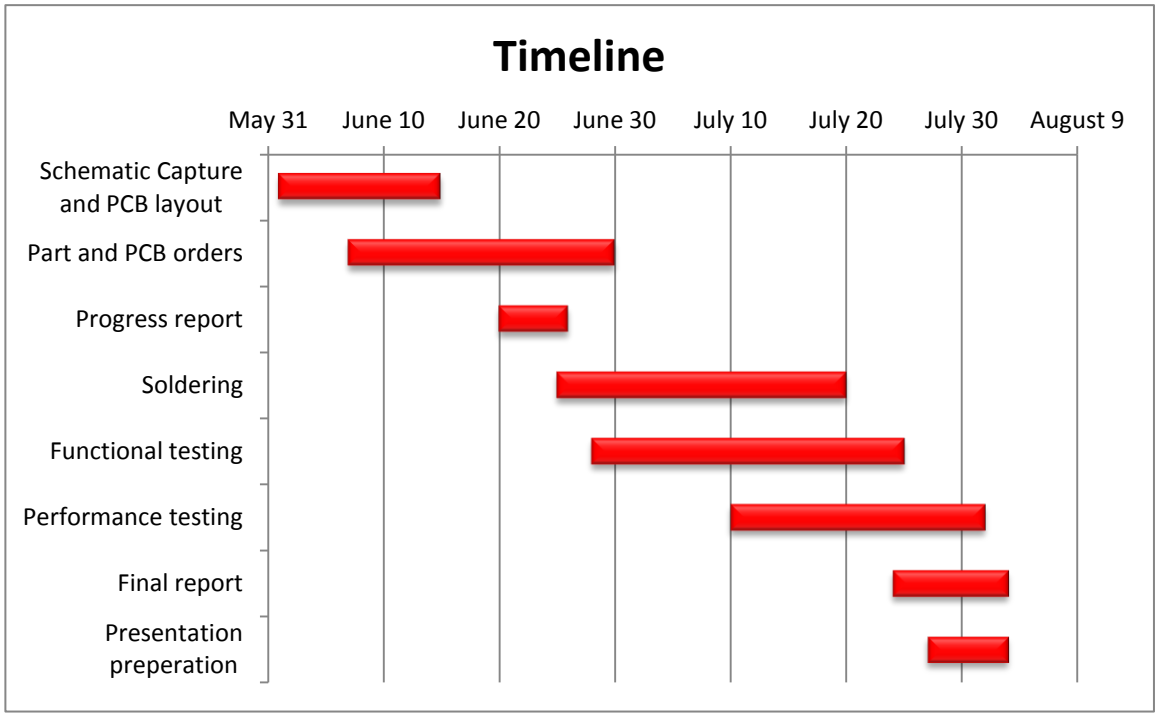
Finishing up the schematic capture, board layout and part selection

Ordering the parts and the PCB boards

Soldering components on to boards

Functional and performance testing

A Gantt chart is shown below of the tasks and associated timeline for the project. Major milestones will include final circuit and PCB design completion, component soldering completion and board and design testing completion.



All of these tasks will be done in cooperation with other members of the communications team and the satellite team as a whole. Synchronization between teams is crucial to complete satellite integration.

By the end of the term, functional RF up-converter and down-converter boards are to be delivered. Also, key performance parameters such as power consumption will be measured to make sure the design will integrate well with the rest of the satellite design. Project progress and final results will be documented as well in the form of a final report and presentation.

Chapter 4. Workload Distribution and Achievements

The workload, as our project, was divided into three main sections, part selection and board layout, board build, and board testing. Also, reports, the presentation and the website were a separate workload. The most demanding parts were the part selection and the board builds. Part selection can be a very arduous task as manufacturer and distributer parametric searches and other types of searches are not always intuitive or reliable. Also, the best combination of different performance factors is sought after and this can significantly lengthen the search time especially when comparing quantities with different measurement methodologies. As the boards came in rather late, the build had to be performed in a week and a half. As a result, a last minute scramble was needed to finish the project. Although overall, the project workload was not very high, at certain times, it was very busy.

Among the two partners, the workload was spread around. Jarrah mostly focused on the board design and build while Kris focused on reports, websites and the presentation. When possible, one partner would help the other. Each partners' strengths were leveraged to maximize the success of the project while trying to learn new things.

Most of the goals were achieved. The design and part selection was completed, and the boards built. The down-converter board was a success: it functioned close to as expected. The up-converter board, because of human error, could not be completed. One of the very last component to be soldered, which was part of the power amplifier, was mistakenly not ordered. However, the rest of the up-converter board was functional.

Chapter 5. Project Discussion

The discussion is broken up into three sections: the design of the boards, the build and the final results and performance.

Circuit Design

For the first part of the project, part selection and finalizing the board design was achieved. This part of the project took significantly more time than expected as the space environment severely constraints the design and part selection as was outlined in the progress report. Temperature was the most limiting factor, not because it is too cold but heat cannot escape and the temperatures were modeled to go up to 100 °C. The crystal, clock generators, filters and the power amplifier had very few options and the eventual selected parts were on the borderline of achieving these requirements. Also, radio frequency design entails a lot of small details which can make a big difference: component placement, track placement and second order effects in components which are not inherently obvious. As a result, the design went through a few people with design experience in the field. This design review also took significantly more time than expected but the design was improved as a result. At the time of the last progress report, the boards and the parts were being ordered.

Board Builds

The boards did finally come back from the board house, as well as the components. The PCB manufacturer did a good job with the boards and they came up as expected. Altium's rendering of the boards are shown in Figure 2 and Figure 3. Unfortunately, parts took longer to arrive which delayed the board build further. To solder the parts, a reflow process was selected. Although hand soldering with a soldering iron was an option, it tends to become unreliable,

especially at these small scales. A hot air gun, in combination with solder paste did the job quite well. The build was started with the power section of both the up-converter and down-converter boards as all the other components need a regulated power rail. Some problems where encountered with the polarity of the filtering tantalum capacitors as the wrong polarity caused shorts which were not inherently obvious with a multi-meter. Second, the intermediate frequency (IF) sections of both boards were built and tested as needed. The IF section of the down-converter board (receiver board) is more complex and required significant testing of the amplification, filtering and automatic gain control (AGC) of the variable gain amplifier (VGA). This section of the board was built without problems. The AGC performed quite well: keeping the output signal at a near constant level with varying input powers.

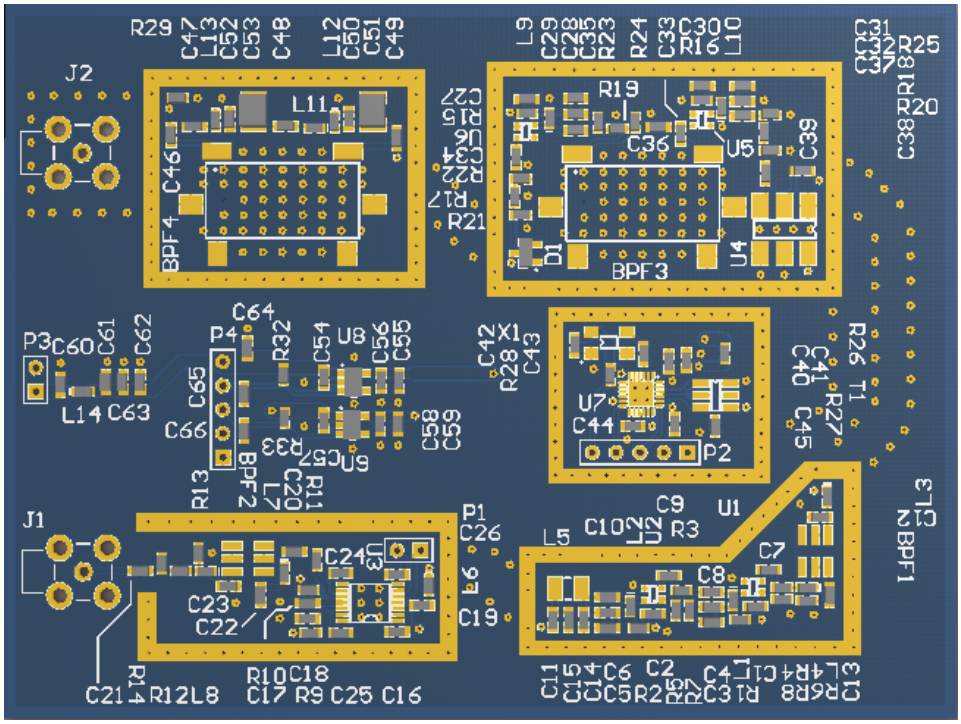


Figure 1: Downconverter PCB rendering

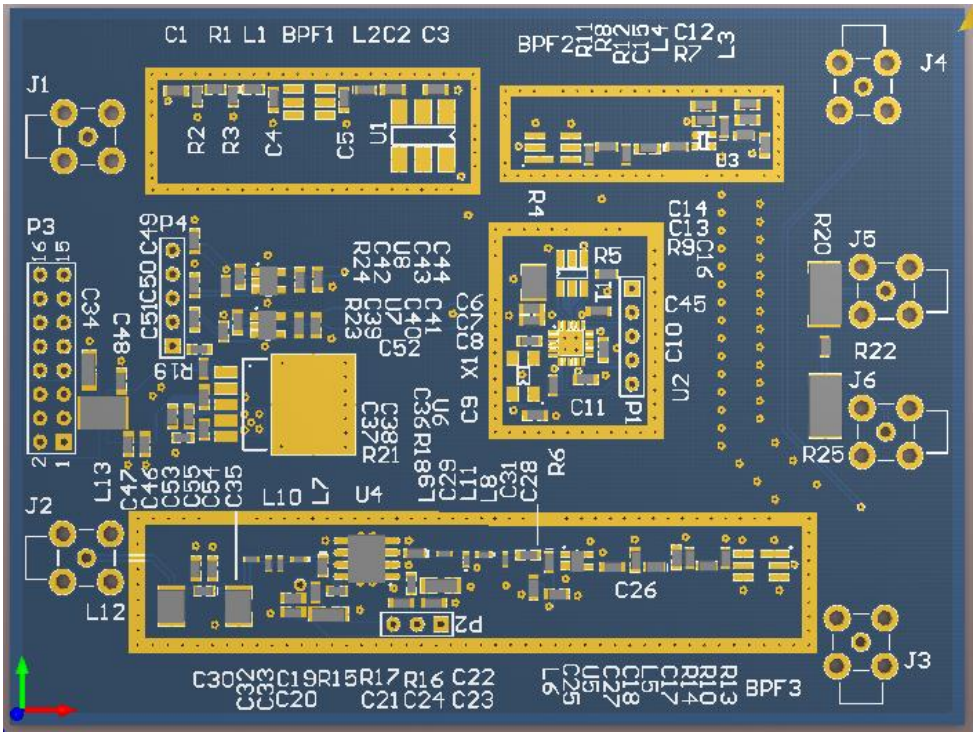


Figure 2: Upconverter PCB rendering

Next, the local oscillator was built. The clock generator is used as a RF oscillator because of its high frequency capability. The circuit was built up easily but the programming of this chip was challenging. The clock generator has a set of registers (over three hundred) which need to configure properly to be able to synthesize the right frequencies and drive logic. Luckily, a desktop program available from the manufacturer's website (ClockBuilder Desktop™) was used to obtain the right register values; however, the chip had yet to be programmed. Using Microchip PICKIT 3 programmer and debugger, in combination with its demo board, a microcontroller (pic18f45k20) was programmed to interface, via I2C, to the clock synthesizer. The setup is shown in Figure 3. The PC is connected to the PICKIT 3 programmer which is connected to the demo board and then the demo board is in turn

connected to either the up-converter or down-converter board via an I^2C bus with appropriated cabling.

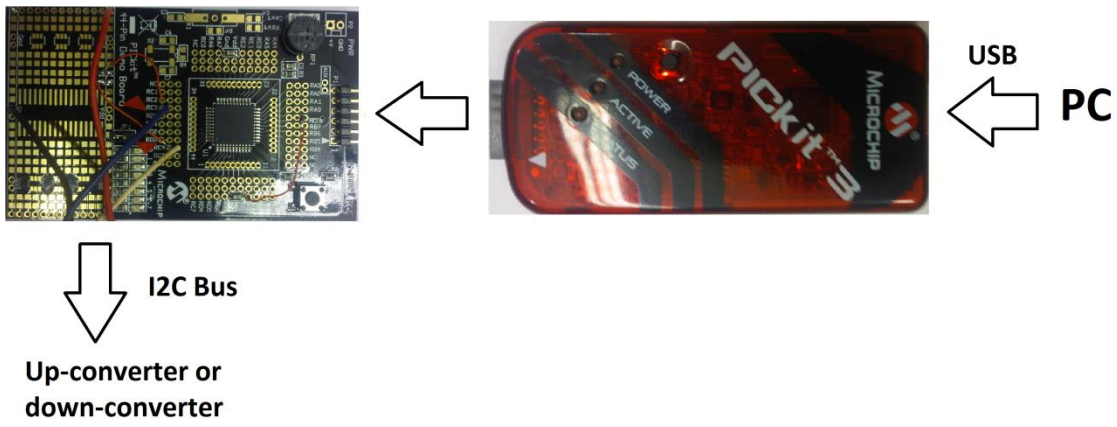


Figure 3: Micro controller interface to the clock synthesizer

Unfortunately, interfacing with this chip was quite challenging as it employed a non standard implementation of the I2C protocol and the System Management Bus (SMBus) protocol. The interfacing issues were eventually resolved but the project was at a standstill for a few days as getting this circuit to work was critical to continuing on the built process. The clock synthesizer operation was confirmed but the output power was lower than expected, especially for the transmitter board which operates at a higher frequency. This fact has consequences for the mixer efficiency to perform up/down frequency conversion.

The next circuit to be built was the RF sections of both boards. An error was found in the PCB. The RF pin of the mixer on the down-converter was connected to the IF section and vice-versa. By tomb stoning components and with some extra wiring, the error was fixed. Also, a solder short was found underneath one of the down-converter filters which was diagnosed by the lack of signal transmission. Unfortunately, the up-converter build could not be completed. One of the main power amplifier inductors was mistakenly not ordered and without this critical component, it could not be tested. The down-converter board was, however, completed and was

deemed functional. Pictures of the boards are shown below. Some pads miss parts because they were placed just in case more components were needed.

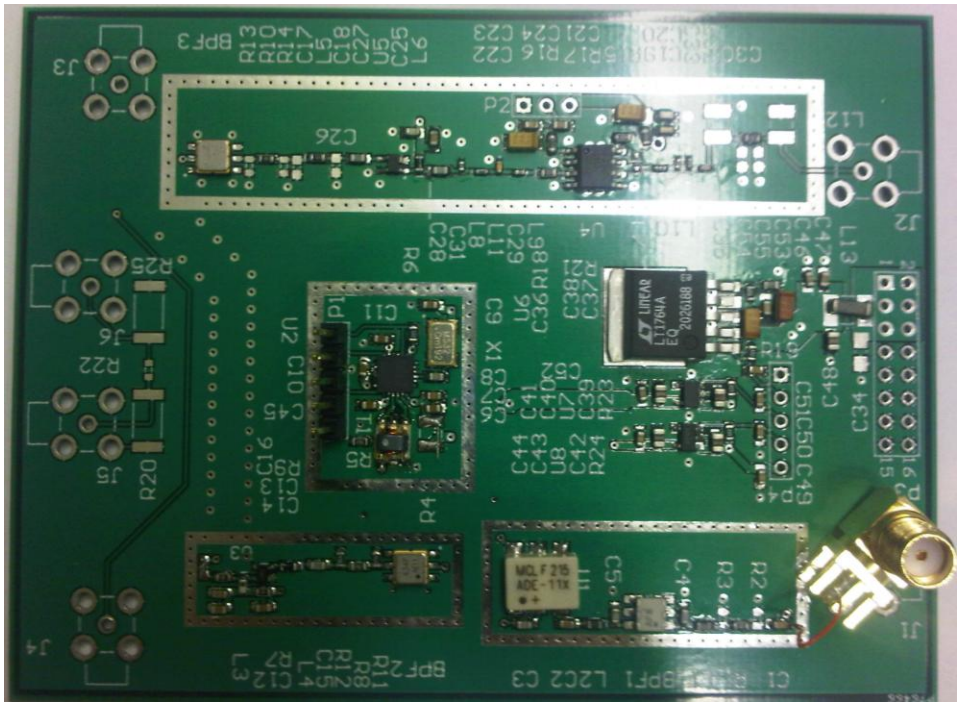


Figure 4: Up-converter board

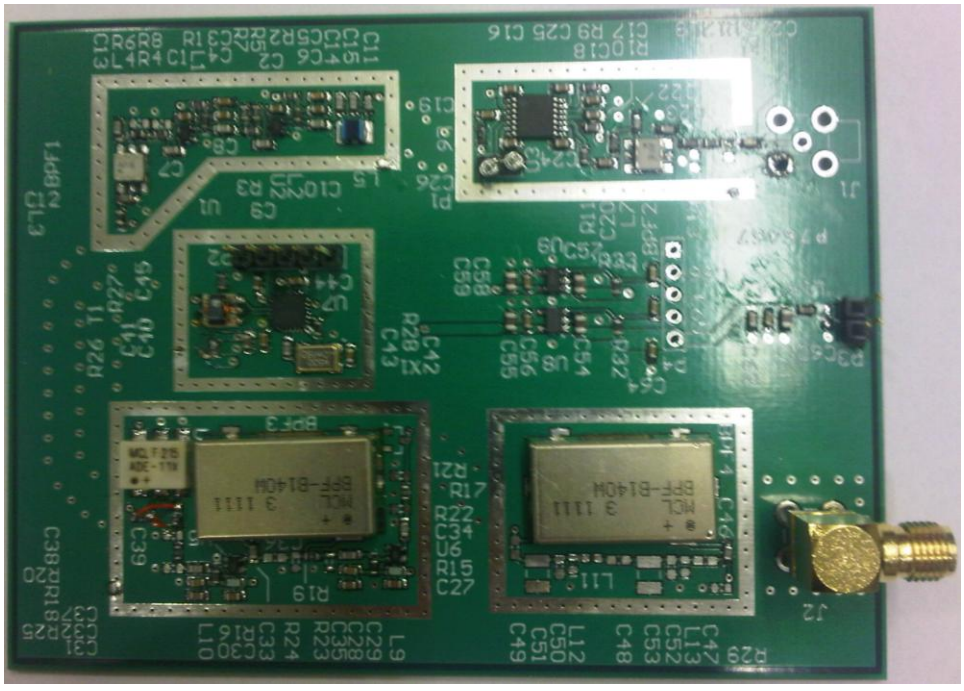


Figure 5: Down-converter board

Final Results

A few of the key performance parameters are shown in and with a discussion on how the parameters were measured following. As mentioned above, the up-converter board could not be completed but the parameters which would have been measured as still shown.

Parameter	Result	Requirement	Comments
Mass	30 g		Total mass of all SDR boards < 334 g
Power consumption	TBD mW		
Output power (3 dB compression)	TBD W	~2.5 W	
Noise figure	TBD dB		(Noise density+174dBm/Hz - gain)
Gain	TBD dB		
3 dB compression point	TBD dBm		
Reflected power	TBD %		
3dB bandwidth	TBD kHz	300 kHz	
Image suppression	TBD dB		

Table 1: Up-converter performance parameters

Note: All parameters measured at the 3 dB compression point.

Parameter	Result	Requirement	Comments
Mass	30 g		Total mass of all SDR boards < 334 g
Power consumption	715 mW		5.5V input
Minimum signal power	-120 dBm	-119.03 dBm	SNR = 5 dB
Noise figure	3.3 dB		At -80 dBm signal
Maximum Gain	95 dB		
3dB bandwidth	315 kHz	200 kHz	
Image suppression	43 dB		

Table 2: Down-converter performance parameters

The mass was measured as being the completed boards including all required connectors. The power consumption was measured using the power supply values at the recommended supply voltage. The output power of the up-converter board would have been measured using a setup similar to Figure 6. The direction coupler serves two purposes. First, it protects the spectrum analyser from the high power output from the power amplifier by only sampling a fraction of the transmitted power. Also, it measures the reflected power which can be used to gauge impedance mismatches between the power amplifier (PA) and the load. The coupling

ratio was first measured by a known, lower power source and then used to measure power. By extrapolating the power at low levels (where the PA is operating in a linear regime) and noting where the true power output deviates by the linear approximation, the 3dB compression point can be found.

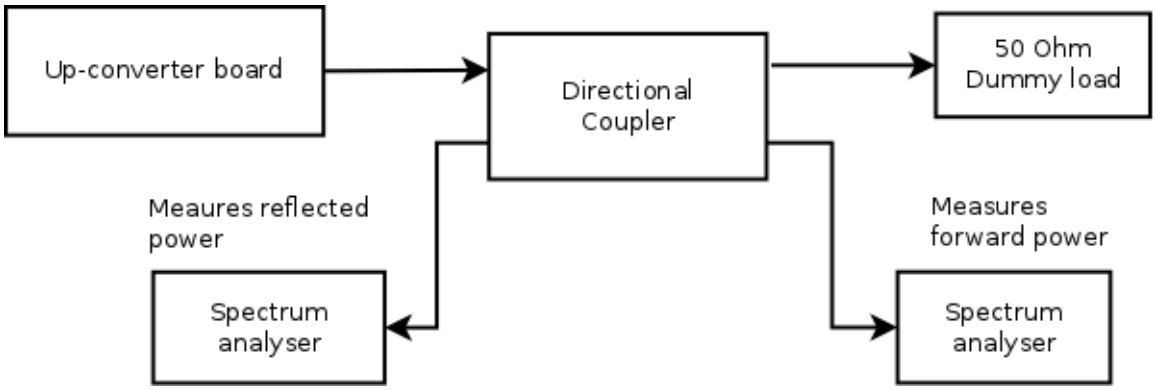


Figure 6: Power amplifier measurement setup

The noise figure was measured by first measuring the gain with an input signal. Next, the input was 50 Ω terminated and then the output noise density can be found by

$$output\ noise\ density + 174\frac{dBm}{Hz} - gain = NF \text{ [1]}$$

, where the output noise density can be found from the spectrum analyser using the noise floor power divided by the resolution bandwidth (RBW). The output SNR can also be plotted versus input signal power as shown in Figure 9.

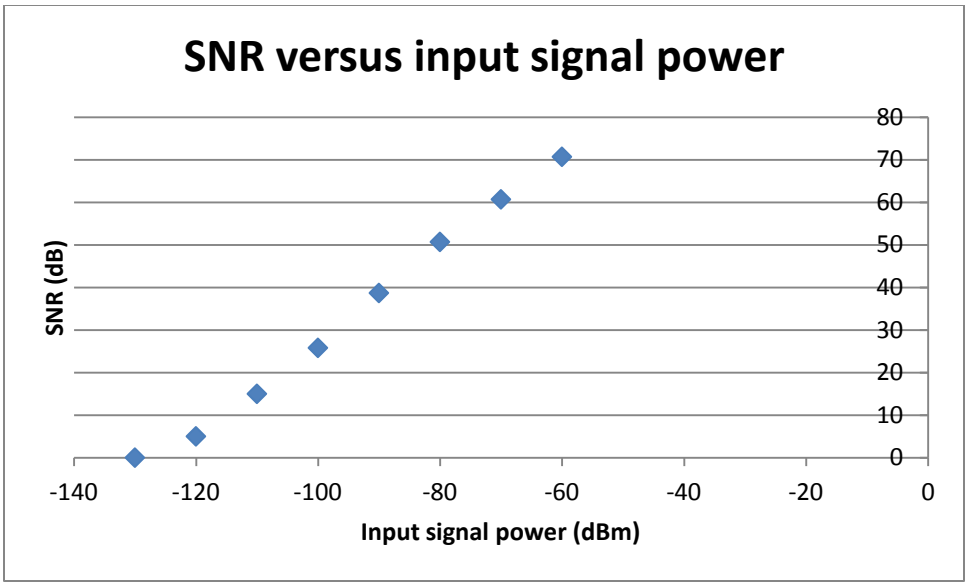


Figure 7: SNR of output signal versus input signal

The down-converter gain was measured as the maximum gain at different input powers. The graph of the output power versus input power is shown in Figure 8. The flat section in the output power is the result of the AGC of the final IF amplifier. The AGC voltage is also plotted, shown in Figure 9. Note the expected linear (with a logarithmic scale) increase in AGC voltage with increasing signal strength from the maximum gain to the maximum attenuation capable from the VGA amplifier.

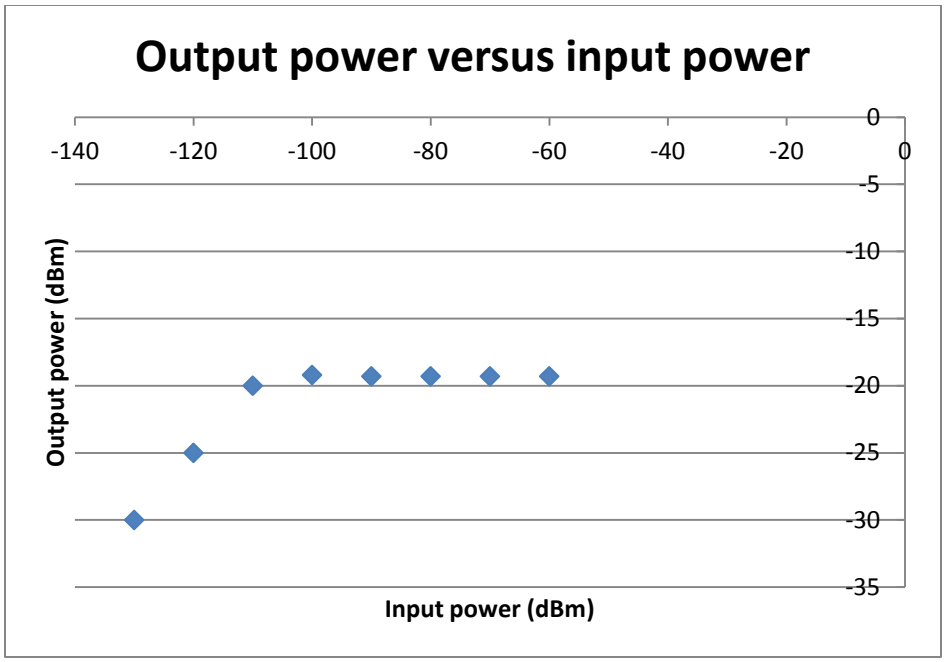


Figure 8: Down-converter output power versus input power

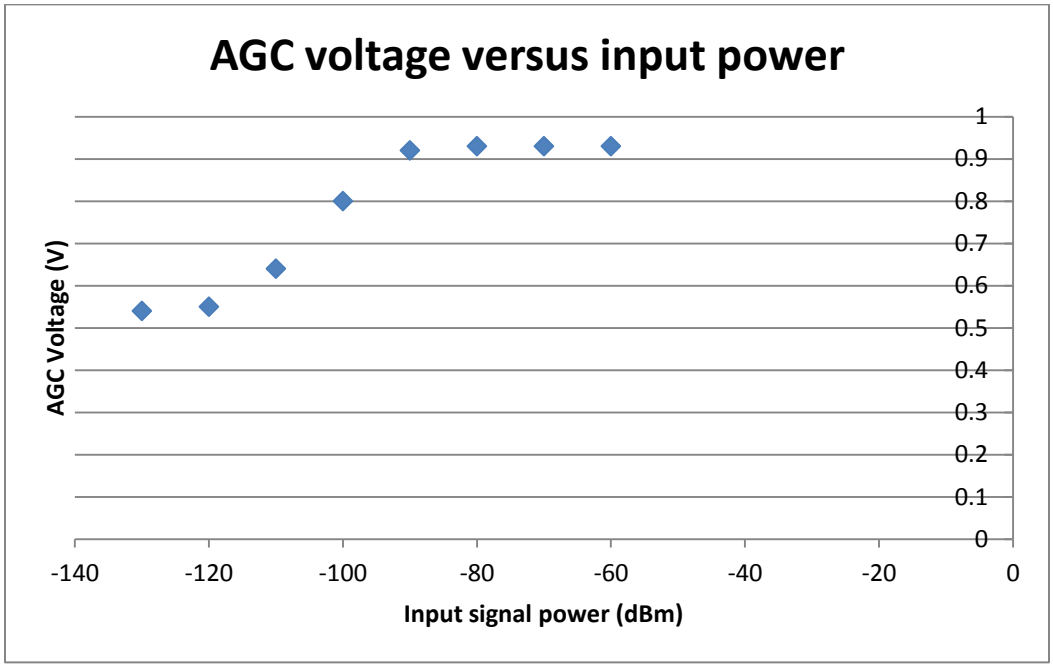


Figure 9: AGC voltage variation versus input voltage

Finally, the image rejection ratio was found for the down-converter. To measure this, first, an in-band reference signal was sent and the output power was recorded. Next, at the image frequency band, the input power was set such that to have the same output power. This

method was chosen as the output signal of the down-converter has a limited dynamic range. The up-converter board image rejection would have been measured by measuring the difference in signal power between the correct signal and its image.

Even though the up-converter was not completed, some measurements were done up to the final power amplifier and the circuit was deemed to be working. The only possible issue, which was mentioned earlier, is the low drive power from the local oscillator (LO). The mixer specified a LO power of 7 dBm; however, the power was measured to be only -5 dB. Although the circuit still works, the conversion efficiency of the mixer will suffer (as well as other parameters). This issue would need to be investigated further and some modification of the circuit may be required later on.

Chapter 6. Summary and Future Works

The board builds were almost a complete success. The down-converter board was completely designed, built and tested and meted our expectations. A few key parameters of interest were measured to check the functionality of the down-converter board. The up-converter board could not be completed but the parts of the circuits which could be built were all functional. We are confident with the last component that the up-converter would work just as well.

The next task to be completed is evidently soldering the last component on the up-converter board and perform the measurements outlined in the discussion section of the report. Also, some performance optimization may be required to enhance their performance if need be. As these boards are only part of a much larger communications system, the other parts of the system must be built including the baseband processing board. And last but not least, the whole satellite must be finished by the end of September when the competition ends and environmental testing begins.

Appendix A. Textbook Review

Read Part 4 of "Systems Analysis & Design" and write a review report on the related contents.

The implementation phase of system design is critical. This is where programmers write code for the system and analysts develop tests that will demonstrate that the system is operating properly within the agreed upon specifications. The project manager assigns certain tasks to programmers. The number of programmers will ideally be the minimum needed to complete the tasks. Time management of the team is critical to the project manager who must adjust the planned schedule to accommodate delays and changing requirements.

As has been mentioned before, testing is an important part of the implementation process. A test plan is a series of tests that evaluate different characteristics of the system. There are many types of tests of interest: unit tests, integration test, system tests, and acceptance tests.

Documentation comes in two main types: user and system. User documentation has three different types: reference documentation, navigation documentation and procedure manuals.

Transitioning to a new system is a very difficult task. Lewin model of changing a system has three steps: unfreeze, move and refreeze.

A migration plan is a plan for changing from the as-is system to the to-be system. It contains elements that can guide the transition. The software and hardware must be installed

and the data must be converted to the new storage format. Those who make the choice to migrate to the new system must understand the factors that make people resistant to change. Conflict can arise if these factors are not taken into consideration.

After the system has been implemented, the operations group must provide technical support for the system. The project must be assessed to determine what aspects of the system were successful and what was not. All important lessons learned must be documented. The discrepancies between the costs and benefits that were calculated before the system was implemented and the costs and benefits that exist in the implemented system must be assessed as these lessons will be served well by any future projects.

Object-oriented techniques have revolutionized system analysis and design. Essentially, an object is a model used to capture information about a person place or thing. There are four important types of diagrams used to aid in object-oriented design. These are the use case diagram, the class diagram, the sequence diagram, and the behavioral state machine diagram. There are several steps involved in building a use-case diagram. The first is to identify the use case. The second is to draw the system boundary, next add the use cases must be added to the diagram. Lastly, the associations must be drawn to connect the use cases to each other. Class diagrams are used to show relationships between classes used in the system. The purposes of sequence diagrams are to show the particular instances of different classes. The first step in creating a sequence diagram is to identify the classes that are important to the use case in question and show the messages passing between them. The behavioural state machine diagram

is also important. It is a comprehensive representation of the different states that a class can pass through in its lifetime.

Learning about the above subject matter did not serve well for our projects. The textbook dwelled too much into information technology processes which are irrelevant to our hardware based project.

References

[1] *Three Methods of Noise Figure Measurement*, Maxim, Retrieved August 1, <http://www.maxim-ic.com/app-notes/index.mvp/id/2875>.

[2] G. Shelly, H. Rosenblatt, *Systems Analysis and Design*, 9th ed., Boston: Course Technology, 2012, p. 2-138.

ELEC/CENG 399 Design Project I
Final Project Report Evaluation Form

To be filled by students:
Project title: ECOSat Communications Subsystem: RF Division
Group #: 11
Group members: Jarrah Bergeron and Kris Dolberg
Supervisor(s): Peter Driessen

To be filled by the supervisor(s):		
Progress report distributed to the supervisors for grading: Friday, August 3, 2012		
Please complete the progress report grading by: **Friday, August 17, 2012**		
Please refer to the rubric for grading.		
Topics		Grade [%]
[5%]Chapter 1, Goals :		
[10%]Chapter 2, Progress Overview:		
[25%]Chapter 3, Detailed Project Description:		
[25%]Chapter 4, Workload Distribution and Achievements:		
[10%]Chapter 5, Project Discussion:		
[5%]Chapter 6, Summary and Future Works:		
Subtotal [80%]:		**0.0**
To be filled by the instructor:		
[20%]Appendix A: Textbook Review	[10%]Write the textbook review in a clear	
	[10%]Meet minimum page requirement (2 pages):	
	Subtotal [20%]:	**0.0**
Total [100%]:		**0.0**

Comments by the supervisor: