

MODE-MATCHING ANALYSIS OF SUBSTRATE-INTEGRATED WAVEGUIDE CIRCUITS

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ABSTRACT

A mode-matching approach is presented for the analysis of substrate-integrated waveguide (SIW) circuits. The numerical technique takes advantage of recently developed fabrication techniques employing rectangular-shaped via holes. Discontinuity models involving all-dielectric waveguides and sections with arbitrary numbers of vias are presented and combined into a powerful analysis tool which can be used straightforwardly for the design of SIW components. The influence of the overall substrate width on the circuit performance is investigated. It is found that the computational domain can be significantly reduced without impacting on the computed performances. A design example involving a back-to-back impedance transformer is presented. The results are verified by comparison with the commercially available field solver CST Microwave Studio.

Index Terms— Substrate-integrated waveguide technology, numerical modeling, mode-matching techniques, computer-aided design.

1. INTRODUCTION

Substrate-integrated waveguide (SIW) circuits form a reasonable compromise between microstrip and waveguide technologies [1]. Their advantages made an impact in the lower millimeter-wave frequency range [2], [3] where microstrip components are increasingly lossy and waveguides too bulky.

Although a large variety of different SIW components have been presented in the recent literature, actual circuit designs involve commercial field solvers such as Ansoft HFSS or CST Microwave Studio. While the accuracy of such packages is undisputed, their numerical effort in circuit optimization is tremendous and time-consuming. Thus other techniques, which are more tailored to waveguide-type modeling, have emerged. The Mode-Matching Technique (MMT) is used for dispersion analysis of SIWs [4], and the Boundary Integral – Resonant Mode Expansion (BI-RME) method for equivalent-circuit extraction [5]. One of the reasons for not using such techniques in the full-wave synthesis and optimization of SIW circuits is the circular shape of the via holes with respect to the Cartesian coordinate system of the principle SIW discontinuities

which form the SIW component. With the emergence of new fabrication techniques, however, more arbitrary via shapes become feasible [2], [6], and rectangular and square via shapes have successfully been implemented [7].

Therefore, this paper presents a MMT approach for the analysis and design of SIW components with square via holes. The numerical procedure follows fundamental MMT principles [8] and uses an all-dielectric waveguide as a low-reflective SIW feed [9].

2. THEORY

Fig. 1 shows a SIW formed by ten equally spaced square via hole pairs with equivalent-width all-dielectric waveguide ports at both ends.

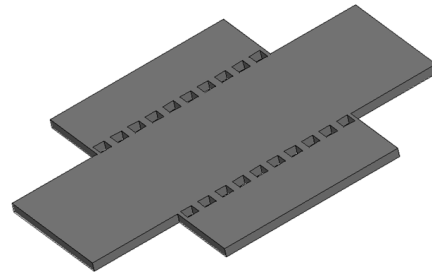


Fig. 1. Substrate-integrated waveguide with square via holes and all-dielectric waveguide ports.

In order to analyze such a circuit with a MMT procedure, two basic discontinuities need to be solved: first, the transition between two all-dielectric waveguides of different width (Fig. 2a) and, secondly, a number of rectangular vias embedded in an all-dielectric waveguide (Fig. 2b).

Since the substrate height is usually much smaller than the waveguide widths, a modal analysis based on TE_{m0} modes is sufficient. Following procedures in [8], the vector potentials in regions $v=-1, 0, n$ ($n=1$ to N) (c.f. Fig. 2) can be written as

$$A_{hz}^{-1} = \sum_{\ell} \sqrt{Z_{\ell}^{-1}} A_{\ell}^{-1} \cos \left\{ \frac{\ell \pi}{a_{-1}} \left(x + \frac{a_{-1}}{2} \right) \right\} \cdot \left[F_{\ell}^{-1} \exp(-jk_{z\ell}^{-1}z) + B_{\ell}^{-1} \exp(+jk_{z\ell}^{-1}z) \right] \quad (1a)$$

$$A_{hz}^0 = \sum_m \sqrt{Z_m^0} A_m^0 \cos \left\{ \frac{m\pi}{a_0} \left(x + \frac{a_0}{2} \right) \right\} \cdot \left[F_m^0 \exp(-jk_{zm}^0 z) + B_m^0 \exp(+jk_{zm}^0 z) \right] \quad (1b)$$

$$A_{hz}^n = \sum_k \sqrt{Z_k^n} A_k^n \cos \left\{ \frac{k\pi}{a_n} (x - x_n) \right\} \cdot \left[F_k^n \exp(-jk_{zk}^n z) + B_k^n \exp(+jk_{zk}^n z) \right] \quad (1c)$$

where F and B are the forward and backward travelling wave amplitudes, respectively; k_z are the propagation constants, A the normalization coefficients and Z the wave impedances, given by [8]

$$\begin{aligned} k_{zi}^v &= \sqrt{\left(\frac{\omega}{c}\right)^2 \epsilon_r - \left(\frac{i\pi}{a_v}\right)^2} \\ A_i^v &= \frac{a_v}{i\pi} \sqrt{\frac{2}{a_v h}} \\ Z_i^v &= \frac{\omega \mu_0}{k_{zi}^v} = \frac{1}{Y_i^v} \end{aligned} \quad (2);$$

c is the speed of light and h the substrate height.

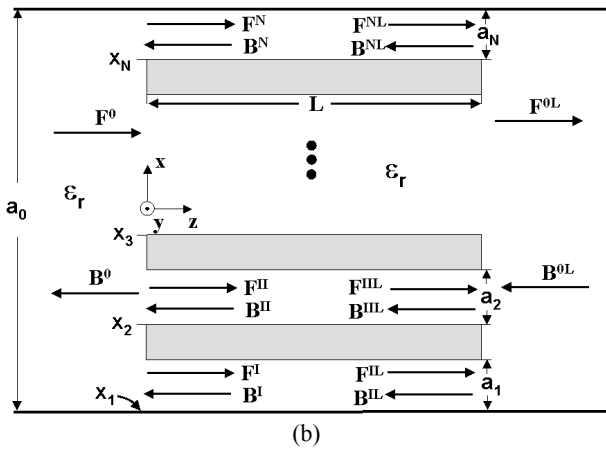
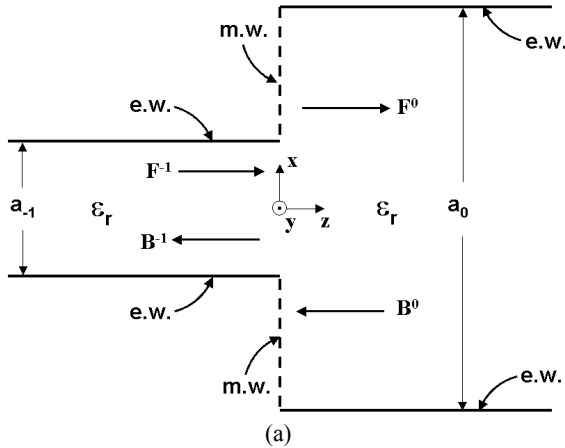


Fig. 2. Discontinuities involved in the MMT process.

Considering the magnetic-wall boundary conditions for the field-matching process in Fig. 2a, the coupling matrix for this discontinuity is

$$M = \text{Diag} \left\{ \sqrt{Y_\ell^{-1}} \right\} (J) \text{Diag} \left\{ \sqrt{Z_m^0} \right\} \quad (3a)$$

with

$$(J)_{\ell m} = \frac{2}{\sqrt{a_{-1} a_0}} \int_{-a_{-1}/2}^{+a_{-1}/2} \sin \left\{ \frac{\ell\pi}{a_{-1}} \left(x + \frac{a_{-1}}{2} \right) \right\} \sin \left\{ \frac{m\pi}{a_0} \left(x + \frac{a_0}{2} \right) \right\} dx \quad (3b)$$

from which the modal scattering matrix follows straightforwardly

$$\begin{bmatrix} B^{-1} \\ F^0 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} F^{-1} \\ B^0 \end{bmatrix} \quad (4a)$$

$$S_{11} = [MM^T + U]^{-1} [MM^T - U]$$

$$S_{12} = 2[MM^T + U]^{-1} M = S_{21}^T \quad (4b)$$

$$S_{21} = M^T [U - S_{11}] = S_{12}^T$$

$$S_{22} = U - M^T S_{12}$$

where U is the unit matrix, and T means transposed.

The discontinuity in Fig. 2b involves N coupling matrices, capturing the coupling from region 0 to each region n (n=1 to N). However, since the number of modes in region 0 is higher than that in region n, the column-type coupling matrices are arranged in one large matrix with the single right side vector holding all forward and backward traveling wave amplitudes F^n and B^n . The individual coupling matrices are

$$M^n = \text{Diag} \left\{ \sqrt{Y_m^0} \right\} (J^n) \text{Diag} \left\{ \sqrt{Z_k^n} \right\} \quad (5a)$$

with

$$(J^n)_{mk} = \frac{2}{\sqrt{a_0 a_n}} \int_{x_n}^{x_n + a_n} \sin \left\{ \frac{m\pi}{a_0} \left(x + \frac{a_0}{2} \right) \right\} \sin \left\{ \frac{k\pi}{a_n} (x - x_n) \right\} dx \quad (5b)$$

With all N output-port amplitudes combined in a single-port vector, the scattering matrix of the N-furcated waveguide discontinuity is as in (4b). The final modal scattering matrix of N via holes in an all-dielectric waveguide (Fig. 2b)

$$\begin{bmatrix} B^0 \\ F^{0L} \end{bmatrix} = \begin{bmatrix} S_{11v} & S_{12v} \\ S_{21v} & S_{22v} \end{bmatrix} \begin{bmatrix} F^0 \\ B^{0L} \end{bmatrix} \quad (6)$$

is obtained by cascading a single diagonal matrix containing the transmission parameters D^n of every single region n=1 to N up to the center location ($z=L/2$) of the via holes (Fig. 2b)

$$D^n = \text{Diag} \left\{ \exp \left(-jk_{zk}^n \frac{L}{2} \right) \right\} \quad (7)$$

and flipping the resulting scattering matrix, i.e., cascading the same scattering matrix but with input and output ports interchanged.

The final overall modal scattering matrix of the structure in Fig. 1 is then obtained by following general procedures of cascading scattering matrices, e.g. [8].

3. RESULTS

The first step in designing a substrate-integrated waveguide is to specify the substrate and the frequency range. For this work, the substrate is chosen as RT Duroid 5880 with a relative permittivity of $\epsilon_r=2.2$ and a substrate height of $h=508\mu\text{m}$. For the frequency range of 18 GHz to 28 GHz, a SIW cutoff frequency of approximately 15 GHz was chosen which, following guidelines in [10], results in circular vias of diameters of 0.72mm and center-to-center (longitudinal) spacings of 1.02mm. The (transverse) width of the SIW measured between the centers of the via holes is $a_{\text{via}}=7.28\text{mm}$. The equivalent waveguide width of such an arrangement is $a_{\text{equ}}=6.71\text{mm}$ according to [11]. In order to employ the MMT procedure outlined in the previous section, the circular vias are translated to square ones based on the assumption that the area of the via hole be preserved. Thus all via holes used in this work have a cross section of 0.64mm x 0.64 mm. Moreover, all examples presented below have been obtained using all modes up to 300 GHz for the modeling of discontinuities and modes up to 150 GHz for the combination of modal scattering matrices.

The quality of a SIW circuit and its transition to an all-dielectric waveguide of width $a_1=a_{\text{equ}}$ (Fig. 2a) is measured by the reflection coefficient seen into the ports. Fig. 3 depicts the performance of the circuit shown in Fig. 1.

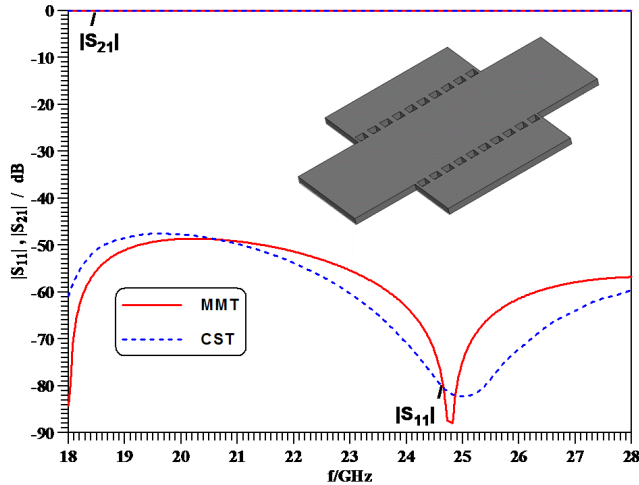


Fig. 3. Performance of the circuit shown in Fig. 1 and comparison between this method (solid lines) and CST (dotted lines).

The reflection coefficient is -50 dB or better, and the results are confirmed by the commercial field solver CST Microwave Studio. For the CST simulations, the accuracy is set to the minimum limit of -80 dB. The agreement between the MMT approach presented here and the CST results is excellent and remarkable, especially considering the fact that the two curves that are compared are both at such a low level. This result instills confidence in the design of future SIW components. It is worthwhile to point out that a different computation of the equivalent waveguide width as

recently published in [12] results in a reflection level that is 10 dB higher than that shown in Fig. 3 and thus is not as well matched to the SIW as the results obtained from [11].

Another critical point involving the computational domain is associated with the substrate width of the via-holed section (a_0 in Fig. 2). Therefore, the performance of the circuit in Fig. 3 has been re-evaluated using different substrate widths normalized to the center-to-center SIW width a_{via} . The resulting performances are shown in Fig. 4. It is observed that the outer substrate walls can be located very closely to the via holes and that the performance is nearly independent of their actual location. Thus the computational domain for SIW circuit modeling can be reduced. As the substrate wall distance is increased, a limit is reached ($a_0/a_{\text{via}}=3$ in Fig. 4) when fields are propagating outside of the SIW and recombine with those in the actual SIW. Then resonance peaks as the one observed at 24.6 GHz in Fig. 4 occur and will affect the accuracy of the MMT modeling process. As the substrate width is further increased (not shown here), more resonance peaks appear and make it difficult to obtain a reliable performance evaluation of a SIW circuit.

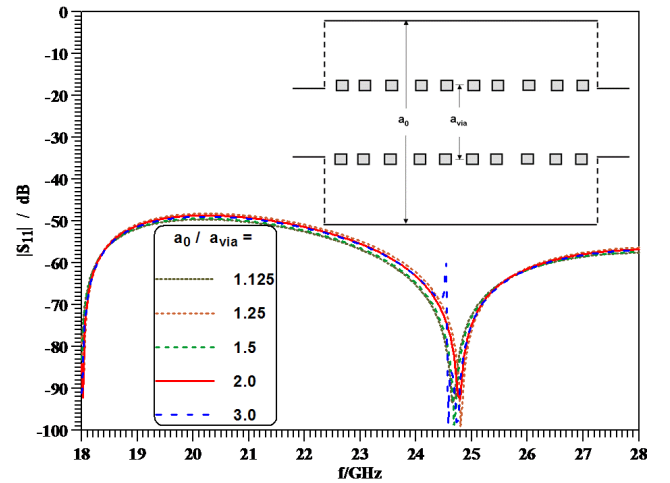


Fig. 4. Influence of the substrate width on the performance of the circuit in Fig. 1.

As a design example, Fig. 5 shows the performance of a back-to-back connection of a two-section impedance transformer in SIW technology. The transformer has been designed using a standard H-plane waveguide transformer synthesis routine [8]. As the exact corners and straight walls of the waveguide model cannot exactly be reproduced by the via holes in the SIW component, fine optimization of transformer lengths and width becomes necessary. For this purpose, additional vias are added at the transitions between different waveguide widths so that the width can be optimized without creating large spaces between via holes. As shown in Fig. 5b, excellent agreement is observed between the results of the MMT approach and those of CST, thus verifying the correctness of the MMT modeling process presented in this paper. Note that all S_{11} levels are below -40 dB.

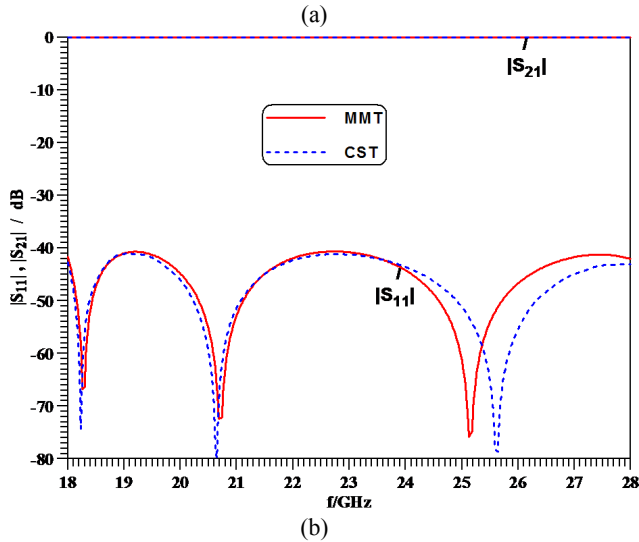
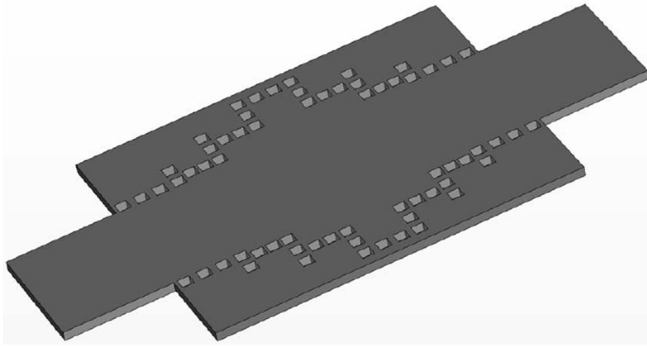


Fig. 5. A back-to-back two-section impedance transformer (a) and performance comparison (b) between this method (solid lines) and CST (dotted lines).

4. CONCLUSIONS

A modeling approach for the analysis and design of SIW circuits is presented. The mode-matching procedure takes advantage of via holes of square cross sections and captures the modal interactions of all individual discontinuities involved. An advantage of this technique is that the actual substrate width can be reduced to extend just a fraction beyond the vias which gives rise to a reduction in the overall computational domain.

Examples include a SIW section fed by all-dielectric waveguide ports and a back-to-back connection of a two-section impedance transformer. Excellent agreement with results obtained from CST Microwave Studio verifies the modeling process presented in this paper.

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