

Design of a Low-Input-Voltage Converter for Thermoelectric Generator

John M. Damaschke

Abstract—Low-grade exhaust heat is used to provide a reliable and independent power source for instrumentation circuitry by means of a thermoelectric generator (TEG). A design of a self-starting dc–dc converter is developed and optimized for very-low-input voltages (below 300 mV) in order to allow operation at temperature differences of 20 °C and less. A prototype is built, and the results are experimentally verified.

Index Terms—DC–DC power conversion, losses, low power, low voltage, power generation, self-starting, thermoelectric generator, voltage control.

I. INTRODUCTION

ELECTRONIC instrumentation is used to monitor and control a variety of processes. It plays an important role in a chemical enterprise, as well as in many other places. Usually, the circuit is supplied with power from a standard outlet or by a battery. In many cases, it is, however, not feasible to run a cable from the power source to the location of application because of the rough environment prevailing in such plants, especially for small, low-power applications like sensors. Therefore, an independent and reliable power source is needed. One solution is to use a thermoelectric generator (TEG) to convert low-grade heat energy into electricity which powers the application or charges a battery backup. Typically, exhaust heat from already available sources can be used, e.g., from engines or warm pipes. Yet, the temperature difference from this kind of sources may be very low, e.g., 20 °C. For this temperature difference, a high-performance bismuth telluride thermoelectric module provides an open-circuit voltage in the order of 300 mV at an internal resistance of about 130 mΩ. In order to get a sufficient voltage output to power the application, a large array of high-performance TEG's would be needed. With a single high-performance module costing an average of several hundreds of dollars, this option often becomes economically unviable. To reduce costs, especially for low-power applications, a single cell could be used where the output power is transformed to the 5-V level.

The theory of dc–dc converters is well known [1], [2], and their design is still the subject of many journal publications. However, designs for very low voltages, as in this application,

Paper IPCSD 97–31, presented at the 1996 IEEE Applied Power Electronics Conference and Exposition, San Jose, CA, March 3–7, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. This work was supported in part by Dr. J. Bornemann of the University of Victoria. Manuscript released for publication May 7, 1997.

The author is with the Department of Electrical and Computer Engineering, University of Victoria, Victoria, B.C., V8W 3P6 Canada.

Publisher Item Identifier S 0093-9994(97)06560-2.

have not been reported yet [3], [4]. The design of the conversion circuit is a major task and the main contribution of this work. The TEG provides a very low voltage at a high current. This causes, even for a reasonably low internal resistance of the converter, a very large relative voltage drop and, therefore, a very low efficiency. Also, the power consumed by the converter itself for regulating and switching is much more critical because of the little total power available. Besides, to provide reliable and maintenance-free operation, the circuit needs to be self starting. This is a challenge when dealing with supply voltages below 300 mV. Moreover, it is desirable to base the converter on standard available circuitry to minimize the effort of the manufacturing, especially when produced in low quantities. Hence, standard converter design cannot be used in this case.

The purpose of this work is to develop a circuit which can easily be built, is reliable and self starting, and converts the above-mentioned input power for $\Delta T = 20$ °C to a stabilized 5-V level with as high an efficiency as possible. The problems arising hereby are discussed in detail in Section II and, from that, the used devices are deducted, and the novel twin converter is introduced to achieve the required performance. In Section III, the final circuit is presented. A prototype of the circuit has been built, and Section IV shows the obtained measurements and discusses the results.

II. CIRCUIT CONSIDERATIONS

It is understood that all dc–dc converters are based on switching a current through an inductor. The main consideration in the design consists in deciding which kind of switching device to use.

Most converters employ high-power MOSFET's as switching devices. Their very low on resistance and their zero gate current lead to very low losses. Unfortunately, a rather high gate voltage is needed for switching them and, therefore, they cannot be used in a self-starting design.

Bipolar junction transistors (BJT's) need a voltage of about 0.7 V for switching them on. In addition, they typically have a considerable collector-emitter voltage drop. This leads to a very poor efficiency. One could mount them upside down to eliminate the voltage drop, but this would yield a high base current which increases losses. Therefore, this kind of device is also excluded from an efficient design.

The self-starting requirement of the circuit certainly demands a normally on device. This is obvious, as no output can be expected without a current flowing at the beginning, and no device can be switched on by a voltage of less than

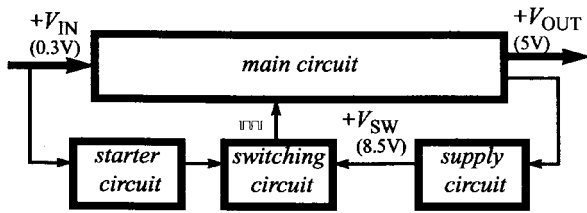


Fig. 1. Block diagram of the complete circuit. The voltages during regular operation are given in parentheses.

300 mV. On the other hand, normally on devices have very high on resistances, typically at least 3Ω . This limits the maximum achievable power output to less than 10 mW at best. With the internal resistance of the used TEG of about $130 \text{ m}\Omega$, the theoretically available power is 173 mW. In order to get close to this value at all, the resistance of the switching device has to be much lower than the TEG's internal resistance.

Considering all factors, it becomes apparent that the requirements cannot be achieved in one single circuit. This gave rise to the twin design consisting of two converters, the *main circuit* and the *starter circuit*. For the starter circuit, a normally on device with as low an on resistance as possible was chosen, i.e., the N-channel FET JFET J105 with $R_{\text{on}} = 3 \Omega$. In the main circuit, the on resistance is the limiting factor for the overall efficiency of the conversion. The high-performance high-power MOSFET SMP 60N06-18, which has an on resistance not exceeding $18 \text{ m}\Omega$ (typically $14 \text{ m}\Omega$) and a fairly low gate charge, was chosen. During the initial phase, the MOSFET is switched off, and the main circuit is dysfunctional. All the energy is pumped into the starter circuit, which provides enough energy to the switching circuit to initialize the main circuit. As soon as this circuit is operational, the much lower on resistance of the MOSFET basically short circuits the input of the starter circuit, and the energy almost exclusively flows into the main circuit.

III. CIRCUIT DESIGN

Fig. 1 shows the block diagram of the complete circuit which consists of the *main circuit*, the *starter circuit*, the *switching circuit*, and the *supply circuit*.

- The starter circuit provides voltage at the beginning to initialize the conversion.
- The main circuit contains the main converter which provides the output voltage with high efficiency.
- The switching circuit switches the main circuit and, in this way, regulates the output.
- The supply circuit generates the 8.5 V for the switching circuit from the 5-V output.

In the following, the operation of the circuits will be outlined in detail. The complete circuit diagram is shown in Fig. 4.

A. The Starter Circuit

The starter circuit is similar to those used in heart pacemakers, e.g., [5]. At the beginning, there is no charge on the capacitor C_3 (see Fig. 4). The current through the normally

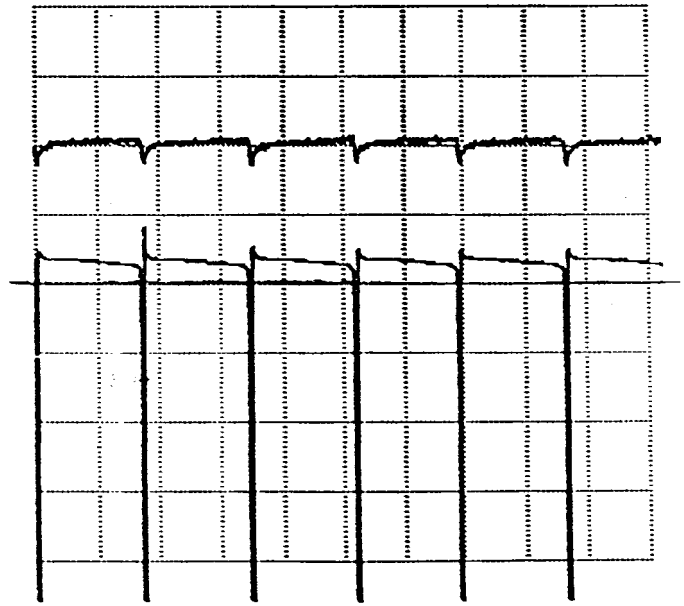


Fig. 2. Gate voltage (lower line, 1 V/div) and drain current (upper line, 50 mA/div) of transistor T_1 in the starter circuit. The timebase is set to 0.5 ms/div.

on JFET T_1 and the transformer induces a negative voltage at the secondary winding of the transformer. Thus, the capacitor C_3 is charged to a negative voltage, where the pn-transition of the transistor acts as a diode. As the current through the primary winding approaches saturation, the voltage across the secondary decreases, hence, leading to a drop in the gate voltage of the transistor T_1 . The transistor starts turning the current through the transformer off which leads to a positive voltage at the secondary, and the negative voltage at the gate of T_1 quickly drops. This diminishes the current through the transformer and leads to a further drop in the gate voltage, and so forth. This way, T_1 is totally turned off very quickly, leading to zero current through the primary winding of the transformer and, thus, to zero voltage across the secondary winding. This smaller negative voltage at the gate of T_1 leads to an increase in the current through the primary winding of the transformer and, thus, through the coupling of the transformer, to a further increase in the gate voltage. The transistor is turned on very quickly and remains conducting until the current approaches saturation again. This yields the waveform as shown in Fig. 2. One can see the very short off cycle of the transistor and the high voltage induced during that time interval. The resistor R_1 ensures that C_3 is discharged at the beginning. Since the switching circuit requires a positive supply voltage, the voltage across the capacitor could not be used as the output. Instead, a third winding was added. The turn ratio is critical for the proper functioning of the circuit. It is found that the input voltage, at which the circuit starts oscillating, is a linear function of the turn ratio between the first and the second winding of the transformer, as long as the resistance of the secondary winding does not become too large.

The starter circuit only supplies the switching circuit with power until the main circuit starts working. Hence, the output need not be regulated.

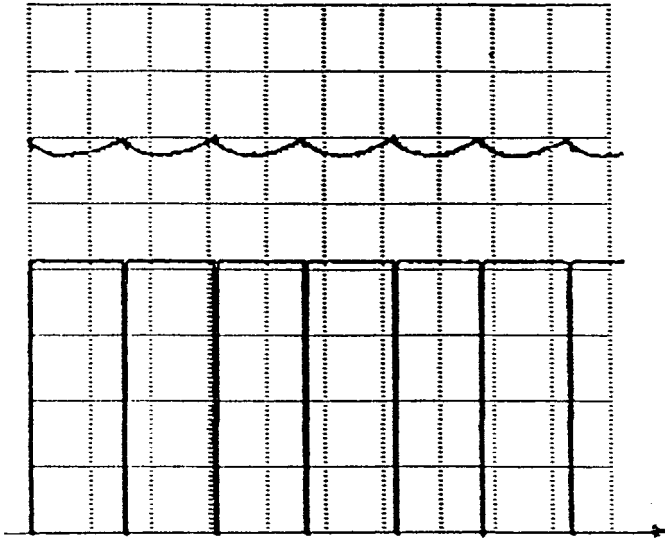


Fig. 3. Gate voltage (lower line, 2 V/div) and drain current (upper line, 1 A/div) of transistor $T2$ in the main circuit. The timebase is 50 μ s/div.

B. The Main Circuit

The main circuit in Fig. 4 is a modified boost converter (see [1]). In order to achieve a high efficiency, a very-low-input resistance is essential. The electric path through the primary winding and the MOSFET $T2$ was made as short as possible. The paths on the stripboard were reinforced by wire. The primary winding consists of three turns on a toroidal body. Six wires with a diameter of 0.9 mm were connected in parallel. This way, the input inductance became 70 μ H, and the dc input resistance, with $T2$ switched on, less than 15 m Ω . Also, the 0.3 V of the TEG with its 130-m Ω internal resistance led to a saturation current of the coil of more than 2 A. Fig. 3 shows the gate voltage and the drain current of the main circuit.

The first design did not incorporate the second transistor $T3$. This resulted in a voltage of approximately 0.7 V across the diode $D2$. At an output voltage of 5 V, thus, a considerable portion of the power was absorbed in the diode. Hence, the second MOSFET $T3$ and the secondary winding were introduced. Whenever $T2$ is switched off, the transformer turns on $T3$. This practically eliminates the voltage across the diode, thus significantly increasing the maximum achievable output power.

It is commonly known (see e.g., [1]) that the output voltage of a boost converter can be estimated by

$$V_{\text{OUT}} = \frac{V_{\text{IN}}}{1 - dc} \quad (1)$$

where the duty cycle dc is the ratio of the on time of the MOSFET to the period length. Equation (1) has its limits of validity, especially for dc close to 1. Theoretically, a dc of 1 yields an infinite output voltage according to (1). Physically, however, it leads to a short circuit at the input, i.e., zero output. It is the task of the switching circuit to control dc so that the output voltage V_{OUT} is regulated to 5 V.

C. The Switching (Regulating) Circuit

The switching/regulating circuit as shown in Fig. 4 uses only one low-power dual CMOS comparator. Comparator A

generates the modified sawtooth voltage, as shown in Fig. 5. The resistors $R2$ and $R3$ provide an almost fixed voltage V^+ at the positive input. Let us assume that the capacitor $C6$ is initially discharged. This means that the output of the comparator is open. Now, $C6$ is charged up through the pull-up resistor $R5$ and the feedback resistor $R4$. Note that the pull-up resistor $R5$ is chosen much larger than the feedback resistor $R4$. So, when the voltage V^- across the capacitor $C6$ reaches V^+ , the output of the comparator switches to ground, and $C6$ discharges very quickly through the small resistor $R4$. Hence, the comparator switches to ground only for a very short period of time during which the output voltage becomes zero. Then, the output becomes open again, and the voltage at the output is determined by the voltage V^- of the capacitor $C6$ and the voltage divider $R4$ and $R5$, i.e., approximately V^- . The resistors $R6$ and $R7$ also represent a voltage divider which causes the voltage at the positive input of comparator B to be slightly lower than the output voltage of comparator A . Due to the capacitor $C7$, this is true even when the output of comparator A is zero volts, resulting in a slightly negative voltage of about -150 mV at the positive input of comparator B for a very short time interval. This leads to the asymmetric shape of the sawtooth voltage, as seen in Fig. 5. However, it has to be ensured that the input voltage at the converter does not drop below -300 mV, since it otherwise could be damaged.

Comparator B now compares this voltage with the output voltage V_{OUT} of the main circuit. Whenever the sawtooth voltage is lower than the output voltage V_{OUT} , the voltage at the gate of the MOSFET $T2$ is connected to ground, otherwise to $+V_{\text{SW}}$. This way, the duty cycle dc of the main converter is changed. A high output voltage yields a smaller dc , which, as we can see from (1), leads to a lower output. The opposite happens for a low output voltage. In particular, zero output voltage leads to a dc which is given by the shortest possible off time. Now we see why it is important that the sawtooth voltage goes below zero for a very short time interval. In this way, it is always ensured that $T2$ is at least switched off for a minimum time, thus avoiding a short circuit at the converter input. In this design, the minimum off time is 2 μ s. With the oscillating frequency of the sawtooth generation of 12.8 kHz, this is equivalent to a maximum dc of 97.5%. Depending on the load, the input voltage will vary between approximately 0.3–0.15 V, thus requiring a duty cycle between 94%–97%. We can see from Fig. 5 that this leads to a very small difference in the output voltage.

The transistors $T4$ and $T5$ finally are used to speed up the switching of the output of the converter, without lowering the value of the pull-down resistor $R8$. This would lead to higher losses.

Altogether, the circuit draws a current of less than 1 mA, or, in terms of power, consumes about 8 mW when operated at a voltage V_{SW} of 8.5 V.

D. The Supply Circuit

It has been mentioned before that the on resistance of the MOSFET $T2$ is crucial for high efficiency. This resistance

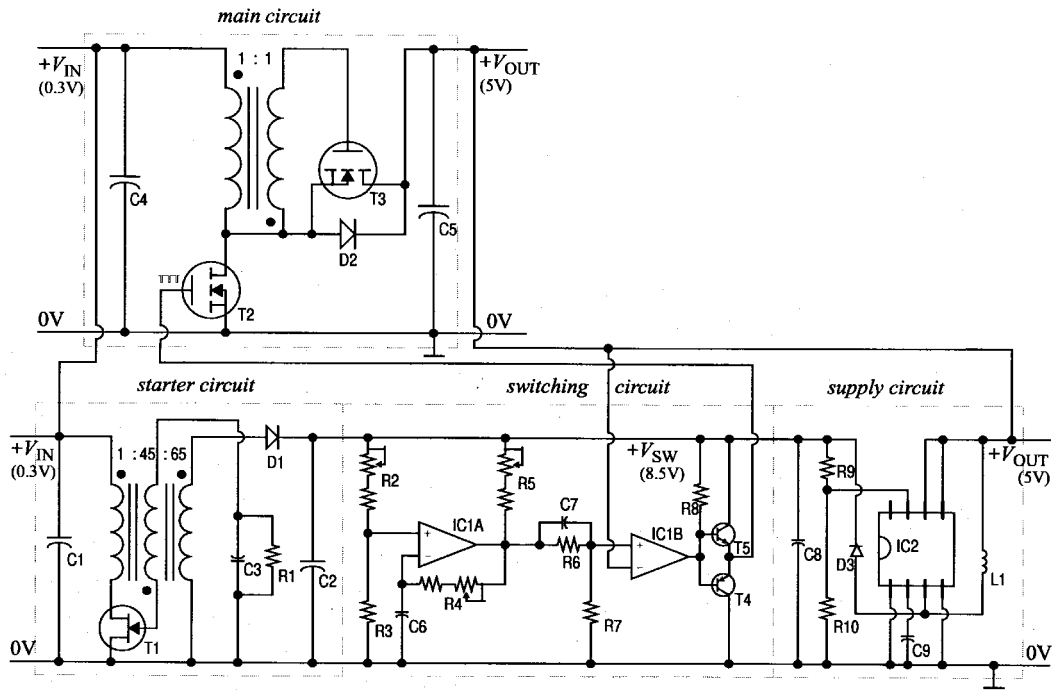


Fig. 4. Circuit diagram of the complete circuit. The voltages during regular operation are given in parentheses. The values of the devices are given as follows: starter circuit— $R1 = 1\text{ M}\Omega$, $C1 = 1\text{ mF}$, $C2 = 470\text{ }\mu\text{F}$, $C3 = 1\text{ nF}$, $D1 = 1\text{N4148}$, $T1 = \text{J105}$; main circuit— $C4 = 2.2\text{ mF}$, $C5 = 1\text{ mF}$, $D2 = 1\text{N4001}$, $T2 = T3 = \text{SMP } 60\text{N06-18}$; switching circuit— $R2 = 350\text{ k}\Omega$, $R3 = 1\text{ M}\Omega$, $R4 = 1.8\text{ k}\Omega$, $R5 = 32\text{ k}\Omega$, $R6 = 270\text{ k}\Omega$, $R7 = 1\text{ M}\Omega$, $R8 = 2.2\text{ k}\Omega$, $C6 = 10\text{ nF}$, $C7 = 1\text{ nF}$, $T4 = \text{BC313}$, $T5 = \text{BC182}$, $\text{IC1} = \text{TLC372CP}$; supply circuit— $R9 = 1\text{ M}\Omega$, $R10 = 182\text{ k}\Omega$, $C8 = 100\text{ }\mu\text{F}$, $C9 = 47\text{ pF}$, $L1 = 1.7\text{ mH}$, $D3 = 1\text{N4148}$, $\text{IC2} = \text{MAX630}$.

becomes smaller for a higher gate-source voltage, i.e., a higher operating voltage of the switching circuit. On the other hand, this also leads to a higher power consumption of the switching circuit which, in terms of the output power, can be considered as losses. For this particular design, it has proven most efficient to use a switching voltage of 8.5 V by employing a third converter. Since the power consumption of the switching circuit is small, the efficiency of this conversion is not so critical. In addition, the switching circuit requires a constant output voltage in order for the regulation to work. Hence, the MAX630 integrated circuit was used to generate a regulated voltage of 8.5 V out of the output of the main circuit. This integrated circuit contains an oscillator, a comparator, a reference voltage, and a MOSFET. Fig. 4 shows the circuit diagram of the supply circuit. The output voltage is divided by the resistors $R9$ and $R10$ and compared to the 1.31-V internal reference voltage. Whenever the voltage is too low, the oscillator switches the MOSFET periodically on and off until the desired voltage of, in this case, 8.5 V is reached. The capacitor $C9$ sets the oscillator frequency to 37.5 kHz. Due to the high on resistance of the onboard MOSFET of about $3\text{ }\Omega$, a higher efficiency can be reached when using a large inductance $L1$. Also, the maximum peak current must not be exceeded. On the other hand, the inductance must be small enough to be able to generate the 8.5 V from as low an input voltage as possible. Good results are achieved for $L1 = 1.7\text{ mH}$.

This circuit could be powered from the 5-V output of the main circuit or from its own 8.5-V output. The lower operating voltage lowers the efficiency of the conversion, but also the power consumption of the converter. Since the circuit provides

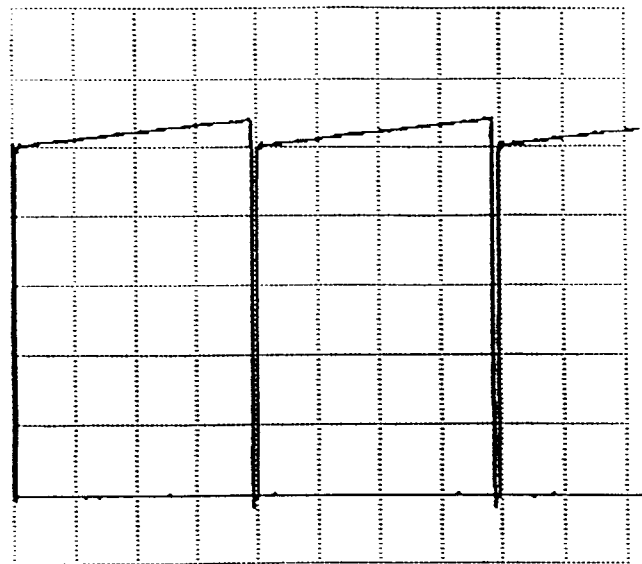


Fig. 5. Diagram of the modified sawtooth voltage generated by the switching circuit. The y axis shows the output of comparator A (1 V/div), and the timebase is 20 $\mu\text{s}/\text{div}$.

only about 8 mW for the switching circuit, it has proven more efficient in this case to power the supply circuit directly from the 5-V output. In this way, the supply circuit consumed a total power of 3 mW.

IV. RESULTS

Fig. 6 shows the results obtained from the circuit when connected to the TEG as a power supply for $\Delta T = 20\text{ }^\circ\text{C}$.

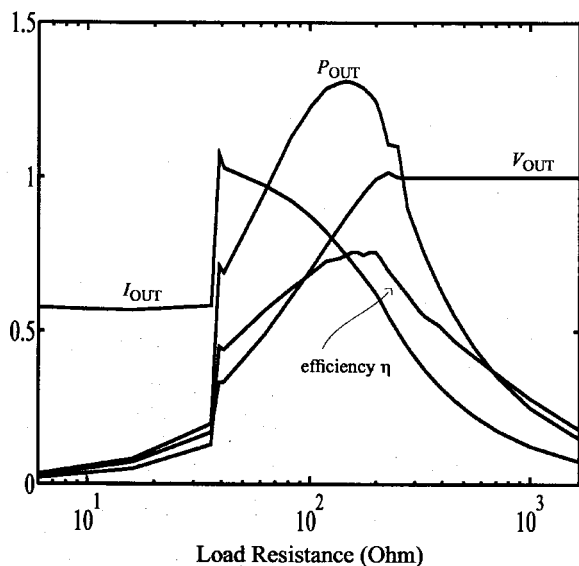


Fig. 6. Normalized output power $P_{OUT}/100$ mW, efficiency η , normalized output voltage $V_{OUT}/5$ V, and normalized output current $I_{OUT}/40$ mA of the converter as a function of the load resistance.

The overall efficiency reaches up to 76%. We can see that the output voltage stays very constant until the load becomes too high. For a load of 175Ω , an output power of 131 mW is achieved, and practically all of the maximum available power from the TEG of about 170 mW enters the circuit. The switching/regulation circuit and the supply circuit consume 11 mW, while 13 mW are dissipated in the resistance of the main circuit. The remaining 16 mW are attributed to switching losses in the main circuit and power creeping into the starter circuit the influence of which could not be completely removed.

It should be mentioned again that the input power is considered exhaust energy and, therefore, the power output was maximized instead of the efficiency. This explains the low efficiency for low loads. In particular, the MOSFET $T3$ (see Fig. 4), in parallel with the diode $D2$, in the main circuit, lowered the efficiency for low loads. This is due to two effects. First, a timing delay can cause the gate drives of $T2$ and $T3$ to overlap, leading to cross conduction. However, this occurs for a very short period of time only. Secondly, for the case with low load, the output voltage across the capacitor $C5$ remains at the desired 5 V and the main circuit operates at a low duty cycle. This means that $T2$ is switched on and $T3$ off for a short period of time only, leading to a relatively low current through the inductor. This is followed by a longer time interval where $T2$ is switched off and $T3$ is on, during which the current decreases exponentially. This leads not only to a current from the TEG to the circuit, but can also cause a current from the circuit back into the TEG, where losses occur in the internal resistance on the TEG. On the other hand, the transistor $T3$ considerably increases the maximum efficiency from the previous 60% to 76% and the maximum available power from 96 to 131 mW.

V. CONCLUSION

A new dc-dc converter circuit has been introduced. It offers an excellent performance in the low-voltage, low-power region. Results are shown when the converter is connected to a bismuth telluride thermoelectric module operating at a temperature difference of 20°C . This combination provides a reasonably stable output voltage of 5 V for up to 131-mW output load. This is 76% of the maximum available power and an excellent result for these low power levels. Another striking feature of the circuit is the self-starting capability, which makes the circuit practically maintenance free. Furthermore, the exclusive use of standard available devices makes the manufacturing very easy and economical, even in small numbers. Overall, the combination with the TEG shows a new kind of stable, economical and reliable off-line power source for low-power instrumentation and certainly will find many applications.

ACKNOWLEDGMENT

The author would like to express his gratitude to Dr. R. Shuttleworth of the University of Manchester and British Gas for initiating this work and for many helpful suggestions in the design phase. He is also indebted to Dr. J. Bornemann of the University of Victoria for his support in the preparation of the manuscript. Finally, he would like to mention Dr. J. Kim of the University of Victoria for his advice during the preparation of the paper.

REFERENCES

- [1] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converter, Applications and Design*. New York: Wiley, 1989.
- [2] K. Sum, *Switch Mode Power Conversion*. New York: Marcel-Dekker, 1984.
- [3] B. K. Bose, "Power electronics and motion control—Technology status and recent trends," *IEEE Trans. Ind. Applicat.*, vol. 29, pp. 902–909, Sept./Oct. 1993.
- [4] P. A. Thollot, *Power Electronics Technology and Applications 1993*. New York: IEEE Press, 1992.
- [5] M. Schaldach and S. Furman, *Advances in Pacemaker Technology*. Berlin: Springer-Verlag, 1975.



John M. Damaschke was born in Hamburg, West Germany, in 1968. He received the Vordiplom and Dipl.-Ing. degrees in electrical engineering from the Technical University Hamburg-Harburg, Germany, in 1990 and 1994, respectively. He is currently working toward the Ph.D. degree at the University of Victoria, Victoria, B.C., Canada.

During his studies, in 1993, he spent six months with the Department of Electrical Engineering, University of Manchester, Manchester, U.K., working in the area of power electronics, and from 1993 to 1994, he was with the Department of Electrical Engineering, University of Victoria. His research interests include numerical modeling in electromagnetics.