Ch.3 Input and Output

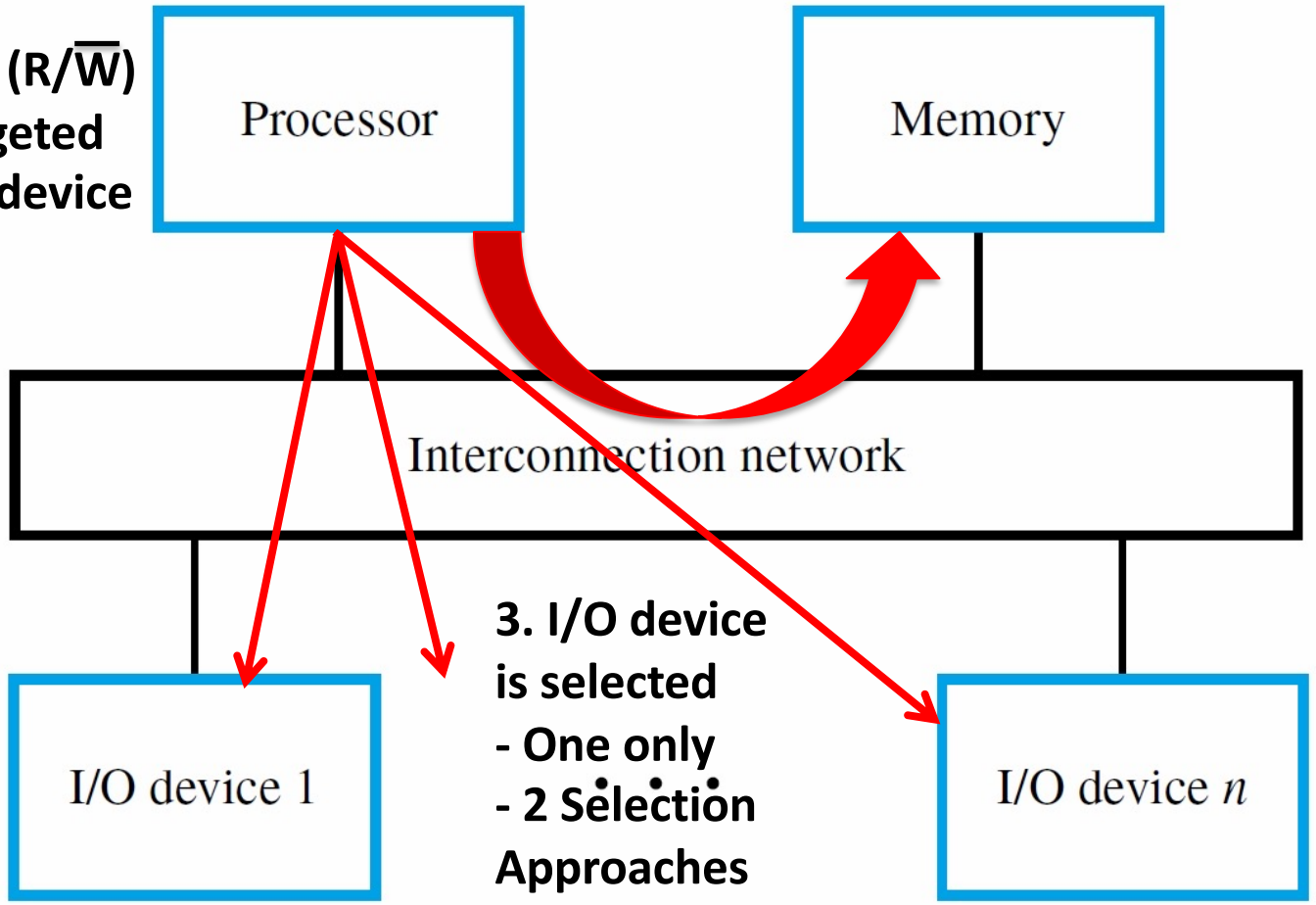
Topics

- Introduction: input and output (I/O)
  - Gaming industry devices
- **3.1.1: I/O device – system interface**
- 3.1.2: Program-controlled I/O transfer
- 3.2: Interrupt-based I/O
- 3.2.6: Exceptions

Fig.3.2 Interconnection Network

Processor: Master

1. Initiate transfer (R/$\overline{W}$)
2. Identify the targeted memory or I/O device

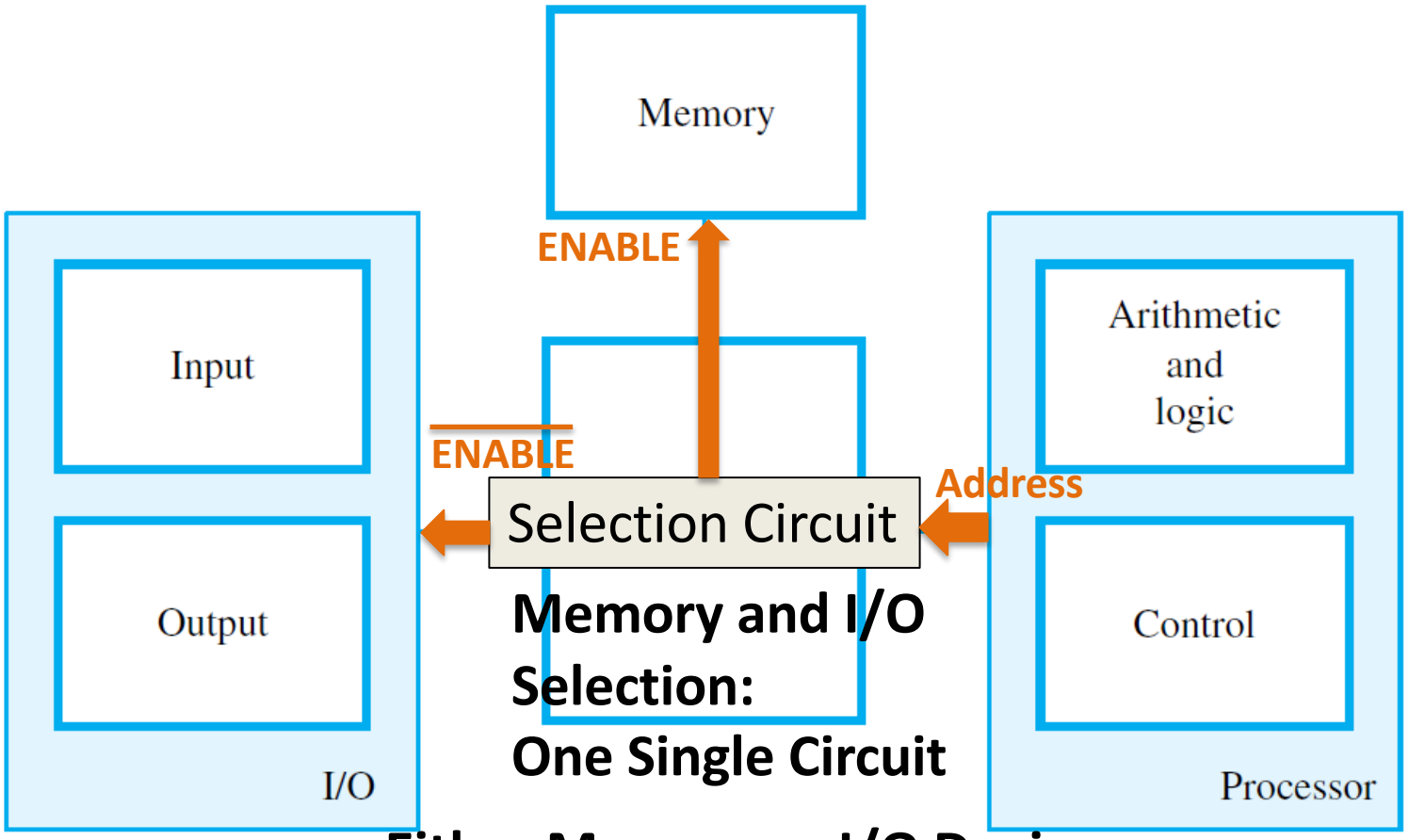


3. I/O device is selected
- One only
- 2 Selection Approaches

I/O Device: Slave

4. Respond to Master when selected

Selecting I/O Method 1: Memory-Mapped



Memory and I/O Selection:
One Single Circuit

Either Memory or I/O Device

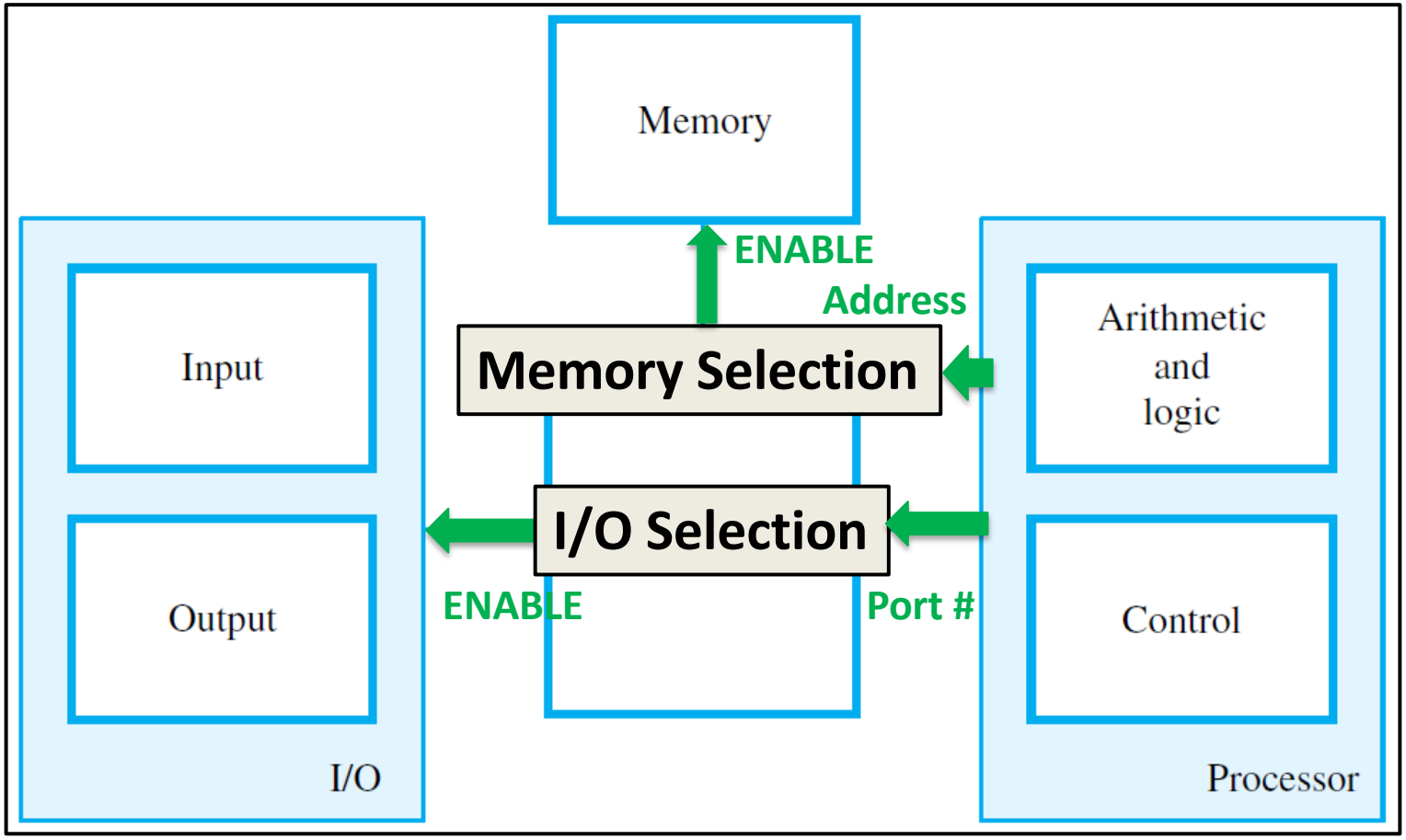
3.1 Memory Mapped I/O

- Locations of **I/O device's registers** are in the same address space as memory

Binary			Integer	
A2	A1	A0	Memory	I/O
0	0	0	0	
0	0	1	1	
0	1	0	2	
0	1	1	3	
1	0	0	4	
1	0	1	5	
1	1	0		Input-1
1	1	1		Output-1

- Use Load and Store (RISC), or Move (CISC) instructions
- Output: Move R0, Output-1 (Output-1=%111=7)
- Input: Load Input-1, R1 (Input1=%110=6)
- Memory addresses: [0..5] (note: 2 less memory locations for user)

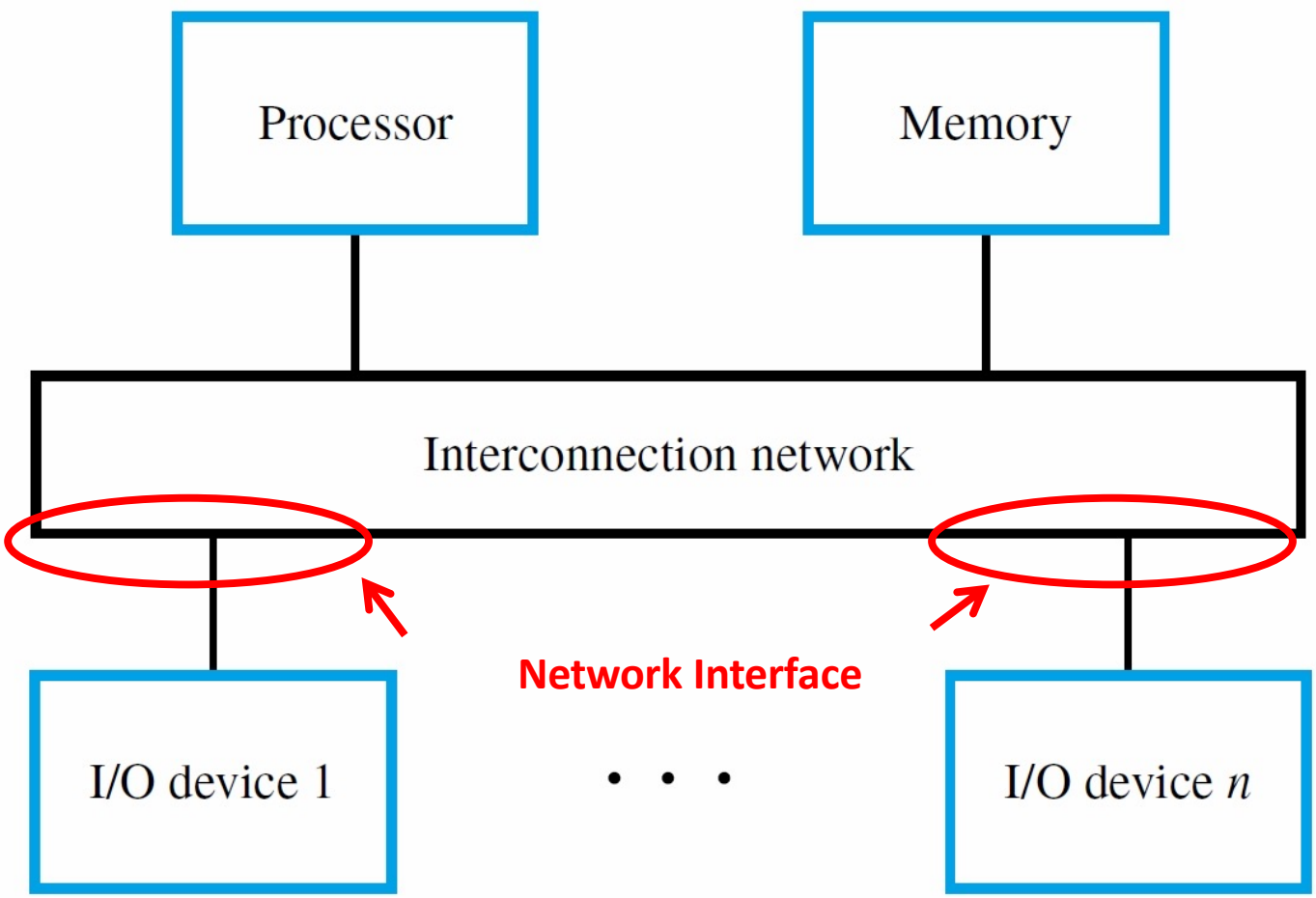
Selecting I/O Method 2: I/O-Mapped



I/O-Mapped I/O

- Each I/O device and its registers are assigned a distinct "I/O address space" or "Ports"
  - Use special I/O instructions (i.e., more instructions in ISA!)
  - Output: Output R6, OutPort1 ; OutPort1 ← R6
  - Input: Input InPort1, R5 ; InPort1 ← R5
  - Need additional circuit to select (i.e., more hardware!)
  - BUT Full memory space is available (vs Memory-mapped)

Fig.3.2 Interconnection Network



3.1.1 I/O Device-Network Interface

- Interconnection Network = System Bus
  - Data — **Number of signals or lines = word size (16, 32, 64 etc.)**
  - Address — **Number of signals or lines often = word size**
  - Control — **Number of signals or lines depends on the CPU design**
- Network Interface:
  - An electronic circuit
  - Between a device and the network
  - Provides control, data transfer, and status information to/from the device

Fig. 7.2 I/O Interface for Input

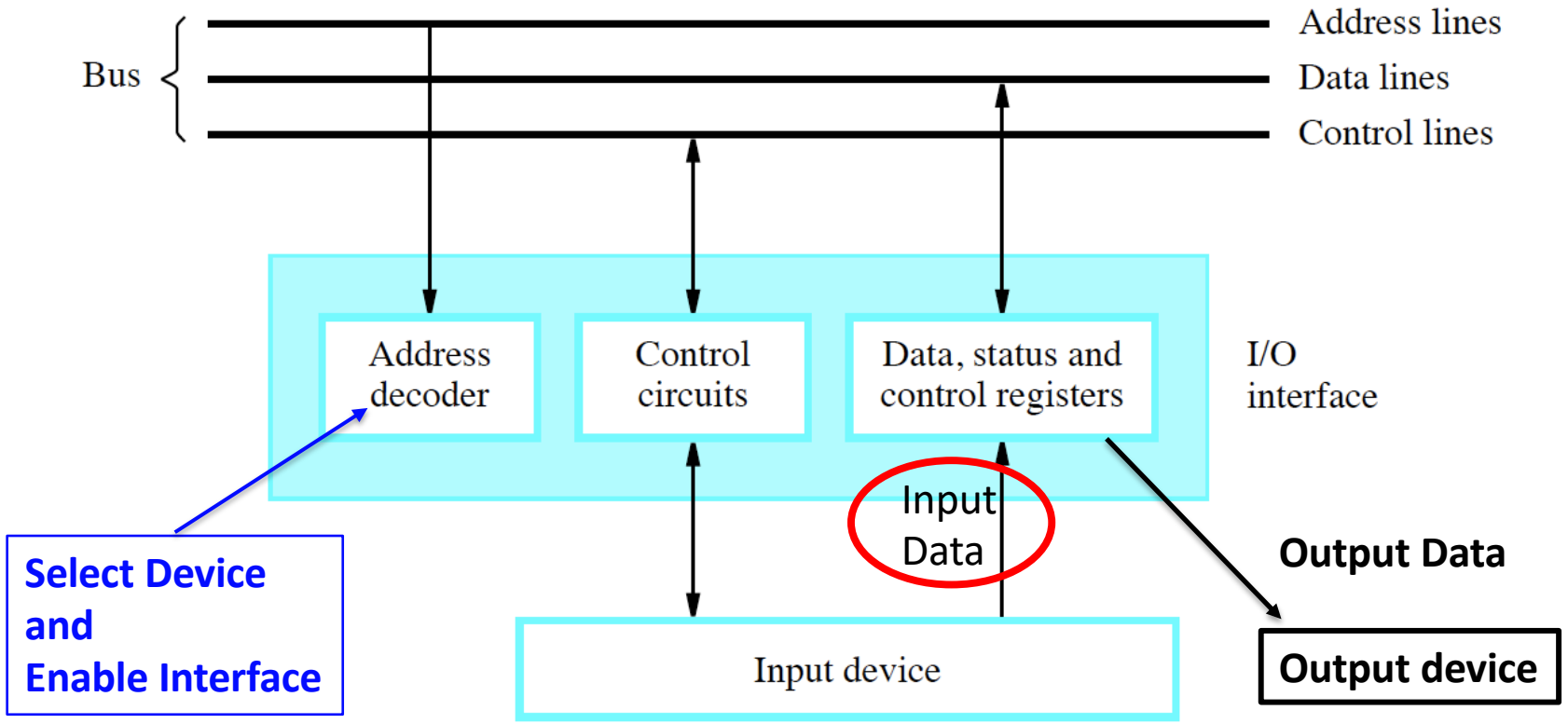


Fig. 3.2 Network Interface

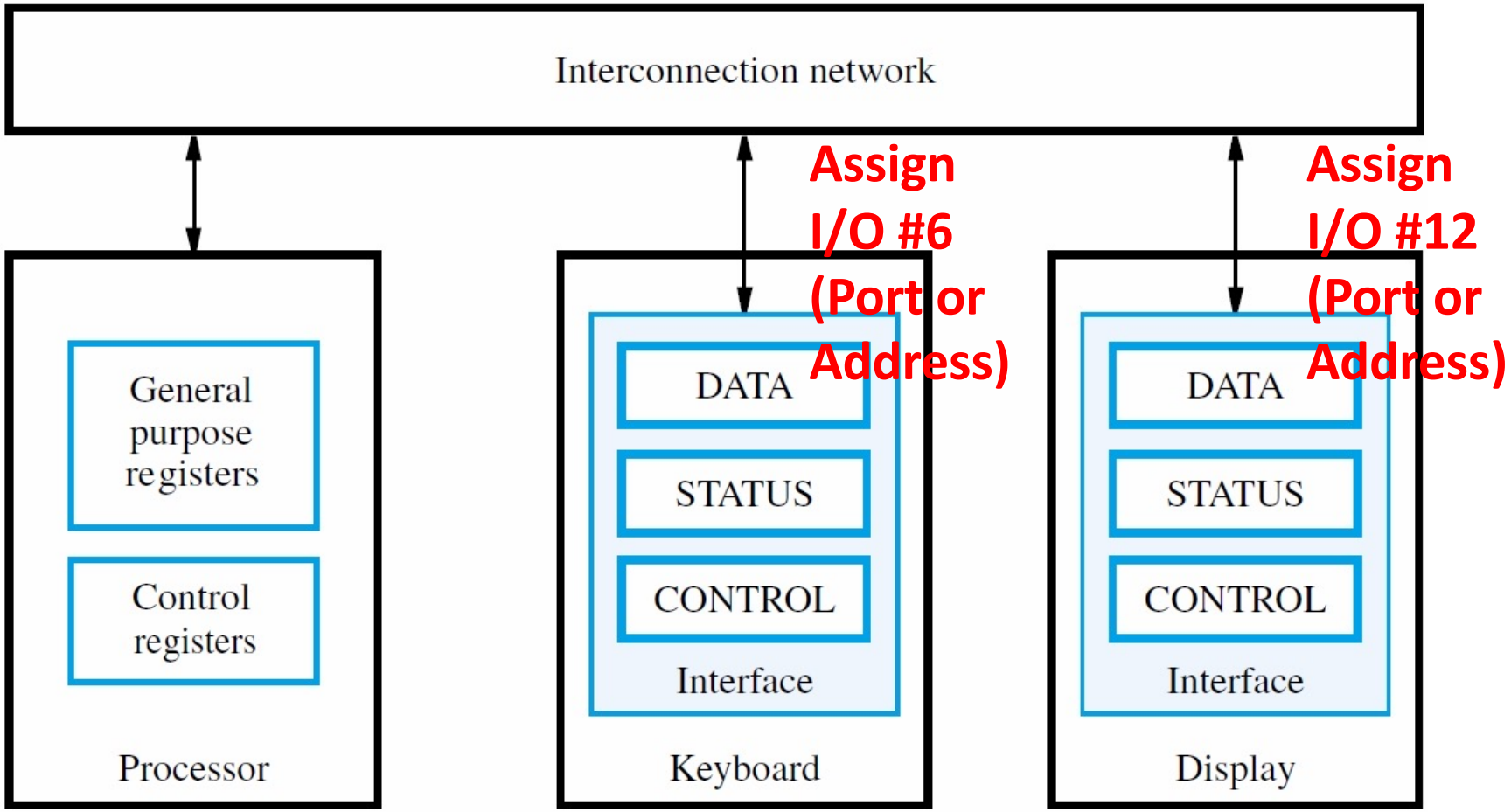
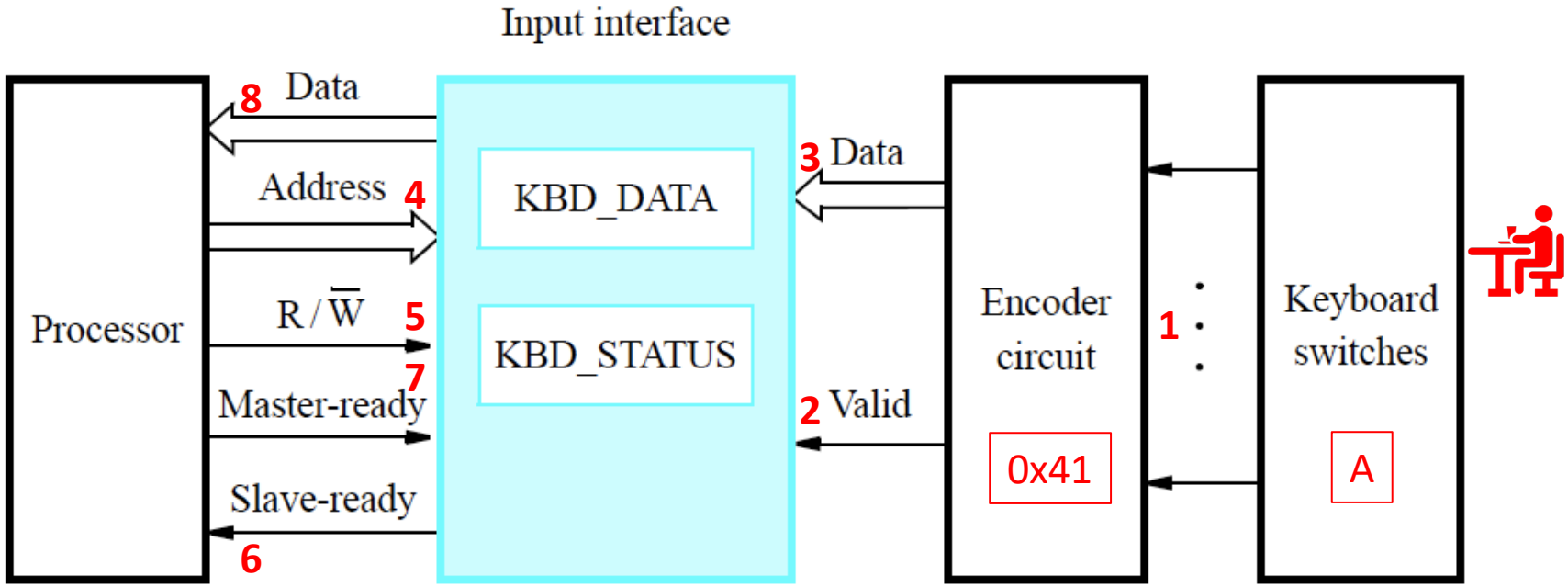


Fig. 7.10 Keyboard and Processor

Signal Sequence: 1,2…7 in order (a handshaking protocol example)



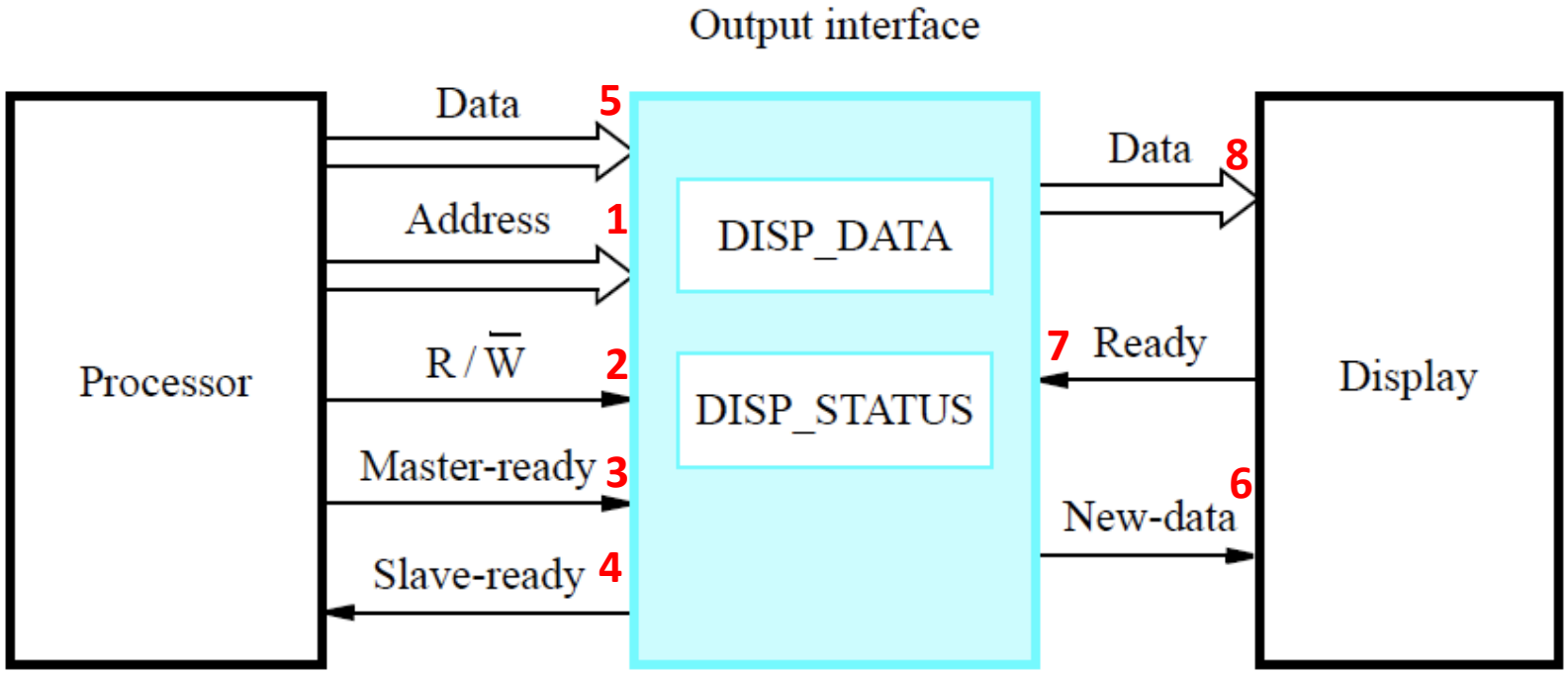
4. Address to select device for Input
5. R/W to select direction
6. I am selected and I am ready
7. I am the Master and I can read now
8. Supply Data

2. Data is valid
3. Supply Data

1. Key position

Fig. 7.13 Display and Processor

Signal Sequence: 1,2…7 in order (a handshaking protocol example)



1. Address to select device for Output
2. R/W to select direction
3. I am the Master and I am ready now
4. I am the selected Slave and I am ready
5. Supply Data
6. I have new data to display
7. I can accept new data
8. Supply Data