Variable Bandwidth DPLL Bit Synchronizer with Rapid Acquisition Implemented as a Finite State Machine

Helmuth Brügel, *Member, IEEE,* and Peter F. Driessen, *Senior Member, IEEE*

Abstract— **A digital PLL bit synchronizer with variable loop bandwidth for rapid acquisition and good tracking performance is proposed, and its performance analyzed using Markov chain techniques. Results are presented for the distributions of acquisition time and time to first bit slip in terms of state transition probabilities. For burst mode data, results for the timing error and bit error rate as a function of the preamble bit number are obtained. All results are evaluated by repeated matrix products and verified by simulation. Comparison of the variable bandwidth DPLL to a fixed bandwidth DPLL shows significantly faster acquisition for a given tracking performance.**

I. Introduction

DIGITAL phase-locked loops (DPLL's) are commonly used for bit synchronization [1] of a digital data stream. In a multiple access system where data is transmitted in bursts or packets, rapid acquisition of bit synchronization is important. This is because rapid acquisition allows the length of the bit sync preamble at the beginning of a data burst to be minimized, thus reducing overhead on the data link and increasing the net data throughput. Once acquisition has been achieved, reliable tracking is needed to minimize the probability of a bit or cycle slip. The performance characteristics of bit synchronizers are discussed in [2].

Traditional DPLL design involves the selection of the order and bandwidth of the digital loop filter to trade off acquisition and tracking performance. For a first order DPLL, the loop filter is a simple gain which determines the DPLL bandwidth [1]. A high loop gain (wide bandwidth) is needed for rapid acquisition, whereas a low gain (narrow bandwidth) is preferred for reliable tracking. Thus any fixed choice of loop gain represents a tradeoff.

To achieve the benefits of both rapid acquisition and reliable tracking simultaneously, this paper considers a DPLL with variable loop gain, called a variable bandwidth DPLL (VBDPLL) in the sequel. The variable gains are arranged so that the loop gain is large at the beginning of a signal for rapid acquisition, and decreases to a small value for reliable tracking. For burst mode data where the signal may be absent or present, the loop gain increases again after the end of a data burst. Thus rapid acquisition may be achieved at the beginning of the next data burst.

The concept of time-varying loop gains with more than two different loop gains has been reported previously [3]–[5]. The effect of a time-varying loop gain for a first order loop is approximated by the adaptive multi-level quantized phase detector of [6]. The variable loop gain is shown to be equivalent to a Kalman filter gain in [7] under certain assumptions. For this case, the mean square timing error is minimized at each timing interval while the signal is present, thus achieving rapid acquisition and reliable tracking.

Any discrete closed-loop bit synchronizer with uniform or nonuniform sampling [8] and a finite number of discrete loop gains may be viewed as a finite state machine. States are defined by two values: the quantized timing error and quantized loop gain. The state machine formulation yields two advantages: it facilitates implementation, and permits analysis of the performance using Markov chain techniques. The state transition probabilities needed for this analysis depend upon the presence/absence of signal, the signaling waveform, signal-to-noise ratio and the type of phase detector employed.

The paper centers around two ideas: the VBDPLL concept in the context of burst mode data, and the analysis of a DPLL as a finite state machine. The main contribution of the paper is a complete solution for the performance characteristics of a finite state machine VBDPLL bit synchronizer in terms of the state transition probabilities. Numerical results are obtained by evaluating repeated matrix products. The timing error probability mass function (pmf) (discrete probability density) as a function of the preamble bit number k is derived, from which the rms timing error and bit error rate as a function of k are readily obtained. The distribution of acquisition time and distribution of the time to first bit slip are derived, from which mean values of acquisition time and first bit slip time are obtained. These results can be used to determine the length of the preamble needed for acceptable performance [9]. The authors of [10] used Chapman-Kolmogorov (C-K) equations to derive a numerical solution for acquisition time probabilities in the case of a sine wave signal and bandlimited noise for a fixed loop gain. In [11] C-K equations are used to derive approximations for steady state pmf's of the timing error. A solution for the distribution of acquisition time assuming low-pass filtered noise and time varying gains has not been previously found [2].

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The authors are with the Department of Electrical and Computer Engineering, University of Victoria, Victoria, B.C. V8W 3P6, Canada.

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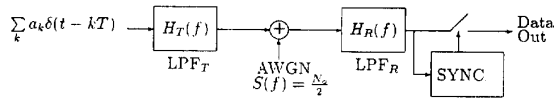

Fig. 1. Bandlimited baseband binary data transmission system.

To illustrate the VBDPLL performance, numerical results are given for the first-order VBDPLL with a zero-crossing type phase detector and sine wave signaling waveform in the preamble. However, results may be calculated for any other type of signaling pulse and phase detector by recomputing the state transition probabilities. The results may also be generalized to second and higher order DPLL's by defining additional states [12]. The results presented here assume that successive noise terms in (7) are independent, but this assumption can be relaxed by adding additional states [12]. The 1st order VBDPLL finite state machine is implemented with a 256 KB read-only memory and a latch as part of a commercial modem product [12].

The paper is organized as follows. In Section II, the signaling waveform and phase detector used to illustrate the results are given and the operation of the variable loop gain bit synchronizer is described. The finite state Markov model is developed in Section III and the timing error pmf's versus preamble bit number k are derived in terms of the state transition probabilities. Section IV contains the derivation of the distribution of acquisition time and first bit slip time, and the corresponding means. Numerical and simulation results are given in Section V, followed by conclusions in Section VI.

II. System Description

A. Signaling Waveform and Phase Detector

In this section, the signaling waveform and phase detector used to obtain numerical results for the VBDPLL performance are given. Consider the binary communications system whose baseband equivalent model is shown in Fig. 1. The transmit and receive filters $H_T(f)$ and $H_R(f)$ form a matched filter pair whose output is the baseband binary PAM signal

$$x(t) = \sum_k a_k g(t - kT - \epsilon) + \eta(t) \tag{1}$$

when signal is present and $x(t) = \eta(t)$ when signal is absent. In equation (1) $a_k \in \{-1, +1\}$ are independent zero mean binary numbers, T is the symbol duration and $g(t)$ is the baseband pulse which is assumed to satisfy the first Nyquist criterion. The delay ϵ is assumed to be constant during a data burst but it may change from one data burst to another. The term $\eta(t)$ is formed by filtering additive white Gaussian noise, with single sided power spectral density N_0, through $H_R(f)$.

Each data burst is preceded by a preamble of a 10101... pattern to maximize the number of zero crossings for rapid synchronization, with $a_k = -a_{k+1}$ for all k up to the preamble length. For a random data pattern the number of zero crossings would be half (on average) compared to a 10101... pattern, hence all acquisition times obtained would be doubled. In the sequel, we assume that

$$g(t) = \begin{cases} C \cdot cos\left(\frac{\pi t}{T}\right) & \text{for } -T/2 < t < T/2 \\ 0 & \text{otherwise} \end{cases} \tag{2}$$

so that the received preamble is a simple sine wave. We also assume that $H_R(f)$ is approximated by a third-order Butterworth filter for simulation purposes.

A zero crossing will occur at

$$t = kT + t_0 + \epsilon + n_k \tag{3}$$

where t_0 is the nominal zero crossing location relative to the optimum sampling instant ($t_0 = T/2$ for a sine wave) and n_k is the horizontal zero crossing displacement due to additive noise at the k-th symbol.

The receiver determines the polarity of the received bit $\hat{a}_k$by sampling the received and hard limited waveform at

$$t = kT + \hat{\epsilon}_k \tag{4}$$

where $\hat{\epsilon}_k$ is the synchronizer's estimate of ϵ for the data symbol $\hat{a}_k$. The synchronizer's timing error is

$$e_k = \{\epsilon - \hat{\epsilon}_k\}_{mod\ T} \tag{5}$$

where $\{\cdot\}_{mod\ T}$ indicates the timing error is modulo T reduced in the range $(-T/2, T/2]$ since timing errors differing by integer multiples of T are indistinguishable in steady state.

We assume a zero crossing based timing error detector or phase detector (PD) [13], however any PD with a discrete output can be used. For every detected zero crossing the PD generates an output y_k, proportional to the difference between the location of the detected zero crossing $kT+t_0+\epsilon+n_k$ from (3) and the predicted location $kT + t_0 + \hat{\epsilon}_k$, and quantized to M discrete values

$$y_k = q_1[\{\epsilon - \hat{\epsilon}_k + n_k\}_{mod\ T} K_{PD}] \tag{6}$$

$$= q_1[\{e_k + n_k\}_{mod\ T} K_{PD}] \tag{7}$$

where $q_1[\cdot]$ is the quantizer characteristic which quantizes its argument to the next larger integer. The PD gain $K_{PD} = M/T$ is chosen to yield M integer PD outputs y_k in the range $\{-M/2 + 1, \ldots, M/2\}$ (M is even).

B. Variable Bandwidth DPLL Bit Synchronizer

In this section, the operation of the VBDPLL bit synchronizer is described. A block diagram of the proposed synchronizer is shown in Fig. 2. The synchronizer is a first order loop with a variable loop gain K_k.

The selection of the specific values of K_k is motivated by the formulation of a DPLL bit synchronizer as a Kalman filter [7] which estimates the constant process ϵ. For a first order DPLL the five Kalman filter equations can be combined into two update equations: the timing update

$$\hat{\epsilon}_{k+1} = \hat{\epsilon}_k + K_k(\epsilon - \hat{\epsilon}_k + n_k), \tag{8}$$

and the gain update

$$K_{k+1} = \frac{A + K_k}{1 + A + K_k}. \tag{9}$$

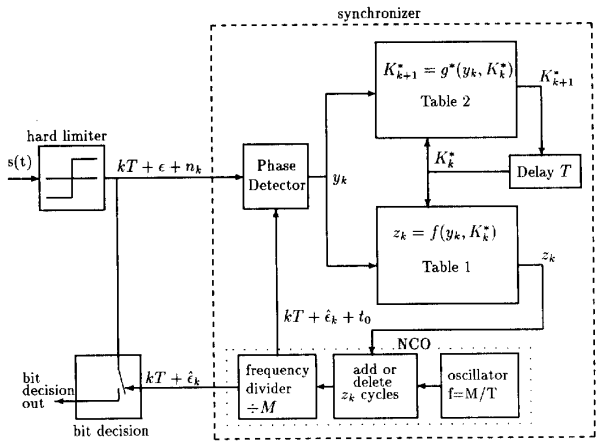

Fig. 2. Variable bandwidth digital PLL sychronizer.

TABLE I
z_k AS A FUNCTION OF ACQUISITION STATE K^*_k AND PD OUTPUT y_k. z_k FOR $y_k > 0$ IS GIVEN BY SYMMETRY

	$K_k=0.829$	0.453	0.312	0.238	0.192	0.161	0.139	0.122
y^*_k	$K^*_k=0$	1	2	3	4	5	6	7
-15	-13	-7	-5	-4	-3	-3	-2	-2
-14	-12	-7	-5	-4	-3	-2	-2	-2
-13	-12	-6	-4	-3	-3	-2	-2	-2
-12	-11	-6	-4	-3	-2	-2	-2	-2
-11	-10	-5	-4	-3	-2	-2	-2	-1
-10	-9	-5	-3	-3	-2	-2	-2	-1
-9	-8	-5	-3	-2	-2	-2	-1	-1
-8	-7	-4	-3	-2	-2	-1	-1	-1
-7	-7	-4	-2	-2	-2	-1	-1	-1
-6	-6	-3	-2	-2	-1	-1	-1	-1
-5	-5	-3	-2	-1	-1	-1	-1	-1
-4	-4	-2	-2	-1	-1	-1	-1	-1
-3	-3	-2	-1	-1	-1	-1	-1	-1
-2	-2	-1	-1	-1	-1	-1	-1	-1
-1	-2	-1	-1	-1	-1	-1	-1	-1
-0	-1	-1	-1	-1	-1	-1	-1	-1

TABLE II
K^*_{k+1} AS A FUNCTION OF ACQUISITION STATE K^*_k AND PD OUTPUT y_k. K^*_{k+1} FOR $y_k > 0$ ARE GIVEN BY SYMMETRY

y^*_k	$K^*_k=0$	1	2	3	4	5	6	7
-15	0	0	0	0	1	2	3	4
-14	0	0	0	0	1	2	3	4
-13	0	0	0	0	1	2	3	4
-12	0	0	0	0	1	2	3	4
-11	0	0	0	1	2	3	4	5
-10	0	0	0	1	2	3	4	5
-9	0	0	0	1	2	3	4	5
-8	0	0	1	2	3	4	5	6
-7	0	0	1	2	3	4	5	6
-6	0	0	1	2	3	4	5	6
-5	0	1	2	3	4	5	6	7
-4	0	1	2	3	4	5	6	7
-3	0	1	2	3	4	5	6	7
-2	1	2	3	4	5	6	7	7
-1	1	2	3	4	5	6	7	7
-0	1	2	3	4	5	6	7	7

In (9), $A=\sigma_u^2/\sigma_n^2$ is the ratio of the process noise variance to the measurement noise variance. A signal detector algorithm is required to set $\sigma_u^2=0$ $(A=0)$ when signal is present and $\sigma_u^2 \gg \sigma_n^2$ $(K_{k+1}\approx 1)$ when signal is absent. These gain adjustment and signal detector algorithms can be combined and represented in table form as shown in the sequel.

A quantized version of (8) is used by the synchronizer to update the timing estimate, $\hat{\epsilon}_k$, according to

$$\hat{\epsilon}_{k+1}=\hat{\epsilon}_k+q_2[K_k q_1[\{\epsilon-\hat{\epsilon}_k+n_k\}_{mod T}K_{PD}]]\Delta T \quad (10)$$

$$=\hat{\epsilon}_k+q_2[K_k y_k]\Delta T \quad (11)$$

where $q_2[K_k y_k]\in\{-\frac{M}{2}+1,\ldots,\frac{M}{2}\}$. In (10) two quantizations are done. First the PD output is quantized by $q_1[\cdot]$, second the timing updates are done in quantized steps by $q_2[\cdot]$. Both quantizers use a quantization step size of $\Delta T=T/M$ so that $q_1[\cdot]=q_2[\cdot]$. A more general timing update, including nonlinear PD's and loop filters, can be written by replacing $q_2[K_k y_k]$ with a general function $z_k=f(y_k,K_k)$ so that

$$\hat{\epsilon}_{k+1}=\hat{\epsilon}_k+f(y_k,K_k)\Delta T=\hat{\epsilon}_k+z_k\Delta T \quad (12)$$

To determine $f(y_k,K_k)$, we assume a set of N discrete loop gains K_k are used. Each of the N possible gains K_k is assigned an integer number $K^*_k\in\{0,\ldots,N-1\}$ where $K^*_k=N-1$ denotes the smallest possible gain (narrowest bandwidth). In the sequel we refer to the N discrete gains as acquisition states since, in general, K_{PD} within one of these acquisition states K^*_k may also depend on y_k, i.e., the PD may be nonlinear. A typical table showing $z_k=f(y_k,K_k)$ for $M=32$, $N=8$ is shown in Table I. This table is based on a deterministic gain sequence K_k calculated using equation (9) with signal present $(A=0)$. Tables for other values of M and N are discussed in [12].

After the timing estimate update (12) is carried out, the gain K_k is updated. This can not be done using equation (9) directly since it is not known apriori if signal is present. We use y_k to estimate the presence or absence of signal, so that the new gain is a function of the present gain and the present PD output

$$K_{k+1}=g(K_k,y_k) \quad (13)$$

This gain update (13) can be defined as an acquisition state update

$$K^*_{k+1}=g^*(K^*_k,y_k) \quad (14)$$

and represented in table form. The function g^* is such that the loop gain is increased for large $|y_k|$ (signal absent), so that rapid acquisition can be achieved when the signal arrives. When the signal arrives, the loop gain is reduced step-by-step to a minimum value for good tracking. At the end of a signal burst the gain increases so that the synchronizer can acquire rapidly on the next signal burst. A typical example for such a table is shown in Table II. The table determines how fast the synchronizer lowers its bandwidth when signal is present and how fast the bandwidth is increased again when a data burst ends. A systematic discussion of different tables is presented in [12]. Table II yields a good compromise between fast acquisition and low steady state timing error.

Equations (12) and (14) can be written as a set of Markov chain equations

$$\Theta_{k+1} = \begin{bmatrix} K^*_{k+1} \\ \hat{\epsilon}_{k+1} \end{bmatrix} = H(\Theta_k, n_k) = \begin{bmatrix} g^*(K^*_k, \hat{\epsilon}_k, n_k) \\ h(K^*_k, \hat{\epsilon}_k, n_k) \end{bmatrix} \quad (15)$$

The corresponding Markov model will be developed in the next section.

The bit synchronizer operates by evaluation of the quantized timing estimate update equation (12) and the quantized acquisition state update equation (14) at each k. Since (12) and (14) can be represented in table form, the bit synchronizer can be implemented using lookup tables as illustrated in figure 2. The discrete PD output y_k and the present acquisition state K^*_k act as indices to the acquisition state update table to determine the next acquisition state K^*_{k+1}. In the implementation proposed in [12] the y_k and K^*_k are represented in binary notation, and these bits are used to control address lines to a ROM containing the stored values of z_k and K^*_{k+1} in Tables I and Table II. Thus if the minimum access time of the ROM is T/M, then data rates up to $1/T$ are possible. For example, a 20 ns ROM can be used at the 1.544 Mbps T1 carrier rate.

The output of the timing update table z_k is used to control the numerically controlled oscillator (NCO) operating at a frequency $f = M/T$. The parameter z_k determines how many cycles of this clock are deleted or added before the clock frequency is divided by M to yield the reference clock. The reference clock is used as reference input to the PD and it determines the sampling instant at which the hard limited received waveform is sampled to make a hard decision on the bit polarity.

III. Finite State Markov Model

In this section, the finite state Markov model for the VBDPLL is developed, and the timing error pmf's versus k are derived. The model in [14] is modified to include the variable loop gain. First, a two dimensional Markov model is defined, with Markov states determined by the synchronizer timing error state and acquisition state. The state transition probabilities are calculated in the Appendix as a function of the signal-to-noise ratio, signaling waveform and phase detector type, and are arranged into a single step state transition matrix $\boldsymbol{P}$ for signal present or $\boldsymbol{P}_n$ for signal absent. To obtain the Markov state pmf (and thus the timing error and acquisition pmf's) versus k, the initial Markov state pmf is multiplied k times by the state transition matrix $\mathbf{P}$.

To begin the development of the Markov model, the discrete timing update equation (12) can be combined with (5) and written as a discrete timing error update equation

$$e_{k+1} = \{e_k - z_k \Delta T\}_{mod\ T} \quad (16)$$

Due to the modulo T reduction of the quantized timing error there are only M equally spaced discrete timing errors possible. We denote these discrete timing errors by $\Phi_0, \Phi_1, \ldots, \Phi_{M-1}$ where $-T/2 < \Phi_0 < \Phi_1 < \ldots < \Phi_{M-1} < T/2$. Thus

$$\Phi_i = (i + 0.5)\Delta T - T/2 \quad i = 0, 1, \ldots, M-1 \quad (17)$$

where we assumed the optimum timing instant ($e_k = 0$) is centered between the two minimum timing error states $\Phi_{M/2-1}$ and $\Phi_{M/2}$. The effect of a noncentered optimum sampling instant can be analysed with a slight modification of the theory [15], but this effect is not significant for large M, e.g., if ΔT is small compared to the actual timing error variances [16].

We assign each of the M possible discrete timing errors a number $e^*_k \in \{0, 1, \ldots, M-1\}$. The timing error update equation (16) can be written

$$e^*_{k+1} = e^*_k - z_k. \quad (18)$$

The overall system state (Markov state) $s_k = s(e^*_k, K^*_k)$ at time k is determined by the combination of the acquisition state K^*_k and the actual timing error state e^*_k. A system state number $s_k \in \{0, \ldots, MN-1\}$ is assigned by the rule

$$s_k = MK^*_k + e^*_k \quad (19)$$

Note that for purposes of analysis, the state of the synchronizer is defined by the timing error e^*_k and the acquisition state K^*_k. The state of a finite state machine implementation is defined by the present PD output y_k and the present acquisition state K^*_k since the synchronizer doesn't know the actual timing error e_k.

We assume that the noise parts of successive PD outputs y_k are statistically independent. This assumption is not strictly valid [12], but is reasonable for the signaling waveform (2) and phase detector (7), since the analytical and simulation results agree closely. For greater accuracy, a higher dimensional Markov model can be used to include any correlation between successive PD outputs [12]. With this independence assumption, the system state sequence $\{s_0, s_1, \ldots, s_k, \ldots\}$ generated by equations (14) and (16) may be assumed to form a Markov chain with MN states. The state s_0 is the state of the synchronizer at the beginning of a data burst.

For $l, m \in \{0, 1, \ldots, (MN-1)\}$, let $p_{l|m}$ denote the single step state transition probability, i.e. the probability that the system presently in state l will occupy state m after its next transition. Thus

$$p_{l|m} = Pr\{s_{k+1} = m | s_k = l\} \quad l, m \in \{0, 1, \ldots, (MN)-1\} \quad (20)$$

The $p_{l|m}$ are a function of the signal to noise ratio at the synchronizer input, the signal shape and the particular PD, and are calculated in the Appendix. These transition probabilities are conveniently arranged in a single step state transition matrix

$$\mathbf{P} = \begin{bmatrix} p_{0|0} & \cdots & p_{0|(MN-1)} \\ \vdots & \ddots & \vdots \\ p_{(MN-1)|0} & \cdots & p_{(MN-1)|(MN-1)} \end{bmatrix} \quad (21)$$

If the signal is absent, we define $\mathbf{P_n}$ in an analogous manner. In general, the state transition matrices may be a function of time k, but this is not explicitly indicated to simplify notation.

We call the probability that a certain state is occupied after k state transitions a Markov state probability [17]. The probability that state l is occupied after k iterations

$$Pr\{s_k = l\} = \pi_{l,k}. \quad (22)$$

If we define the Markov state probability mass vector

$$\boldsymbol{\pi}_k = [\pi_{0,k}, \pi_{1,k}, \ldots, \pi_{(MN-1),k}], \quad (23)$$

then the state pmf after the $(k+1)$st state transition is related to the state pmf after the kth iteration by the recursion [17]

$$\boldsymbol{\pi}_{k+1} = \boldsymbol{\pi}_k \mathbf{P}. \tag{24}$$

This recursion can be used to calculate the state pmf $\boldsymbol{\pi}_k$ at time k given the state transition probability matrix $\mathbf{P}$ and the initial state pmf $\boldsymbol{\pi}_0$. For the described Markov chain with MN states, it is possible to reach any state in exactly k steps for $k > MN$. For a Markov chain with this property, $\boldsymbol{\pi}_k$ in (24) will tend to a unique distribution as k tends to infinity [18]. We assume that the initial state pmf $\boldsymbol{\pi}_0$ at the beginning of a data burst synchronizer is the steady state ($k = \infty$) pmf with signal absent.

The timing error pmf is defined by $\mathbf{v}_k = [v_{0,k}, v_{1,k}, \ldots, v_{M-1,k}]$ with $Pr\{e_k = \Phi_i\} = v_{i,k} = \sum_{j=0}^{N-1} \pi_{(jM+i),k}$. The acquisition state pmf is defined by $\mathbf{w}_k = [w_{0,k}, w_{1,k}, \ldots, w_{N-1,k}]$ with $Pr\{K_k^* = i\} = w_{i,k} = \sum_{j=0}^{M-1} \pi_{(iM+j),k}$. The pmf's $\mathbf{v}_k$ and $\mathbf{w}_k$ are marginal pmf's of the joint pmf $\boldsymbol{\pi}_k$.

IV. Synchronizer Performance Characteristics

This section contains the derivation of the synchronizer performance characteristics using the Markov state pmf, $\boldsymbol{\pi}_k$, obtained in Section III. The timing error variance and bit error rate as a function of k are obtained in Section IV–A. The distribution of acquisition time is derived in Section IV-B, followed by the distribution of first bit slip time in Section IV–C.

A. RMS Phase Jitter and Bit Error Performance

The timing error variance $\sigma_{e_k}^2$ can be calculated directly from the timing error pmf $\mathbf{v}_k$.

The bit error probability $P_e(k)$ as a function of the preamble bit number k can be used to determine the required preamble length for a given application. The data detector takes samples of the hard limited signal at $t = kT + \hat{\epsilon}_k$ as an estimate $\hat{a}_k$ for the bit polarity a_k. The bit error probability P_e conditioned on the timing error e_k is given by

$$P_e(e_k = \Phi_i) = Q\left(\frac{\sum_k a_k g(\Phi_i - kT)}{\sigma_n}\right) \tag{25}$$

where

$$Q(x) = \frac{1}{2\pi}\int_x^\infty e^{-y^2/2} dy. \tag{26}$$

For the pulse shape of (2) and a 10101... preamble we get

$$P_e(e_k = \Phi_i) = Q\left(\frac{C \cdot cos\frac{\pi\Phi_i}{T}}{\sigma_n}\right). \tag{27}$$

The timing error, $P_e(e_k = \Phi_i)$, can be averaged over the discrete timing error pmf, $\mathbf{v}_k$, of the synchronizer to obtain $P_e(k)$.

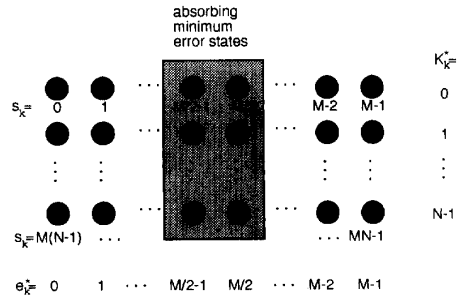

Fig. 3. Markov state diagram to calculate the acquisition time pmf. The timing error e_k is modulo T reduced. Minimum error states are absorbing states.

B. Acquisition Time Distribution

We define the acquisition time T_{acq} as the time (normalized by the bit duration T) to reach one of the minimum timing error states ($\Phi_{\frac{M}{2}-1}, \Phi_{\frac{M}{2}}$) for the first time. In this section, the discrete distribution $Pr(T_{acq} \leq k)$ of the acquisition time is found.

We denote $U_{k|s_0=l}$ as the probability that a minimum timing error state is reached after k state transitions starting from the initial Markov state $s_0 = l$. Let the set $\{j\}$ contain the state numbers of all states s_k which represent one of the two minimum timing error states $\Phi_{M/2-1}$ and $\Phi_{M/2}$ (see Fig. 3).

The probability $U_{0|s_0=l}$that a minimum timing error state is reached in zero transitions is the probability of being in that state initially, thus

$$U_{0|s_0=l} = \begin{cases} 1 & \text{for} \quad l \in \{j\} \\ 0 & \text{for} \quad l \notin \{j\} \end{cases} \tag{28}$$

Furthermore, if the initial timing error state e_0 is a minimum error state, then the probability is zero that the acquisition time is larger than zero, thus

$$U_{k|s_0=l} = 0 \text{if}, l \in \{j\} \text{and } k > 0. \tag{29}$$

We assume now that the initial state s_0 is not a minimum error state and that the first transition is from state $s_0 = l$ to $s_1 = m$. The conditional probability $U_{1|s_0=l,s_1=m}$ that a minimum error state is reached in one transition given the first transition is from $s_0 = l$ to $s_1 = m$ is equal to the probability $U_{0|s_0=m}$ that zero transitions are required from state $s_0 = m$ to a minimum error state. The probabilities $U_{1|s_0=l}$ can be found by averaging over the state transition probabilities

$$\begin{aligned} U_{1|s_0=l} &= \sum_{m=0}^{MN-1} p_{l|m} U_{1|s_0=l,s_1=m} \\ &= \sum_{m=0}^{MN-1} p_{l|m} U_{0|s_0=m} \qquad l \notin \{j\} \quad k \geq 0 \end{aligned} \tag{30}$$

This argument can be repeated for the probabilities of reaching a minimum error state in $2, 3, \ldots$ transitions. Thus,

$$\begin{aligned} U_{k+1|s_0=l} &= 0 \qquad\qquad\qquad\qquad l \in \{j\} \quad k \geq 0 \\ U_{k+1|s_0=l} &= \sum_{m=0}^{MN-1} p_{l|m} U_{k|s_0=m} \quad l \notin \{j\} \quad k \geq 0 \end{aligned} \tag{31}$$

This iteration is started with the initial conditions (28).

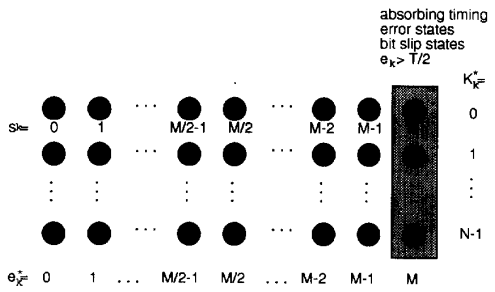

Fig. 4. Markov state diagram to calculate bit slip pmf. The timing error e_k is not modulo T reduced. All timing errors larger that $T/2$ are represented by absorbing timing error states.

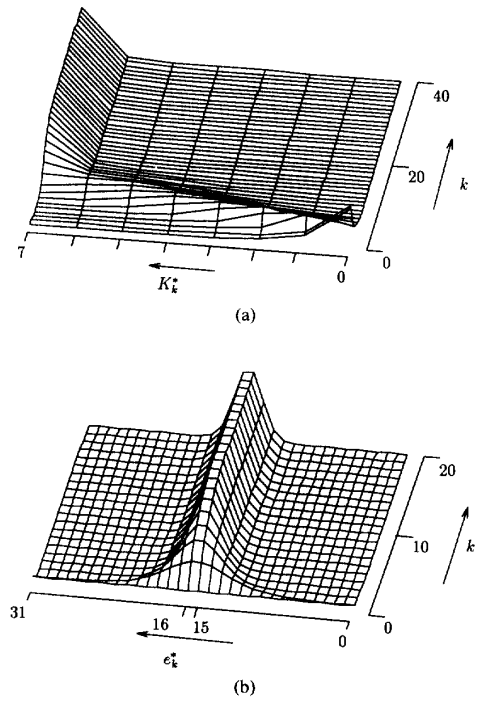

Fig. 5. Discrete acquisition state density and discrete timing error density for $E_b/N_0 = 10$ dB as a function of the preamble bit number k. $M = 32$, $N = 8$.

The probabilities $/!U_{k|s_0=l}/!$ are conditioned on the initial Markov state $s_0 = l$, i.e., they are joint probabilities conditioned on initial timing error $e_0 = \Phi_i$ and initial acquisition state. The marginal probabilities $U_{k|e_0=\Phi_i} = \sum_{l=0}^{N-1} U_{k|s_0=l}\pi_{lM+i,0}$ are the pmf of the acquisition time T_{acq} and it is now straightforward to find the discrete distribution and the mean of T_{acq} conditioned on $e_0 = \Phi_i$. The unconditional pmf is $U_k = \sum_{i=0}^{M-1} U_{k|e_0=\Phi_i} v_{i,k}$.

The acquisition time may be defined in slightly different ways. Some authors [2] define the acquisition time as the time before the timing error stays smaller than a defined threshold for longer than a given lock detection time T_{lk}. The mean and the distribution of the acquisition time defined in this way can easily be calculated using the described methods if the Markov model is modified by adding T_{lk}/T additional timing error states for each minimum error state [12]. The acquisition time can also be defined as the time to reach one of the minimum timing error states and simultaneously also the minimum gain state $K_k^* = N - 1$.

The method proposed by Feller [18] to determine the mean duration of a game in the classical "gambler's ruin" problem [16], [15] was used [12] to confirm the mean values obtained above.

C. First Bit Slip Time Distribution

A zero crossing based bit synchronizer in steady state cannot distinguish between timing errors differing by multiple integers of a bit duration T. Thus for all the preceding analysis it was assumed that the timing error e_k is modulo T reduced. To analyze the bit slip performance of the synchronizer, we assume that transitions to timing error states outside the interval $(-T/2, T/2]$ are treated as transitions to an error state Φ_M (bit slip state, see figure 4). Also, since we are only interested in the time to the first bit slip, we make the bit slip state an absorbing state. The Markov state diagram with the additional bit slip states is shown in Fig. 4. There are now $(M+1)N$ Markov states. The state transition probabilities $p_{l|m}$ have to be recalculated using this state transition diagram. The pmf of the bit slip time can then be calculated using the same procedure as for the acquisition time pmf in Section IV–B.

V. Numerical Results

In this section we present numerical results obtained with the analysis method presented in the previous sections for the phase detector and signaling waveform described in Section II. The results are verified by computer simulation. A sampled cosine wave with M samples per half period T has been combined with samples of filtered AWGN to generate the input signal to the VBDPLL. The noise filter was a third-order Butterworth filter with cutoff frequency $1/2T$. We assume timing update Table I and acquisition state update Table II.

To calculate the synchronizer performance, we first must calculate $\boldsymbol{P}, \boldsymbol{P}_n, \boldsymbol{\pi}_k$ as outlined in Section III and the Appendix.

The acquisition state density $\boldsymbol{w}_k$ and the timing error density $\boldsymbol{v}_k$ are obtained from $\boldsymbol{\pi}_k$ and are shown in Figs. 5 and 6 as a function of the preamble bit number k. The probability that the synchronizer is in a narrow acquisition state and a small timing error state increases with k, thus illustrating how acquisition is achieved.

The timing error distributions $\mathbf{v}_k$ have been used to calculate the rms timing error as a function of the preamble bit number k. The result is shown in Fig. 7 for different signal-to-noise ratios. For comparison, rms timing error curves are also shown in Fig. 7 for a fixed step size synchronizer, i.e., a synchronizer where $z_k \in \{+1, -1\}$. The improvement of the adaptive synchronizer is obvious. The fixed step size synchronizer reaches steady state only after more than 30 bits, whereas the adaptive synchronizer reaches the same steady state rms timing error after less than 5 bits. We note that the fixed step size

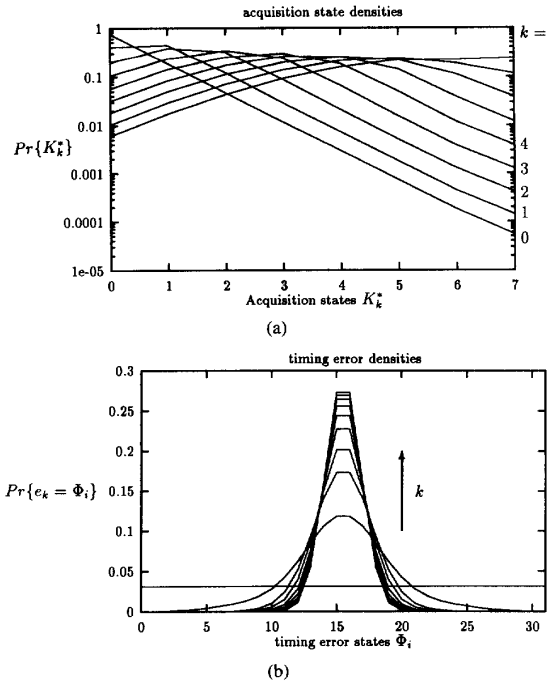

Fig. 6. Discrete acquisition state density and discrete timing error density for $E_b/N_0 = 10$dB as a function of the preamble bit number k. $M = 32$, $N = 8$.

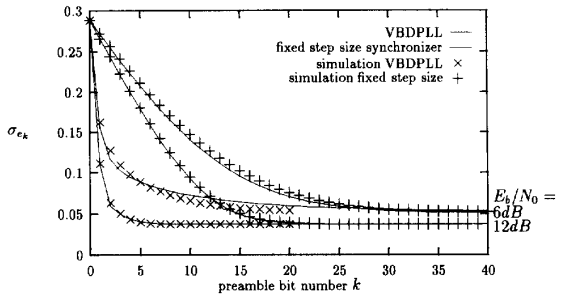

Fig. 7. RMS timing error as a function of the preamble bit number k.

synchronizer is identical to a synchronizer proposed by Payzin [14] except for a different phase detector. The steady-state values shown in Fig. 7 are identical to the values published in [14].

The analytical results are verified by computer simulation and the agreement between simulation and analysis is good except for low signal-to-noise ratios ($E_b/N_0 < 6dB$) where the assumptions made in calculating the state transition probabilities are no longer accurate.

When comparing the required computing time for the numerical method and the simulation method, the advantage of the numerical method becomes obvious. To simulate 10^4 trials of a 40 bit preamble with $M = 32$ and 8 acquisition states we required 2385 s of CPU time on a SUN4/60M with a 20 MHz

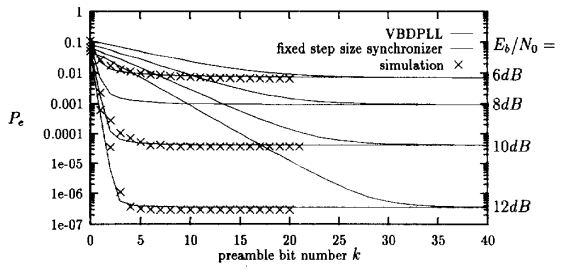

Fig. 8. Bit error rate as a function of the preamble bit number k.

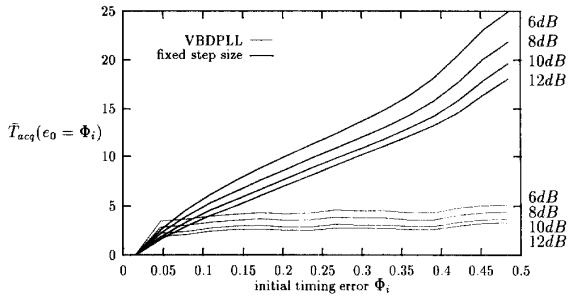

Fig. 9. Mean time to acquire as a function of the initial timing error e_0 for different E_b/N_0.

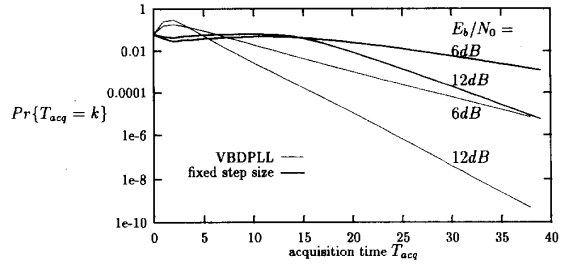

Fig. 10. pmf of the acquisition time for different E_b/N_0 assuming uniform initial timing error.

SPARC CPU. Using the numerical method the same result could be obtained using 4.9 s of CPU time.

The bit error rate of a single sample detector has been calculated using (27) and averaging over the timing error pmf $\boldsymbol{v}_k$. The result is shown in Fig. 8. Again the improvement of the adaptive synchronizer is obvious.

The mean time to acquire $\bar{T}_{acq}(e_0 = \Phi_i)$ as a function of the initial timing error e_0 is shown in Fig. 9. It can be seen that the mean time to acquire is much smaller for the adaptive synchronizer than for the fixed step size synchronizer. For the adaptive (VBDPLL) synchronizer the mean time to acquire is almost independent of the initial timing error e_0 since for large timing errors one timing correction is enough to reach a small timing error due to the large loop gain during acquisition.

The acquisition time pmf's in Fig. 10 are used to calculate the probabilities of not acquiring after k bits as shown in Fig. 11. It was assumed that the initial Markov state distribution, $\boldsymbol{\pi}_0$ is the steady state distribution in noise, i.e., the initial

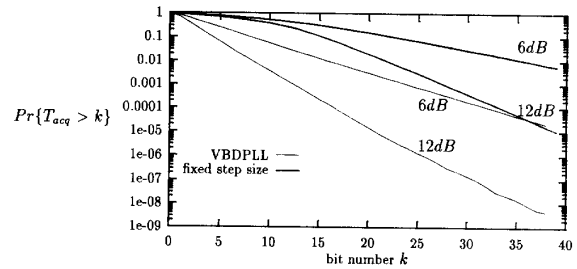

Fig. 11. Probability that T_{acq} is bigger than bit number k assuming uniform initial timing error.

timing error is uniformly distributed. These distributions can be used to determine the required preamble length for a required probability of acquisition before data starts. As can be seen from the figures, the acquisition time and hence the required preamble length is significantly shorter for the adaptive synchronizer. Hang-up effects are insignificant since after 35 bits the probability of not acquiring is $\approx 10^{-8}$ for a signal-to-noise ratio of 12 dB (Fig. 11). When using the pmf's of Fig. 10 to calculate the distributions of Fig. 11 very small probabilities have to be added to large probabilities (close to one).

VI. Conclusions

This paper has presented two main ideas: a variable loop gain DPLL bit synchronizer for burst mode data, and a performance analysis using Markov chain techniques which yields numerical results in terms of state transition probabilities. It is demonstrated how a nonuniform sampling closed loop DPLL bit synchronizer with variable loop gains can achieve the benefits of both rapid acquisition and reliable tracking simultaneously. The VBDPLL has a large loop gain at the beginning of a signal for rapid acquisition, which decreases as long as the signal is present for reliable tracking, and increases again when the signal disappears to be ready for rapid acquisition at the beginning of the next data burst. The bit synchronizer with a discrete number of possible loop gains (acquisition states) and timing error states is implemented as a finite state machine, with states defined by the quantized timing error and the loop gain. By defining a two-dimensional Markov chain, complete numerical solutions for the performance of the finite state machine VBDPLL bit synchronizer are derived, including the timing error pmf as a function of the preamble bit number k, the distribution of acquisition time and the distribution of the time to first bit slip. The results can also be applied directly to timing error detectors other than the zero-crossing phase detector considered here, provided that the noise parts of the timing error samples are independent from bit to bit. If not, additional states can be added. Future work includes a generalization of this analysis by adding additional states for other signaling waveforms, including partial response signaling, and higher order loops. [12]. A generalization for the case of frequency offsets is outlined in [12].

The Markov model is a powerful tool which makes it possible to analyse a discrete closed loop bit synchronizer in detail.

Appendix
Derivation Of State Transition Probabilities

In this Appendix we describe how to calculate the elements $p_{l|m}$ of the state transition matrix $\boldsymbol{P}$. In general these probabilities depend on the signaling waveform, signal-to-noise ratio and phase detector type. To simplify the analysis, we make the assumptions described in Section II and further assume that every zero crossing is due to a bit transition, there are no additional zero crossings due to noise, and the probability is zero that the zero crossing displacement due to noise is greater than $\pm T/2$. These assumptions will fail if the noise $\eta(t)$ is not sufficiently bandlimited and/or the signal to noise ratio is too low to assume a single zero crossing per bit interval [19].

We first find the discrete pmf of the zero crossing displacement n_k due to noise, use this to find the discrete pmf of the PD output y_k for each possible timing error, from which the state transition probabilities are found.

We define the discrete zero crossing pmf

$$u_i = Pr\{ZC \text{ in } (\Phi_i, \Phi_{i+1}]\} = \int_{\Phi_i}^{\Phi_{i+1}} f_{\mathbf{n_k}}(n_k) dn_k \quad i \in \{0, \ldots, M-1\}, \tag{32}$$

where $f_{\mathbf{n_k}}(n_k)$ is the density of the zero crossing displacement n_k.

For the data pulse shape given by (2) and a preamble data pattern, $f_{\mathbf{n_k}}(n_k)$ is given by the modulo T reduced zero crossing density of a sine wave in noise. A high signal-to-noise ratio approximation of $f_{\mathbf{n_k}}(n_k)$ is given by (33) below [12], [20].

The state transition probabilities can be calculated in terms of the u_i using the algorithm in Table III.

If the signal is absent, then the state transition probabilities may be found in exactly the same way, except that $u_i = 1/M$ for all i. Note that the time between state transitions is a random variable. With signal absent and AWGN filtered with a third-order Butterworth filter with 3 dB cutoff $1/2T$, the mean time between state transitions was found by simulation to be $0.7T$.

$$f_{\mathbf{n_k}}(n_k) = \begin{cases} \dfrac{1}{\sqrt{2\pi}\sigma_n} \exp\left\{-\dfrac{C^2 \sin^2(n_k \pi/T)}{2\sigma_n^2}\right\} \dfrac{C\pi}{T} \cos\left(\dfrac{\pi}{T} n_k\right) & \text{if} \quad |n_k| < T/2 \\ 0 & \text{if} \quad |n_k| \geq T/2 \end{cases} \tag{33}$$

TABLE III
ALGORITHM TO CALCULATE STATE TRANSITION PROBABILITIES

FOR $s_k = 0$ TO $(MN-1)$
  $K_k^* = \lfloor \frac{s_k}{M} \rfloor$
  $e_k^* = s_k - MK_k^*$
  FOR $y_k = (-\frac{M}{2}+1)$ TO $\frac{M}{2}$
    $z_k = f(y_k, K_k)$
    $e_{k+1}^* = e_k^* - z_k$
    $K_{k+1}^* = g^*(y_k, K_k^*)$
    $s_{k+1} = K_{k+1}^* M + e_{k+1}^*$
    $p_{s_k|s_{k+1}} = u_{\{e_k^* - y_k\}_{mod M}}$
  NEXT y_k
NEXT s_k

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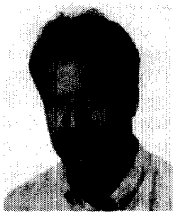
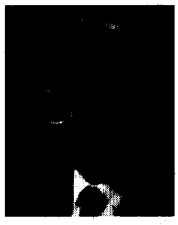


Helmuth Brügel (S'89–M'90) was born in Radolfzell, Germany, in 1963. He received the Dipl.-Ing. (FH) degree in communications engineering from the Fachhochschule Konstanz, Germany, in 1988, and the M.A.Sc. degree from the University of Victoria, B.C., Canada, in 1991.

In 1986 and 1987 he was a working student at AEG, Konstanz, where he was involved in the development of recognition systems. In 1991 he joined CGK Computer Gesellschaft Konstanz (a Siemens Nixdorf Information Systems company) where he is working in the Quality Control and Service department. His interests include mobile radio, digital signal processing and optical character recognition.



Peter F. Driessen (S'79–M'79–M'83–SM'93) received the Ph.D degree in electrical engineering from the University of British Columbia, Canada, in 1981.

He was with MacDonald Dettwiler and Associates, Vancouver, B.C., Canada, from 1981 to 1982 and worked on several projects for data transmission on HF radio. He was with MDI Mobile Data International from 1982 to 1985 as Senior Systems engineer, and worked on the design of a custom VLSI modem chip. Since 1986 he has been at the University of Victoria, Victoria, B.C., Canada, where he is now Associate Professor in the Department of Electrical and Computer Engineering. He was on sabbatical leave at AT&T Bell Laboratories, Holmdel, NJ, during the academic year 1992–1993, and worked on high-speed wireless indoor transmission. His research interests are in the areas of wireless communications systems, synchronization, and radio propagation.