DPLL Bit Synchronizer with Rapid Acquisition Using Adaptive Kalman Filtering Techniques

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Abstract—A second-order DPLL with time-varying loop gains is applied to the symbol synchronization of burst mode data signals. An algorithm to control the DPLL loop gains is derived from adaptive Kalman filtering theory. Simulation results for the variable gain DPLL compared to a fixed gain DPLL demonstrate the improved acquisition performance.

I. INTRODUCTION AND PRELIMINARIES

HEN data is transmitted in bursts or packets, rapid acquisition of symbol synchronization is important. The main novelties in this letter are the application of a DPLL with time-varying gains [1]–[7] to burst mode discrete time symbol synchronization, and the derivation of an algorithm to control the DPLL gains using Kalman filter theory. Simulation results show that the variable gain DPLL bit synchronizer acquires bit timing more rapidly than one with fixed gain. The acquisition and tracking performance is illustrated using a zero-crossing type of phase detector [8], [9] but the results for other types of phase detectors are expected to be similar.

To derive the update equations for a second-order DPLL, we define the unknown phase and frequency in terms of process and measurement equations of a Kalman filtering problem, and then show the Kalman gains to be equivalent to time-varying DPLL loop gains. For burst mode data where the signal may be absent at times, we adapt a method of [10] as a lock detector.

Consider the baseband binary communication system comprising transmit and receive filters $H_T(f)$, $H_R(f)$ forming a matched filter pair whose output is the binary PAM signal s(t). This signal model is motivated by packet radio data communications systems which use existing commercial VHF/UHF FM two-way radios. Data modulation of an RF carrier is achieved with filtered baseband nonreturn to zero (NRZ) data pulses of period T_1 applied to the input of the FM modulator in the transmitter. The resulting RF signal is a bandlimited binary FSK. Data demodulation is achieved by using the output of the FM discriminator in the receiver, filtered by $H_R(f)$. Thus s(t) is the input to the bit synchronizer and decision device. An unknown RF carrier frequency offset causes a dc shift in s(t) which can be easily compensated for. For cost reasons, timing information is obtained from the zero-crossing locations of s(t).

Since the receiver DPLL has a natural clock frequency $f_0=1/T_0 \neq f_1=1/T_1$, there is a clock frequency offset $f_{\triangle}=f_1-f_0$ between the clock rates of the transmitter

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and receiver. Thus, the input signal s(t) has a timing offset $\dot{t}=T_1-T_0$, where $\dot{t}/T_0\simeq -f_\triangle/f_0$ for $f_\triangle\ll 1$. We assume that \dot{t} is a random variable with some assumed probability density which takes on a sample value $\dot{t}_{k+1}=\dot{t}_k=T_1-T_0$ which is fixed for the duration of each data burst.

At the beginning of a data burst, we use a preamble with a 1010... dotting pattern with nominal timing epochs or zero crossing locations $t_k = kT_1 + t_0$ so that $t_{k+1} = t_k + T_1 = t_k + T_0 + \dot{t}_k$. For random data, a term representing intersymbol interference should be added [9], but is not required during the preamble. Estimates \hat{t}_k of t_k are based on noisy measurements $x_k = t_k + n_k$. The DPLL zc-type phase detector (PD) generates an output $z_k = x_k - \hat{t}_k = t_k - \hat{t}_k + n_k \in (-T_0/2, T_0/2]$. The probability density of the noise n_k will depend on the signal-to-noise ratio, amount of timing error, and details of the timing error detector used to generate the PD output from the input signal. From [8], a second-order DPLL estimates \hat{t}_k recursively from the PD outputs z_k via

$$\hat{t}_{k+1} = \hat{t}_k + T_0 + K_{0f} z_k + K_{1f} \sum_{i=0}^k z_i$$
 (1)

where K_{0f} and K_{1f} are fixed DPLL loop gains.

II. KALMAN FILTER MODEL FOR DPLL

In this section, the DPLL timing phase estimate (1) with time-varying gains $K_{0,k}$ and $K_{1,k}$ is derived using a Kalman filter model. To establish the model, we define a signal vector $\mathbf{E_k}^T = [\epsilon_k \, \dot{\epsilon}_k]$ with $\epsilon_k = t_k - kT_0 = t_0 + k(T_1 - T_0)$ and $\dot{\epsilon}_k = \dot{t}_k$, and write process or signal model equations

$$\mathbf{E}_{\mathbf{k}+\mathbf{1}} = \mathbf{\Phi}\mathbf{E}_{\mathbf{k}} + \mathbf{U}_{\mathbf{k}} \tag{2}$$

with $\Phi = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$ and $\mathbf{U_k} = \begin{bmatrix} u_k \\ w_k \end{bmatrix}$ representing a zero mean white phase jitter u_k and timing offset jitter w_k . The values of $E[u_k^2] = \sigma_u^2$ and $E[w_k]^2 = \sigma_w^2$ for burst mode data are discussed in Section III. Defining $\tau_k = x_k - kT_0$, we write the measurement equation

$$\tau_k = \mathbf{H}\mathbf{E_k} + n_k \tag{3}$$

where $\mathbf{H}=[10]$. n_k is assumed to be white with $E[n_k]=0$, and $E[n_k^2]$ is an a priori estimate $\hat{\sigma}_n^2$ of the noise variance. We define $\hat{\mathbf{E}}_{\mathbf{k}|\mathbf{k}-1}^{\mathbf{T}}=[\hat{\epsilon}_{k|k-1}\,\hat{\epsilon}_{k|k-1}]=[\hat{t}_k-kT_0\,\hat{t}_k]$ as the estimate of $\mathbf{E}_{\mathbf{k}}$ which is obtained using the Kalman filter

 1 For the ZC_1 sampling DPLL as defined in [8], if $\hat{t}_k \simeq x_k$, then the sequence of signal samples $z_k^* \simeq \hat{t}_k - x_k = -z_k$ aside from a constant factor. In [8], the filtered samples $y_k = K_0 z_k^* + K_1 \sum_{i=0}^k z_i^*$ are used in the update $\hat{t}_{k+1} - \hat{t}_k = T_0 - y_k$ which is equivalent to (1).

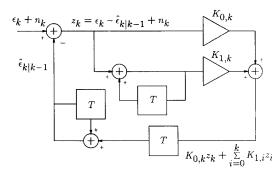


Fig. 1. Second-order DPLL with variable loop gains.

algorithm with initial conditions $\hat{\mathbf{E}}_{\mathbf{0}|-1}^{\mathbf{T}} = [0\,0]$, and $\mathbf{V}_{\mathbf{0}|-1} = \begin{bmatrix} T_0^2/12 & 0 \\ 0 & T_0^2 f_{\Delta n}^2 \end{bmatrix}$. In $\mathbf{V}_{\mathbf{0}|-1}$, $E[(\hat{\epsilon}_{\mathbf{0}|-1})^2] = T_0^2/12$ is the variance of the uniform distribution of the initial phase ϵ_0 . $E[(\hat{\epsilon}_{\mathbf{0}|-1})^2] = T_0^2 f_{\Delta n}^2$, where $f_{\Delta n}^2 = E[(f_{\Delta}/f_0)^2]$ is the normalized variance of an assumed zero mean distribution for f_{Δ} .

We further define $\mathbf{K_k}^T = [K_{0,k} \ K_{1,k}]$ to be the Kalman gain vector, and $\sigma_{\mathbf{U}}^2 = \begin{bmatrix} \sigma_u^2 & 0 \\ 0 & \sigma_w^2 \end{bmatrix}$ to be the driving noise variance independent of k.

The Kalman filter equations for the process (2) and the measurements (3) can be simplified by combining the two equations for $\hat{\mathbf{E}}$ and noting that $(\tau_k - \mathbf{H}\hat{\mathbf{E}}_{\mathbf{k}|\mathbf{k}-\mathbf{1}}) = z_k$ to obtain

$$\mathbf{K}_{\mathbf{k}} = \mathbf{V}_{\mathbf{k}|\mathbf{k}-1} \mathbf{H}^{\mathbf{T}} [\mathbf{H} \mathbf{V}_{\mathbf{k}|\mathbf{k}-1} \mathbf{H}^{\mathbf{T}} + \hat{\sigma}_{n}^{2}]^{-1}$$
(4)

$$V_{\mathbf{k}|\mathbf{k}} = V_{\mathbf{k}|\mathbf{k}-1} - K_{\mathbf{k}}HV_{\mathbf{k}|\mathbf{k}-1}$$
 (5)

$$\mathbf{V}_{\mathbf{k}+\mathbf{1}|\mathbf{k}} = \mathbf{\Phi} \mathbf{V}_{\mathbf{k}|\mathbf{k}} \mathbf{\Phi}^{\mathbf{T}} + \sigma_{\mathbf{I}\mathbf{I}}^{\mathbf{2}} \tag{6}$$

$$\hat{\mathbf{E}}_{\mathbf{k+1}|\mathbf{k}} = \mathbf{\Phi}\hat{\mathbf{E}}_{\mathbf{k}|\mathbf{k-1}} + \mathbf{\Phi}\mathbf{K}_{\mathbf{k}}z_{\mathbf{k}} \tag{7}$$

The DPLL update (1) can be derived by writing (7) as two scalar equations for each k=0,1,... and substituting as follows.

$$\hat{\epsilon}_{1|0} = \hat{\epsilon}_{0|-1} + \hat{\epsilon}_{0|-1} + K_{0,0}z_0 + K_{1,0}z_0,$$

$$\hat{\epsilon}_{1|0} = \hat{\epsilon}_{0|-1} + K_{1,0}z_0$$
(8)

$$\hat{\epsilon}_{2|1} = \hat{\epsilon}_{1|0} + \hat{\epsilon}_{1|0} + K_{0,1}z_1 + K_{1,1}z_1
= \hat{\epsilon}_{1|0} + \hat{\epsilon}_{0|-1} + K_{1,0}z_0 + K_{0,1}z_1 + K_{1,1}z_1
= \hat{\epsilon}_{1|0} + K_{0,1}z_1 + \sum_{i=0}^{1} K_{1,i}z_i$$
(9)

$$\hat{\epsilon}_{k+1|k} = \hat{\epsilon}_{k|k-1} + K_{0,k} z_k + \sum_{i=0}^{k} K_{1,i} z_i$$
 (10)

Equation (10) is equivalent to (1) with time-varying gains $K_{0,k}$ and $K_{1,k}$ (Fig. 1).

III. SIMULATION METHODS AND RESULTS

For simulation of the DPLL synchronizer with burst mode data, a lock detector algorithm is required. The example

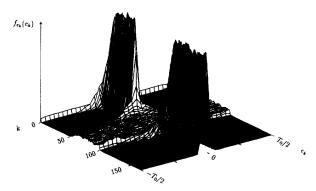
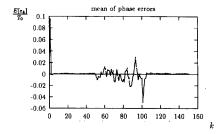


Fig. 2. $f_{\varepsilon_k}(e_k)$ versus k, second-order DPLL, variable loop gains with lower bounds $K_{0f}=0.2, K_{1f}=0.05, E_b/N_0=10.6$ dB, $\sigma_n^2/T_0^2=\hat{\sigma}_0^2/T_0^2=0.001, f_{\Delta}/f_0=0.1, w=3, a=10$, histogram with 31 bins, 1000 trials

algorithm used in the simulations is to modify the approach of [10] such that we set $\sigma_u^2 = \sigma_w^2 = T_0^2/12$ in (6) when a windowed average $\sum_{i=0}^w z_{k-i} > a\sigma_n$ and to set $\sigma_u^2 = \sigma_w^2 = 0$ otherwise. Alternatively, a more complex multistage in-lock and out- of-lock detection algorithm may be employed which trades off acquisition, tracking and false lock performance according to the system requirements. Such tradeoff issues are beyond the scope of this letter.

To establish the synchronizer performance, we define the actual timing error $e_k = \epsilon_k - \hat{\epsilon}_{k|k-1}$ whose density $f_{e_k}(e_k)$ versus bit number k (counted from the beginning of a data burst) may be readily obtained by simulation. Thus $E[e_k^2]$ versus k is adopted here as a useful measure of synchronizer performance, and will depend on the densities of $\epsilon_0, \dot{\epsilon}_0$, Kalman parameters $\hat{\mathbf{E}}_{0|-1}, \mathbf{V}_{0|-1}, a\ priori$ estimate $\hat{\sigma}_n^2$, actual E_b/N_0 , and lock detector parameters w, a. When comparing the performance of fixed and variable gain DPLL's, we set $K_{0,k} \geq K_{0f}$ and $K_{1,k} \geq K_{1f}$ for all k, so that the tracking performance ($E[e_k^2]$ as $k \to \infty$) is the same for both cases.

Simulations have been carried out with data present for $0 < t < 50T_1$, data absent for $50T_1 < t < 100T_1$, and data present for $100T_1 < t < 150T_1$. Since the start time t_k of the first data burst is known to be at k=0, the gains $\mathbf{K_k}$ for k < 50 are fixed by the initial conditions to yield a linear MMSE estimate of the timing error. Since the start time k = 100 of the second burst is unknown to the DPLL (as occurs in practice), the gains K_k for 50 < k < 150 are random variables which change with time k. Fig. 2 shows that $f_{e_k}(e_k)$ is sharply peaked near 0 when the signal is present, and uniformly distributed when the signal is absent. The mean and variance of $f_{e_k}(e_k)$ versus k in Fig. 3 show that the acquisition time when the start time is unknown is degraded only slightly compared to that when the start time is known. This is because when the signal is absent, then the densities $f_{K_{0,k}}(K_{0,k})$ and $f_{K_{1,k}}(K_{1,k})$ are peaked near $K_{0,k} = K_{1,k} = 1$ (Fig. 4), thus yielding reliable rapid acquisition. For comparison, Fig. 5 shows the mean and variance of $f_{e_k}(e_k)$ versus k for a DPLL with fixed gains K_{0f} , K_{1f} . The improvement in acquisition performance resulting from the time-varying gains is clearly evident from a comparison of Fig. 3 with Fig. 5.



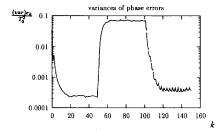


Fig. 3. $\frac{E[e_k]}{T_0}$ versus k. $\frac{(\mathrm{var})e_k}{T_0^2}$ versus k. Second-order DPLL, variable loop gains with lower bounds $K_{0f}=0.2,\,K_{1f}=0.05.E_b/N_0=10.6$ dB, $\sigma_n^2/T_0^2=0.001,f_\Delta/f_0=0.1,w=3,a=10.$

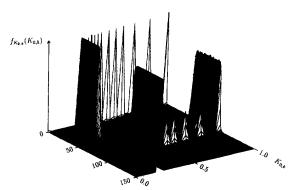
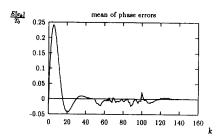


Fig. 4. Second-order DPLL, variable loop gains with lower bounds $K_{0f}=0.2,K_{1f}=0.05.E_b/N_0=10.6$ dB, $\sigma_n^2/T_0^2=0.001,f_\Delta/$ $f_0 = 0.1, w = 3, a = 10$, histogram with 31 bins, 1000 trials.

IV. CONCLUSIONS

The update equation for a second-order DPLL bit synchronizer with a zero-crossing phase detector has been derived starting from a Kalman filter model of the phase process. This derivation leads to time-varying Kalman gains in the DPLL. The acquisition performance of this DPLL bit synchronizer is improved significantly by using these time-varying loop gains in place of the fixed gains of a conventional DPLL. At the end of a data burst, the loop gains can be increased either adaptively or by a priori knowledge of the end-of-burst time to permit rapid acquisition on the next data burst. The use



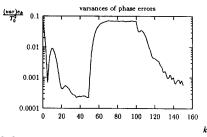


Fig. 5. $\frac{E[e_k]}{T_0}$ versus k. $\frac{(\text{var})e_k}{T_0}$ versus k. Second-order DPLL, fixed loop gains $K_{0f}=0.2$, $K_{1f}=0.05.E_b/N_0=10.6$ dB, $\sigma_n^2/T_0^2=\hat{\sigma}_n^2/T_0^2=0.001, f_\Delta/f_0=0.1$.

of time varying loop gains in the DPLL makes it possible to achieve both rapid acquisition and reliable tracking without the tradeoffs associated with conventional fixed loop gain DPLL's.

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REFERENCES

- R.D. Gitlin and J. Salz, "Timing recovery in PAM systems," Bell Syst. Tech. J., vol. 50, no. 5, pp. 1645-1669, May-June 1971.
 D.R. Polk and S.C. Gupta, "Quasi-optimum digital phase-locked loops", IEEE Trans. Comm., vol. COM-21, pp. 75-82, Jan. 1973.
 P.R. Hirshler and J.P. Perronet, "Simultaneous detection and timing
- recovery with adaptive filter," Int. Conf. Inform. Theory Syst. Theory Digital Commun., Berlin, Germany, Sept. 1978.

 E.Akinci, M.Oberle, and G. Maral, "Bit synchronization and detection
- by extended Kalman filtering algorithm implemented with microprocessor," *IEEE GLOBECOM Conf.*, 1982, pp. 901-905.

 O. Nakajima, H.Hikawa, and S.Mori, "Performance improvement of
- all digital phase-locked loop with adaptive multilevel-quantized phase comparator," Trans. IEICE, vol. E72, no. 3, pp. 194-201, Mar. 1989.
- S.A. Merritt, "The iterated extended Kalman phase detector," *IEEE Trans. Commun.*, vol. 37, pp. 522-526, May 1989.
 A. Aghamohammadi, H. Meyr, and G. Ascheid, "Adaptive synchroniza-
- tion and channel parameter estimation using an extended Kalman filter," IEEE Trans. Commun., vol. 37, pp. 1212-1219, Nov. 1989. W. C. Lindsay and C.M. Chie, "A survey of digital phase-locked loops,"
- Proc. IEEE, vol. 69, pp. 410- 431, Apr. 1981.
 P. Ogmundsen and P. F. Driessen, "Zero-crossing DPLL bit synchro-
- nizer with pattern jitter compensation," IEEE Trans. Commun., vol. 39, pp. 961-969, Apr. 1991. A. H. Jazwinski, Stochastic Processes and Filtering Theory. New
- York: Academic, 1970, pp. 311-313.