### Introduction of lab project --- ELEC 454

(Design and realization of a Two-Stage, Low-Noise Microstrip Transistor Amplifier)

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## Outline

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#### Contact information

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Lab section: ELEC454LS02

 Time:
 On Feb.4, Feb.25, Mar. 10, and Mar. 24; 14:30 to 17:30

 Location:
 ELW-A359

You may reach me in my lab or office from 9:30am to 5:00pm on week days.

### Brief introduction of this lab project

- In order to reinforce the theories and techniques learnt in an engineering course, the best way is to put them into practice. The purpose of this laboratory project is to realize a complete microstrip transistor amplifier using the design methods discussed in this course as well as employing commercial design software packages.
- 2. We will design a two-stage low noise amplifier working in the frequency range of 1.4 to 1.6GHz.
- 3. The active devices are RF bipolar transistors which are easier to match at these frequencies and offer almost the same noise performance as FETs.



Amplifie	r Specifications
Frequency Band	1.4 to 1.6GHz
Gain	$\geq 20 \text{ dB} \pm 0.5 \text{ dB}$
Noise Figure	< 2 dB
S <sub>11</sub>	< -10 dB
S <sub>22</sub>	< -16 dB

#### Stability Check

For a two-port device with a  $2 \times 2$  S-parameter matrix, the stability factor is given as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$
  
$$\Delta = S - S - S - S$$

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where  $\Delta$  is the determinant of the scattering matrix. A two-port device is unconditionally stable if K > 1 and  $|\Delta| \leq 1$ .

12<sup>1</sup>21

#### Theory related to amplifier design





Therefore, we can solve for  $\Gamma_{\rm in}$  as

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

Similarly, the output reflection coefficient is given as

$$\Gamma_{out} = \frac{V_2^-}{V_2^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}$$



In order to have the maximum power transferred, we want to use conjugate impedance matching, therefore we have:

$$\Gamma_{in} = \Gamma_S^* \quad \Gamma_{out} = \Gamma_L^*$$

The maximum total gain resulting from this match, assuming lossless sections, becomes:

$$G_{T_{\text{max}}} = \frac{1}{1 - |\Gamma_{S}|^{2}} |S_{21}|^{2} \frac{1 - |\Gamma_{L}|^{2}}{|1 - S_{22}\Gamma_{L}|^{2}}$$

For a bilateral device we have:

$$\Gamma_{S} = \frac{B_{1} \pm \sqrt{B_{1}^{2} - 4|C_{1}|^{2}}}{2C_{1}} \quad B_{1} = 1 + |S_{11}|^{2} - |S_{22}|^{2} - |\Delta|^{2}}{B_{2} = 1 + |S_{22}|^{2} - |S_{11}|^{2} - |\Delta|^{2}}$$
$$\Gamma_{L} = \frac{B_{2} \pm \sqrt{B_{2}^{2} - 4|C_{2}|^{2}}}{2C_{2}} \quad C_{1} = S_{11} - \Delta S_{22}^{*}}{C_{2} = S_{22} - \Delta S_{11}^{*}}$$

Once  $\Gamma_s$  and  $\Gamma_L$  are identified, the input and output matching networks can be built for optimum gain.

## Theory related to amplifier design

For a unilateral device we have:  $S_{12} = 0$ 

$$\Gamma_{S} = S_{11} \quad \Gamma_{L} = S_{22}$$

In this case, the maximum total transistor gain is given by

$$G_{TU_{\text{max}}} = \frac{1}{1 - |S_{11}|^2} |S_{21}|^2 \frac{1}{1 - |S_{22}|^2}$$

Obviously a unilateral device has much simplified equations, therefore even when  $S_{12}$  is small but not exactly zero, it may still be desirable to assume the unilateral case for initial designs if the discrepancy is acceptable.

The range of the error introduced by this assumption can be approximated by the *unilateral figure of merit*:

$$U = \frac{|S_{12}||S_{21}||S_{11}||S_{22}|}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$$
$$\frac{1}{(1 + U)^2} < \frac{G_T}{G_{TU}} < \frac{1}{(1 - U)^2}$$

If the requirements specified allow such error range, the device can be assumed unilateral for a quicker design.

Theory related to amplifier design

#### Noise Figure:

Circles of constant noise figure:

#### Center:

r: 
$$C_F = \frac{1}{N+1}$$
  
s:  $R_F = \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{N+1}$   $N = \frac{F-F_{min}}{4R_N/Z_0} |1+\Gamma_{opt}|^2$ 

Radius

for a cascaded system with several two-port devices like the one we have, the overall noise figure is given as

$$F_{overall} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots$$

## Initial design

The objective of our project is to design a two-stage amplifier operating in the 1.4 to 1.6 GHz range. Both the minimum noise figure and maximum transducer power gain should be achieved by the design.



The design should employ two bipolar transistors, NE85639: the first one should operate at  $V_{CE} = 10$ V and  $I_C = 7$ mA for low noise condition, the second one should be optimized for power amplification at  $V_{CE} = 10$ V and  $I_C = 20$ mA.

## Initial design

The S-parameters of the transistor for the two bias conditions at 1.5GHz and  $Z_0 = 50 \Omega$  were provided by the manufacturer. So we can proceed according to the theory presented in the previous slides:

- 1. Stability Check
- 2. Noise Figure Check
- 3. Input Matching Network design
- 4. Inter-Stage Matching Network design
- 5. Output Matching Network design

### Input Matching Network



The first stage has the dominant effect on the overall system noise; therefore, we want it to be as small as possible. The noise is minimized when  $\Gamma_{S1} = \Gamma_{opt}$ .

•  $\Gamma_{opt}$  is given (0.43*e*-*j*174°) so by using a Smith Chart, we can match  $\Gamma_{S1}$  to the characteristic impedance of 50 $\Omega$  to get the input matching network.

• In order to make the stub susceptance less sensitive to frequency changes, we change the L-section network to a T-section by replacing the single shunt stub by two shorter stubs.



## **Output Matching Network**



• Finally we design the output matching network. In the same way as we have calculated the inter-stage matching network, we can calculate  $\Gamma_{1,2} = \Gamma_{out2}^{*}$ .

- We can design the output matching network by matching  $\Gamma_{L2}$  to the load impedance of 50  $\Omega$ .





## Computer Analysis

Initial design result with ideal transmission line elements :





## PCB Design

Overall Circuit Design with Bias Circuits and Matching Networks



## PCB Design

#### Bias Circuit Design:

For the first stage	For the second stage
$V_{CE} = 10V  I_C = 7mA$	$V_{CE} = 10V  I_C = 20mA$
$h_{FE} = 120  V_{CC} = 20V$	$h_{FE} = 120  V_{CC} = 20V$

Using the assumptions that for both stages:  $V_{BE} = 0.7$ V,  $I_{BB} = 5I_B$ ,  $V_{BB} = 2$ V, we can calculate:

For the first stage	For the second stage
$Rb_1 = 22.3 \mathrm{k} \Omega$	$Rb_2 = 7.78 \mathrm{k}  \Omega$
$Rb_{11} = 22.84 \text{k} \Omega$	$Rb_{21} = 10k \Omega$
$Rb_{12} = 6.85 \text{k} \Omega$	$Rb_{22} = 2.4 \text{k} \Omega$
$R_{1\mathrm{C}} = 1.36\mathrm{k}\Omega$	$R_{\rm 2C} = 476 \Omega$

## PCB Design

#### **Board Layout:**

You can create your layout according to your optimized transmission line parameters and bias circuit design.

### Manufacture and Measurement

• Our amplifier board will be fabricated by an external company and populated by the lab technician.

• When the board is ready, we will check the bias circuits using a regular power supply and a digital multi-meter.

• We then verify our design by measuring gain and noise figure over the specified frequency band (1.4 to 1.6 GHz).

Initial Design (using Smith Chart)	
Stability circles Noise circle Input matching network Inter-stage matching network Transducer Power Gain	30
Computer Analysis (using ADS) Stability circles Noise circle Analysis of the first design using 'ideal' elements	10

# Project marking scheme (continued)

Testing Test bias voltages of completed amplifier Measure gain and noise figure Compare with expectations	5
Discussions/Conclusions	15
Overall Report	
Introduction Initial design data, observation, discuss difficulties, problems, etc. Touchstone design data, observation, discuss difficulties, problems, etc. PCB design	15
Total	100

## Time schedule

Lab period 1: (Feb. 4, 2:30-5:30pm ELW-A359)

Using transistor data, make a preliminary design of the amplifier at 1.5GHz following the steps shown on page a-16 in lab manual.

Lab period 2: (Feb. 25, 2:30-5:30pm ELW-A359)

Computer analysis by using ADS

Bias circuit design

Lab period 3: (Mar. 10, 2:30-5:30pm ELW-A359)

Finish final PCB board

Lab period 4: (Mar. 24, 2:30-5:30pm ELW-A359) Testing of the amplifier

Lab report is due one week after the last lab.